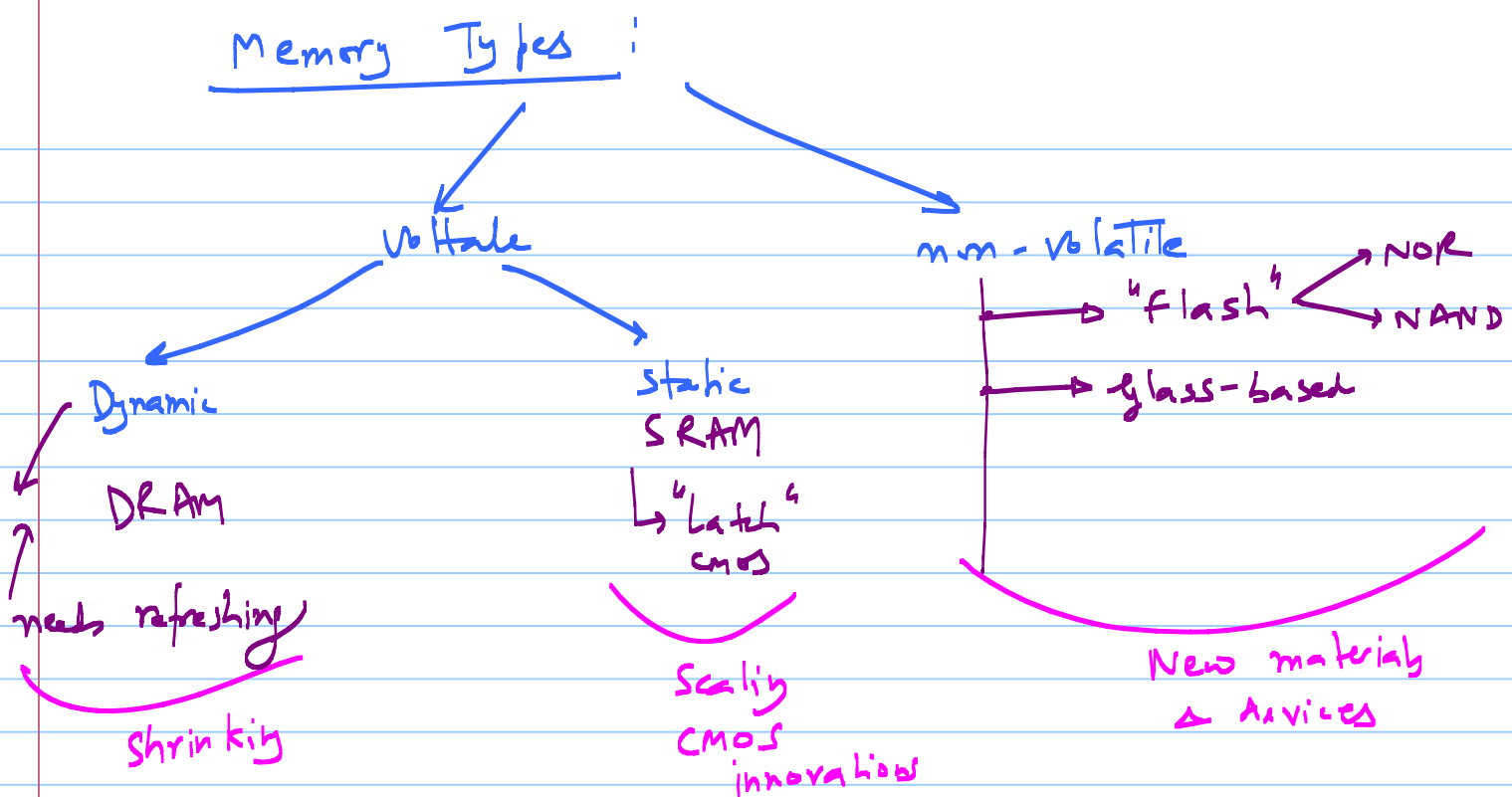
ECE 518 - Lecture 1

Note Title 1/22/2013

Elements of Memory IC Design

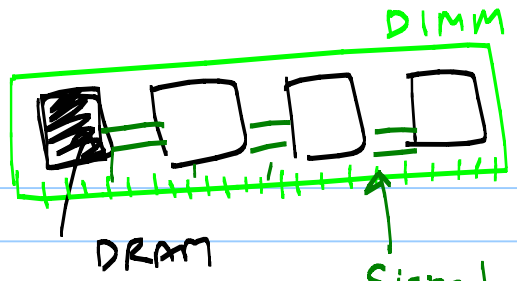
- operation of the memory cell (device design)
- array design (architecture)
- sensing circuits & peripheral circuits
- clocking circuits, I/O


Memory Types :
Volatile
non-volatile
Dynamic
DRAM
needs refreshing
Shrinking
Static
SRAM
"Latch"
CMOS
Scaling
CMOS
innovations
"flash"
NOR
NAND
glass-based
New materials
& devices

Considerations:

1. Memory Density
2. Latency (access speed)

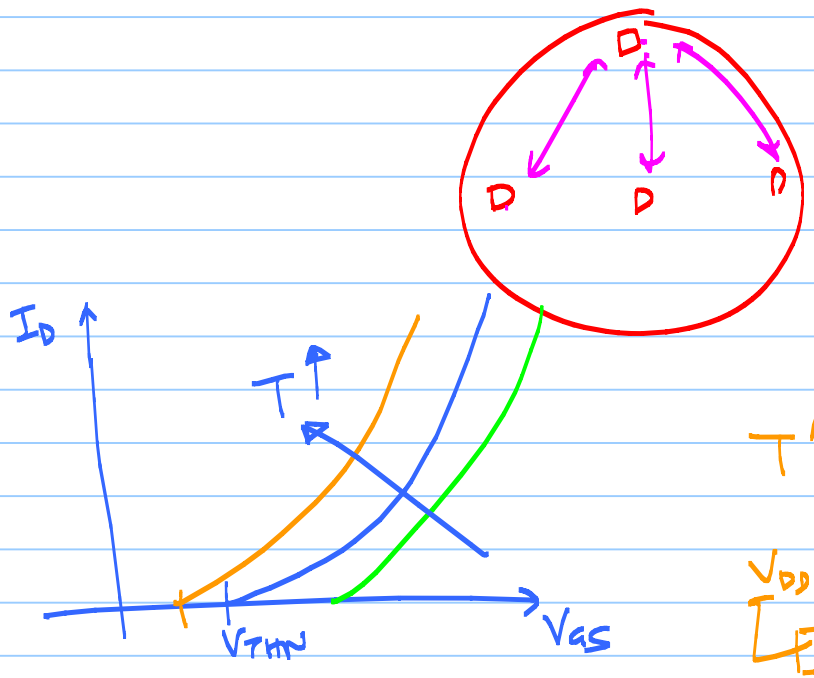
SRAM > DRAM > HDD

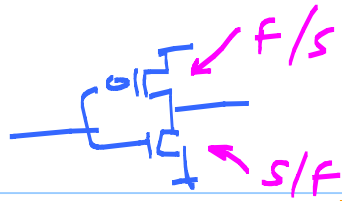


NOR
NAND
"Strata Flash"

3. Power Consumption
4. Process → compatible with CMOS ?
5. scaling ⇒ circuit design challenges with V_{DD} ↓
   - leakage
   - Variability

Process Corners CMOS





Spectre

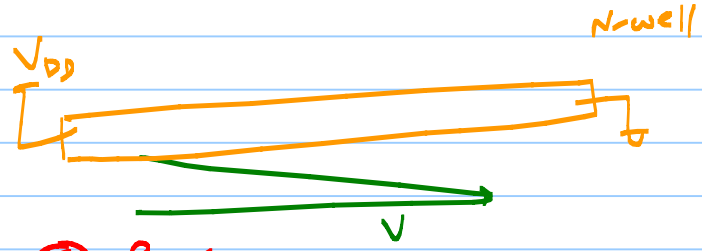
① models

- TT
- SF
- SS
- FF
- FS

② T ⇒ 0°C → 75°C

V_{THN}

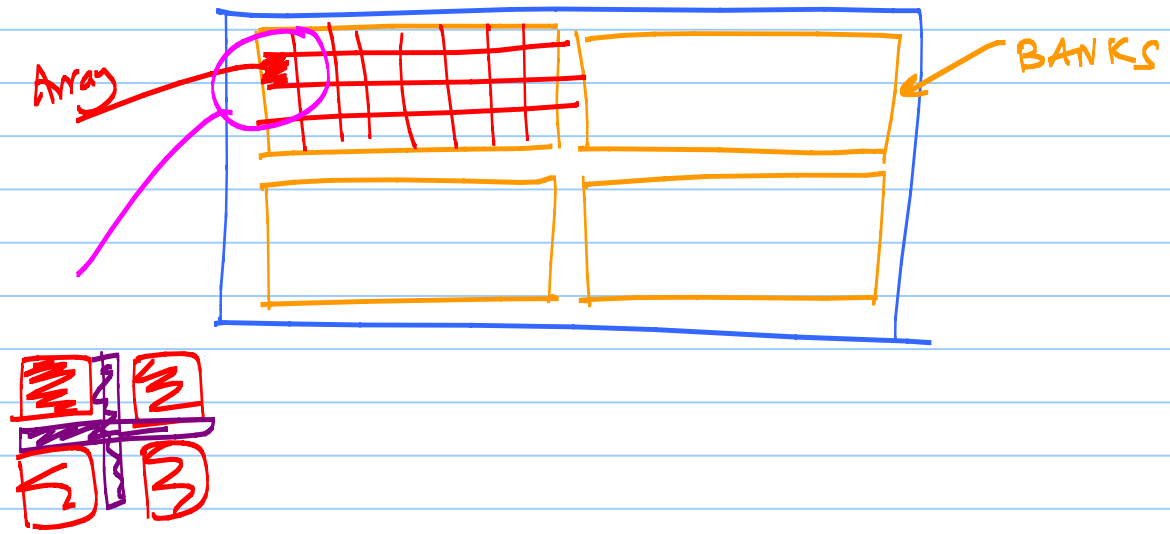
T ↑, V_{THN} ↓



③ R, C variations

±20 % → die-to-die

19. on same chip



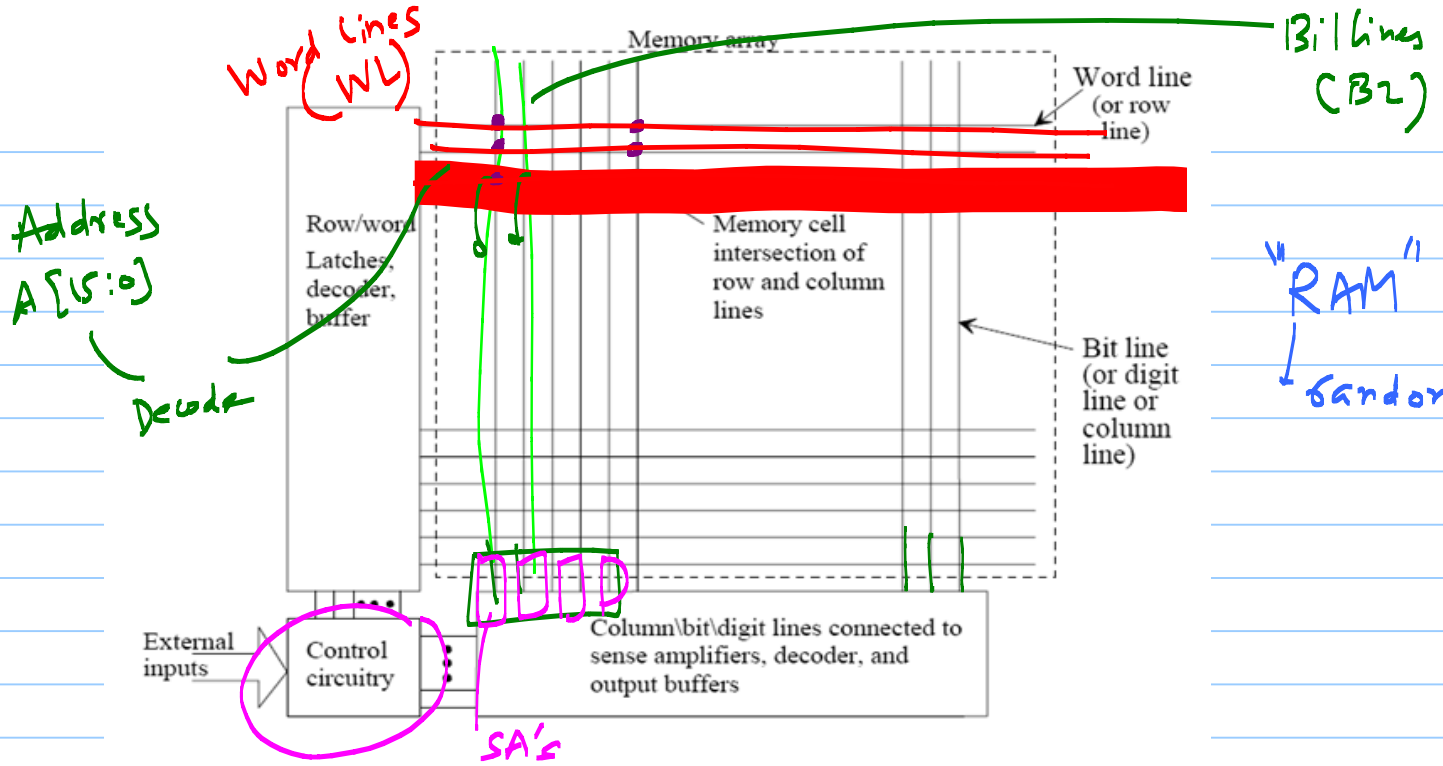
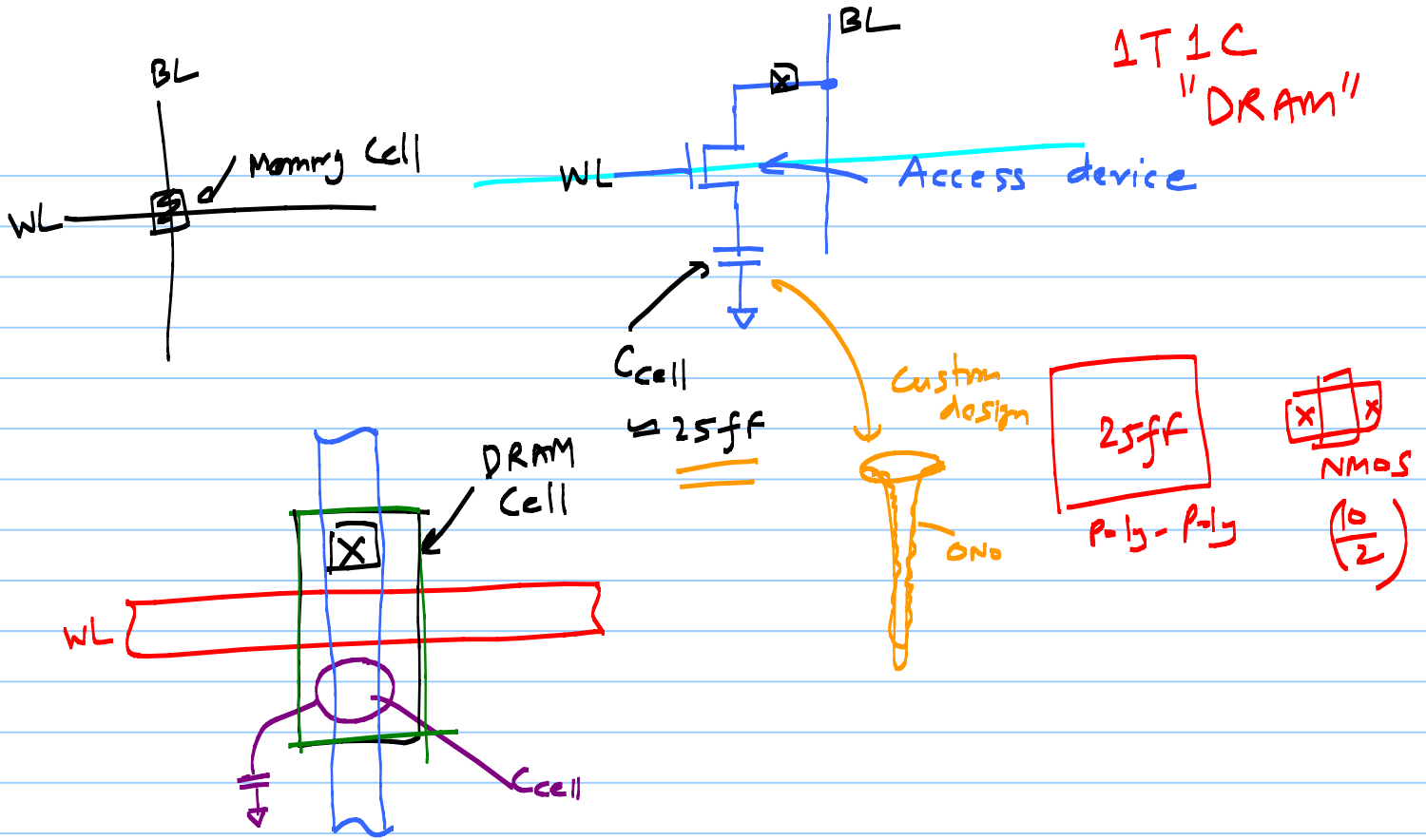
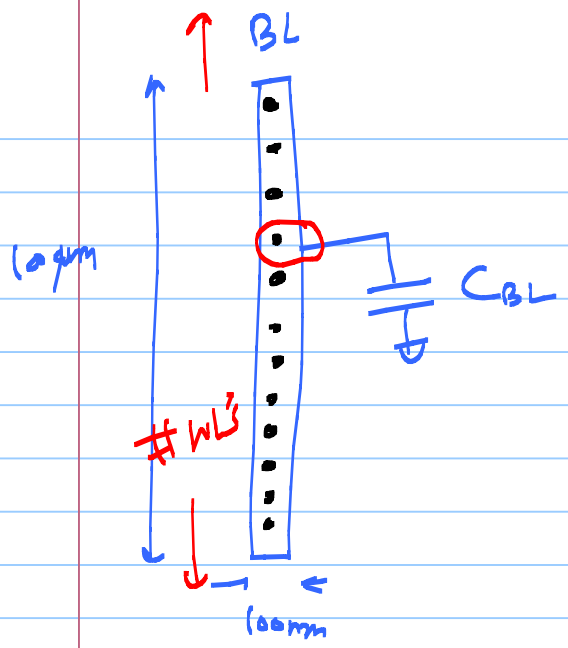


Figure 16.1 Block diagram of random access memory.


BL
Memory Cell
WL
BL
WL
Access device
1T1C
"DRAM"
C_{cell}
≈ 25ff
Custom design
25ff
Poly - Poly
NMOS
(10/2)
ONO
DRAM Cell
WL
C_{cell}



BL ↑ ⇒ WL is long
↳ slow to drive

$t_d = 0.35 R_D C_D l_L$

WL ↑ ⇒ more # of cells on the BL
⇒ more cap on BL
⇒ small signal after sensing
⇒ slow (RC↑)