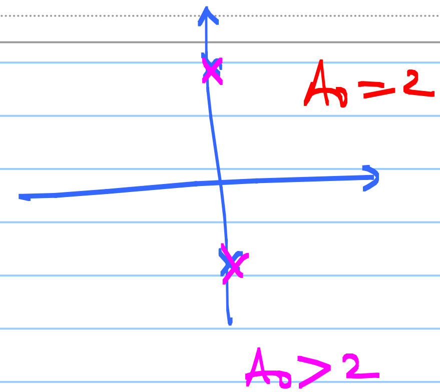
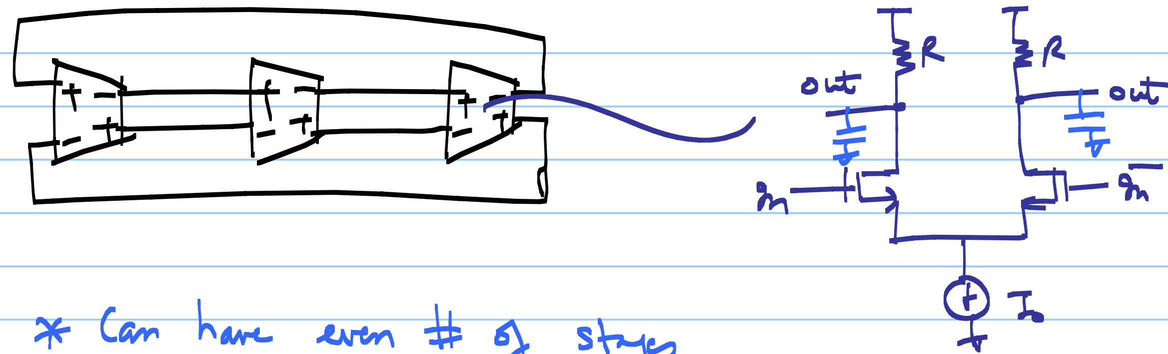
ECE 518 - Lecture 19

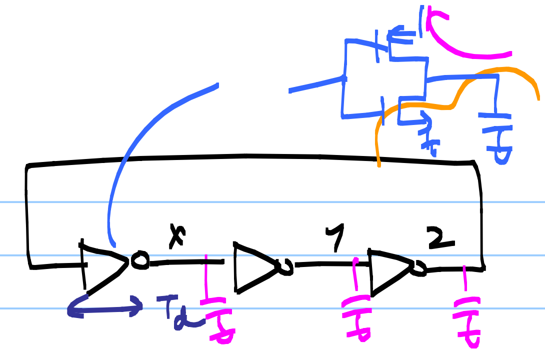
Note Title 4/2/2013

for 3-stage oscillator $\quad \omega_{osc} = \frac{A_o}{2}\omega_o\sqrt{3}$

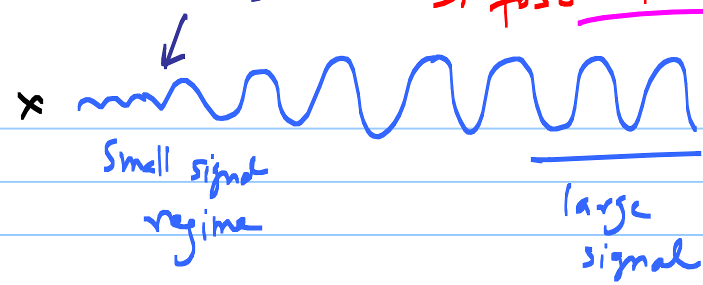


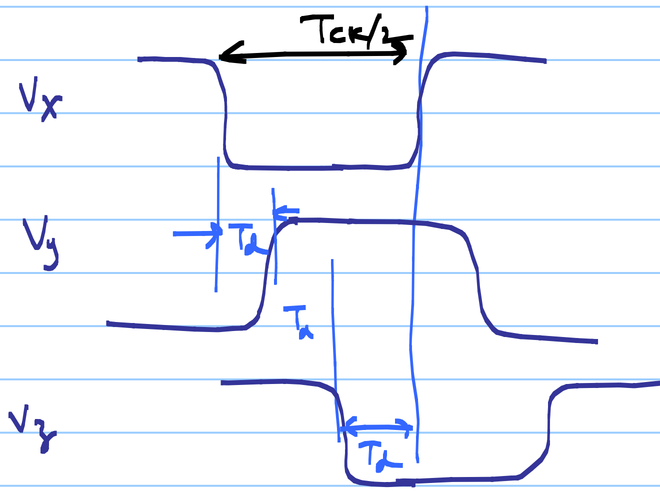


* Can have even # of stages
with differential design



$\omega_{osc} = \omega_0\sqrt{3} \Rightarrow f_{osc} = f_0\sqrt{3}$





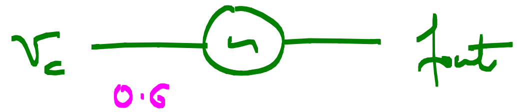
$\frac{T_{ck}}{2} = 3T_d$

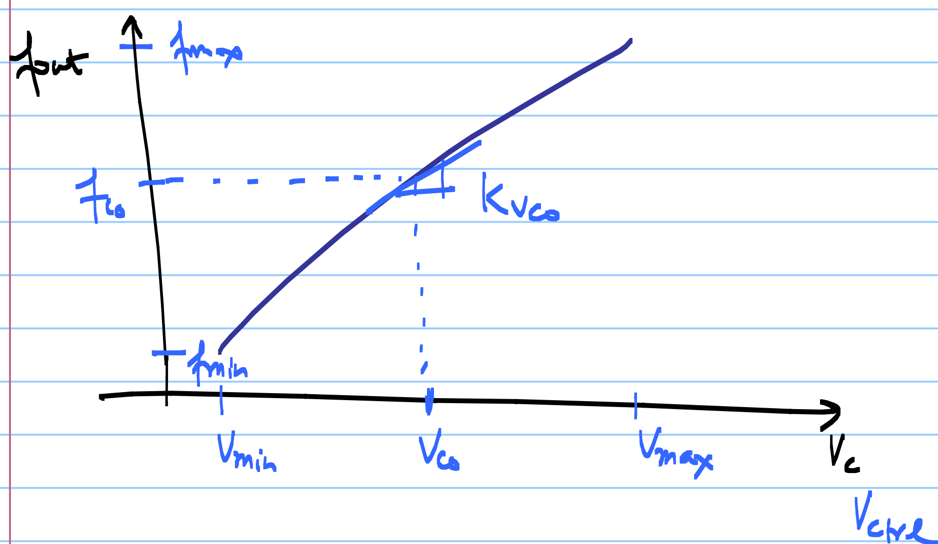
$\omega_0 = \frac{1}{RC}$

$\Rightarrow T_{ck} = 6T_d$

$\Rightarrow f_{osc} = \boxed{\frac{1}{6T_d}} < f_0\sqrt{3}$

VCOs





$$f_{out} = f_0 + 2\pi K_{VCO} \cdot v_c(t)$$

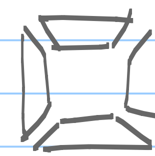
incremental phase domain $\qquad \phi_{out} = 2\pi K_{VCO} \int_{-\infty}^{t} v_c(t)\,dt$

ASIDE

XTAL

BAW

MEMS



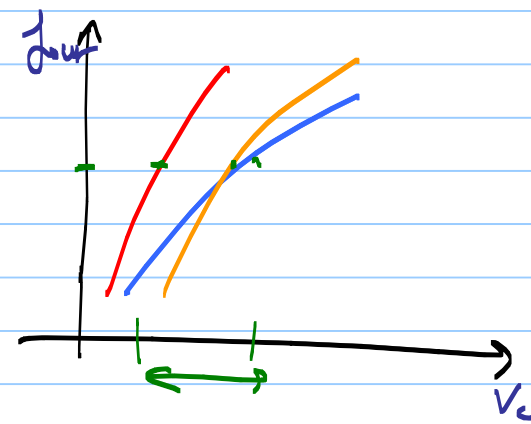
"SiTime"

"PVT"

Laplace domain : $\phi_{out}(s) = \frac{2\pi K_{VCO}}{s} \cdot V_c(s)$

Performance Metrics : * K_{VCO}

* Tuning range :



* 50% frequency variation across PVT corners

* Need a wide-enough tuning range to cover PVT variation

↳ ASIC's need 5X tuning range

Spectre

* UltraSim
* FastSpice
* UltraSpice

* <u>Tuning Linearity:</u>

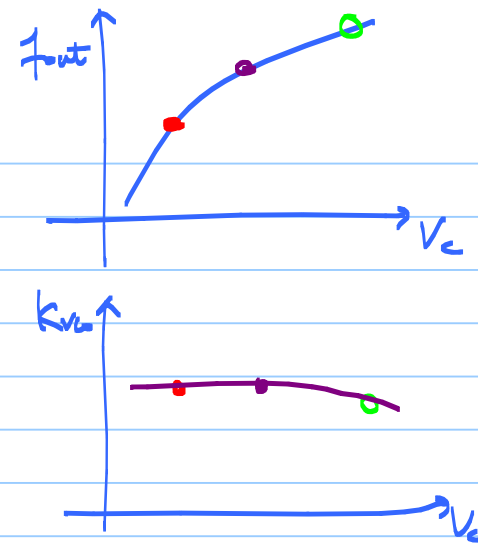
↳ Kvco depends upon fout

↳ Affects loop dynamics

↳ BW & PM

↳ ring VCO → 2–3x variation

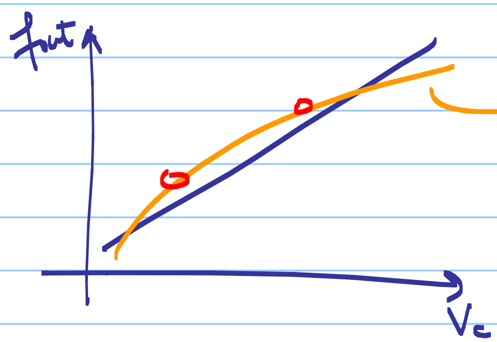
↳ can "linearize" VCO



* <u>Power</u> → tradeoff noise & power

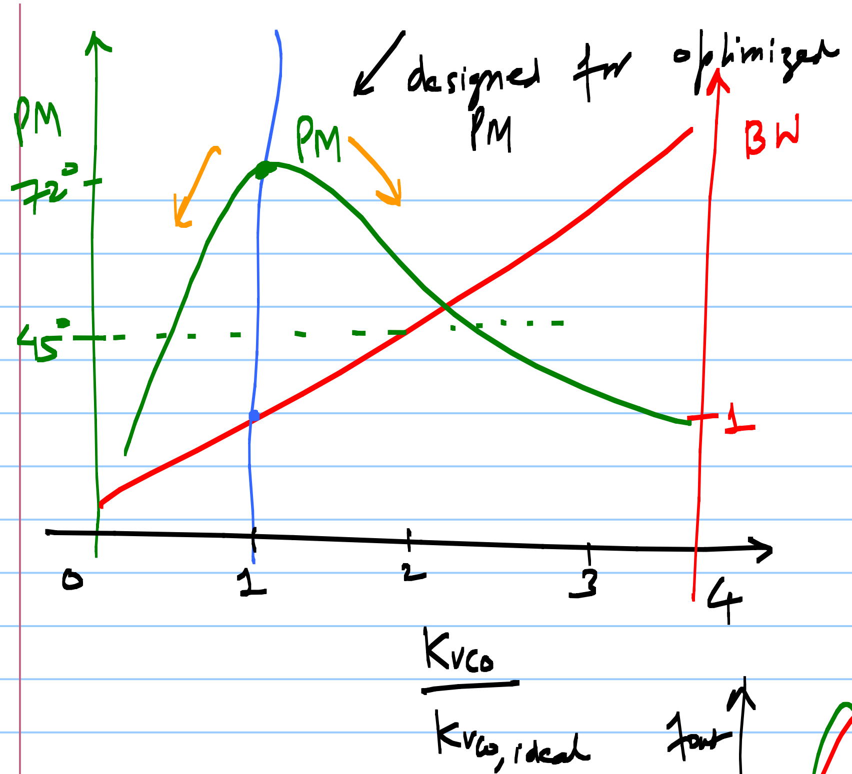
* <u>PSRR</u> ⇒ power supply noise should not limit the jitter performance

Tuning linearity



$K_{VCO} = f(f_{out})$

↳ behavior depends upon the operating frequency



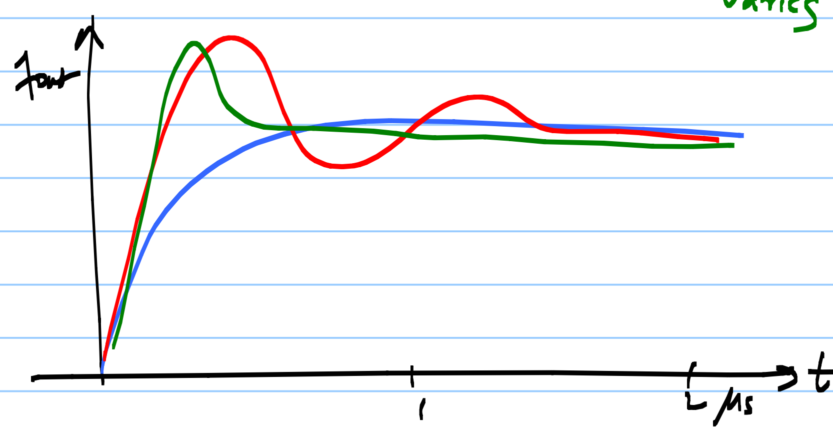
small signal loop-gain

$$L(s) = \frac{K_{vco} I_0}{N} \; \frac{\left(s + \frac{1}{RC_1}\right)}{s^2 C_2 \left(s + \frac{1}{R \, C_1 \| C_2}\right)}$$

↳ $\omega_{u,loop}$ varies with K_{vco}

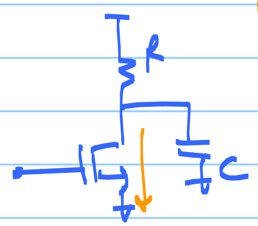
→ ω_{3dB}, ζ

↳ PM also varies

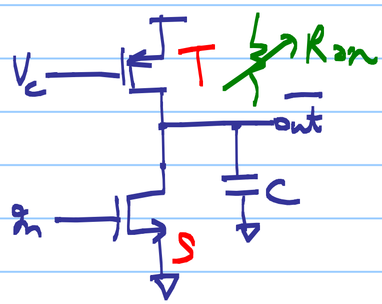


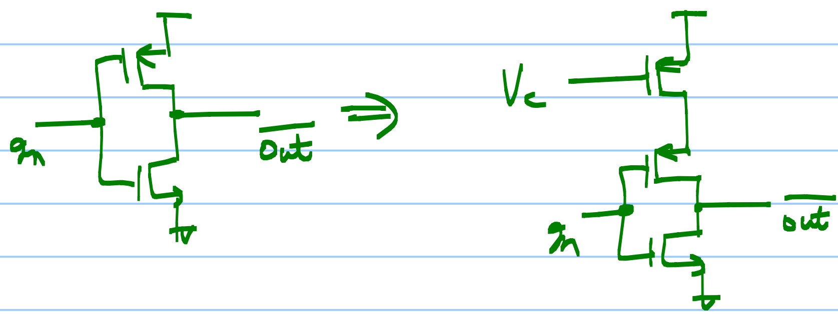
VCO Tuning

* Need a knob to control the oscillation frequency.



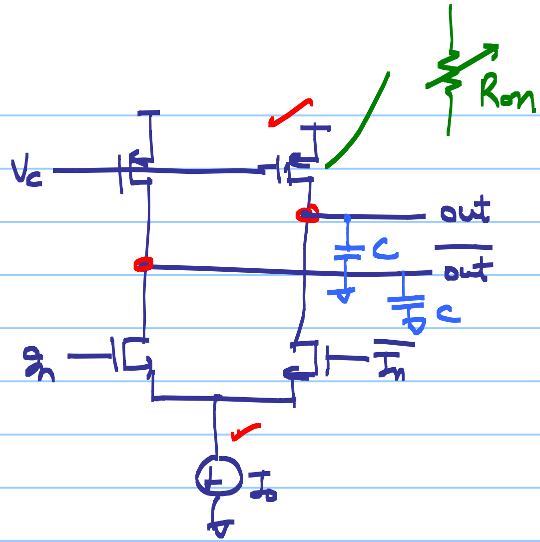
Vary R
C
I_D
V_{DD}

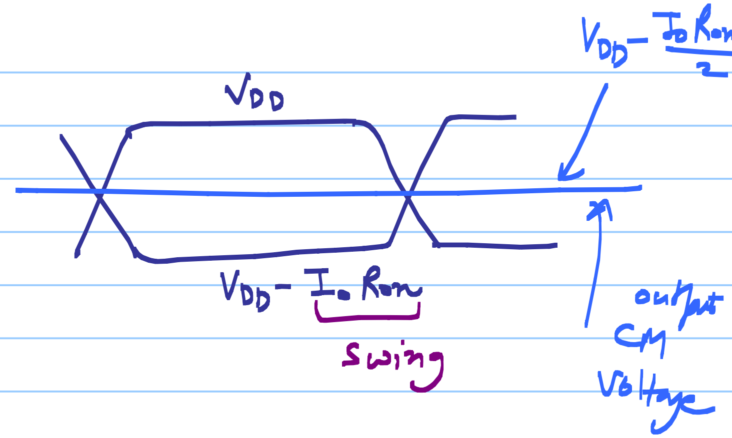




Need:

* Wide tuning range
* good linearity
* No phase noise generation





$$\tau = R_{on} C = \frac{C}{K'_n \frac{W}{L} \left(V_{DD} - V_c - |V_{THP}| \right)}$$

R_{on}^{-1} assuming deep Triode $V_{DS} << V_{DS,sat}$

$$f_{out} \propto \frac{1}{\tau} \propto \frac{K'_n \frac{W}{L} \left(V_{DD} - V_c - |V_{THP}| \right)}{C}$$

* f_{out} Varies with V_c

↳ Valid only when the load Transistors are in Triode

$$V_{DS} = I_o R_{on} = \frac{I_o}{K P_n \frac{W}{L}(V_{DD} - V_c - V_{THP})} \ll \underbrace{(V_{DD} - V_c)}_{V_{SG}} - V_{THP}$$

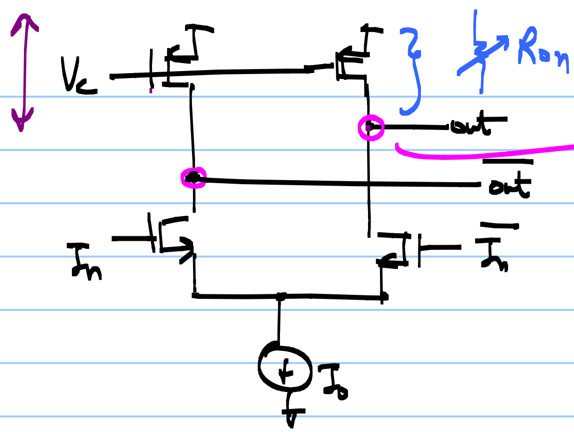
* If the above condition is not satisfied

↳ load transistors saturate

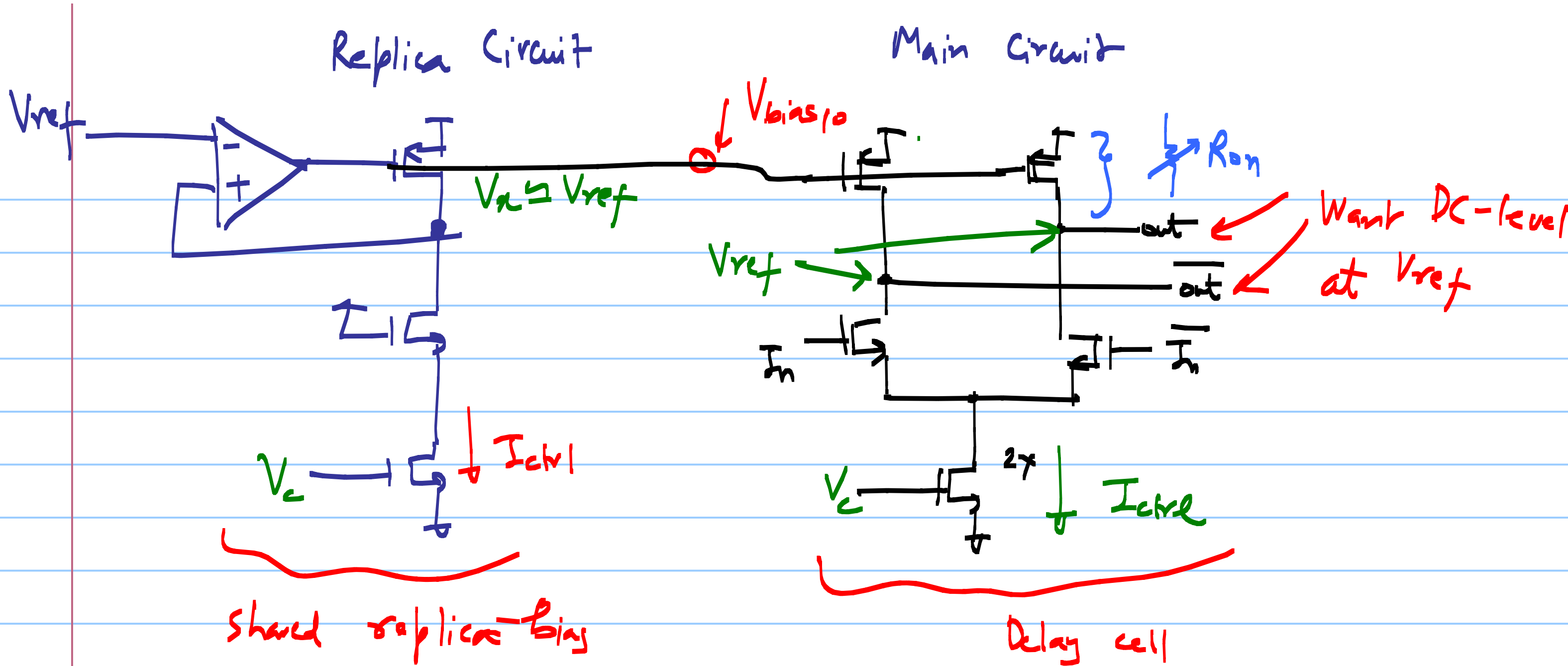
↳ VCO characteristics saturates

↳ output CM voltage is undefined

* Output swing is frequency dependent



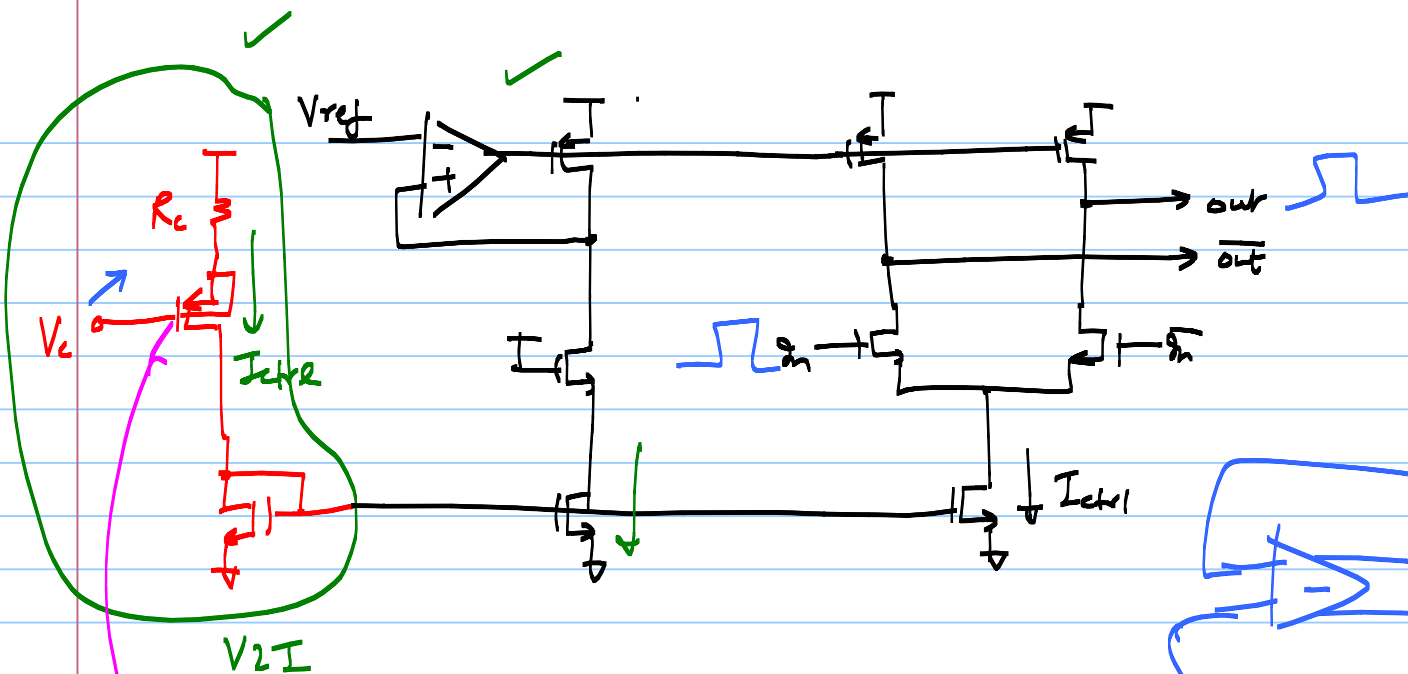
fix the output CM-level

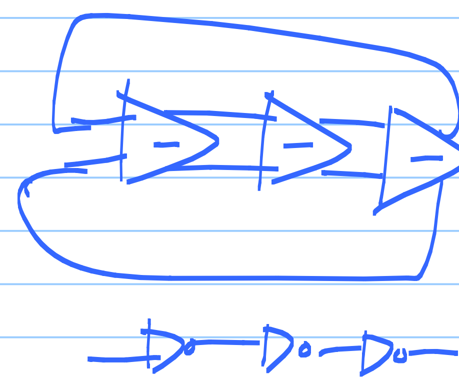


Replica bias forces $R_{on} = \dfrac{(V_{DD}-V_{ref})}{I_{ctrl}}$

$$f_{out} \propto \frac{1}{R_{on}C} \propto \frac{I_{ctrl}}{(V_{DD}-V_{ref})\,C}$$

$I_{ctrl} = f(V_c) \leftarrow$ non-linearity of the NMOS





$$f_{out} \propto \frac{-V_{ctrl}}{R_c (V_{DD} - V_{ref}) C}$$

$$g_m \gg 1/R_c$$