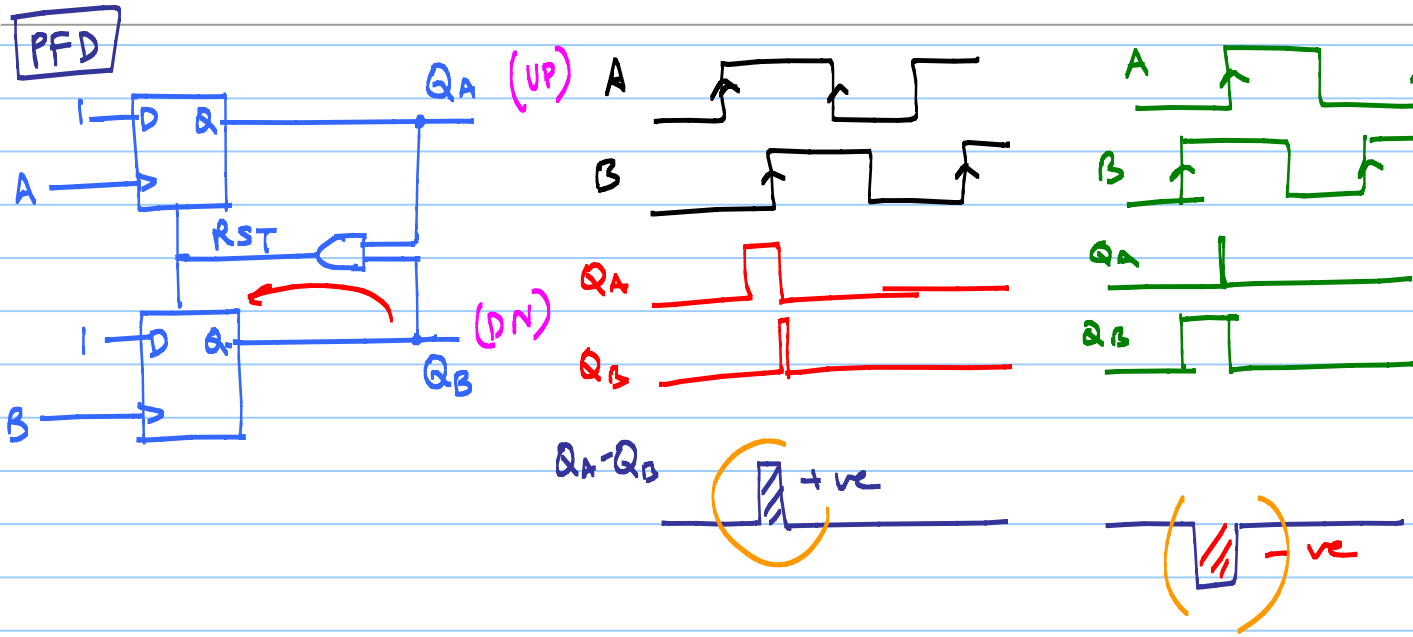
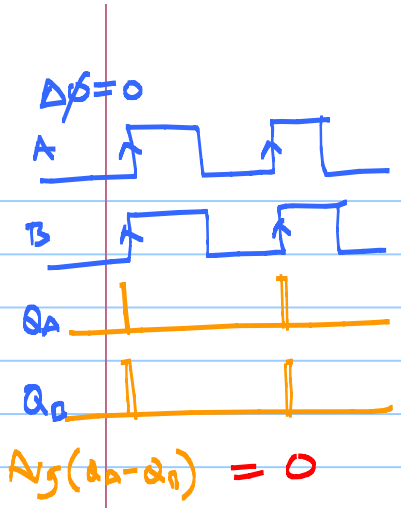
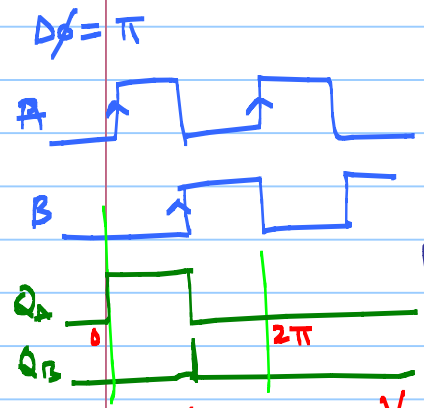
ECE 518 - Lecture 11

Note Title 2/26/2013





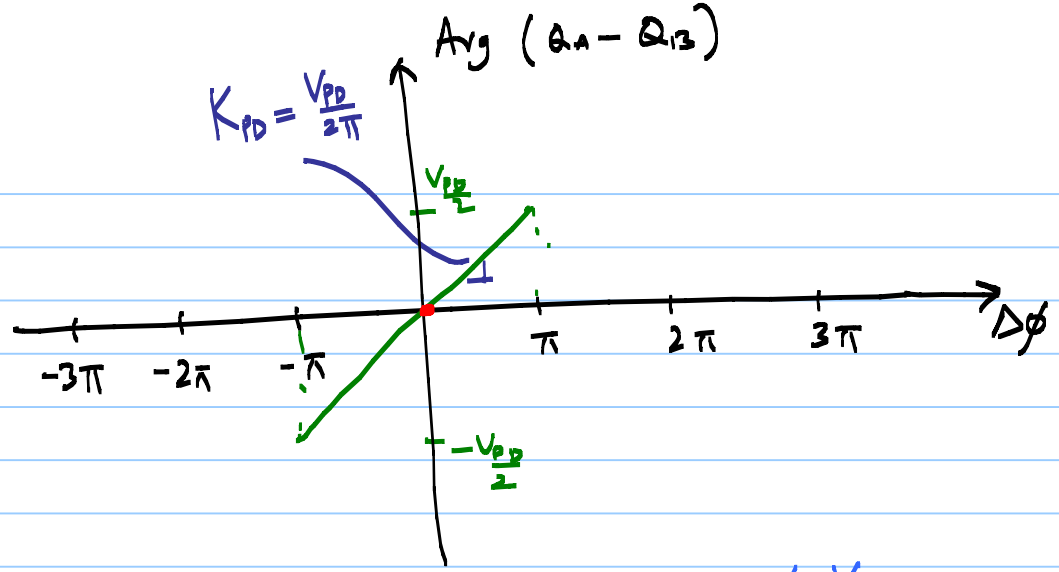
$Avg(Q_A - Q_B) = 0$



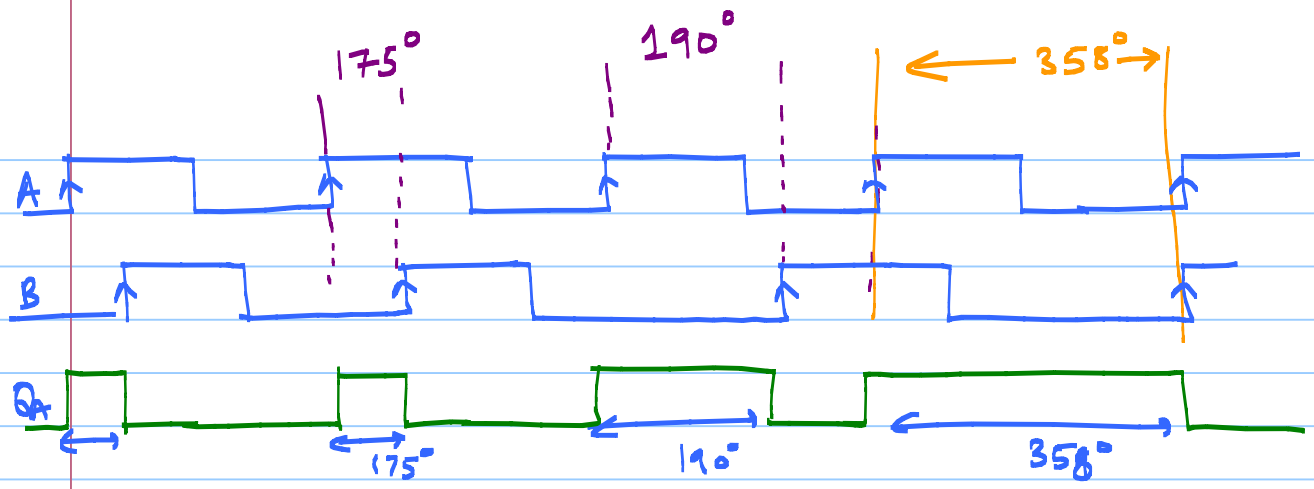
$avg(Q_A - Q_B) = +\frac{V_{PD}}{2}$

$\Delta\phi = -\pi$

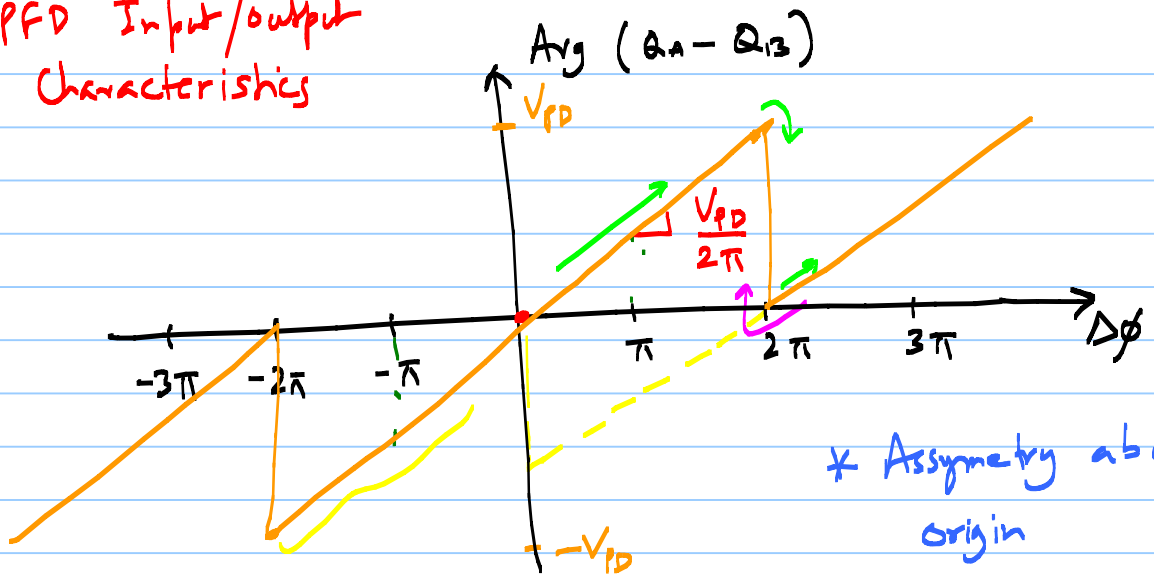
$avg(Q_A - Q_B) = -\frac{V_{PD}}{2}$



$avg(Q_A - Q_B) = \Delta\phi \cdot \frac{V_{PD}}{2\pi}$


175°
190°
358°
A
B
QA
175°
190°
358°

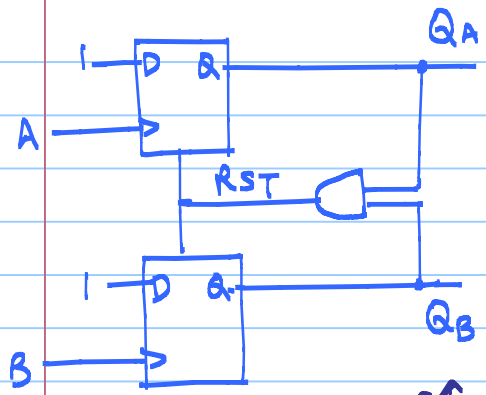
* PFD Input/output Characteristics



* Assymetry about the origin

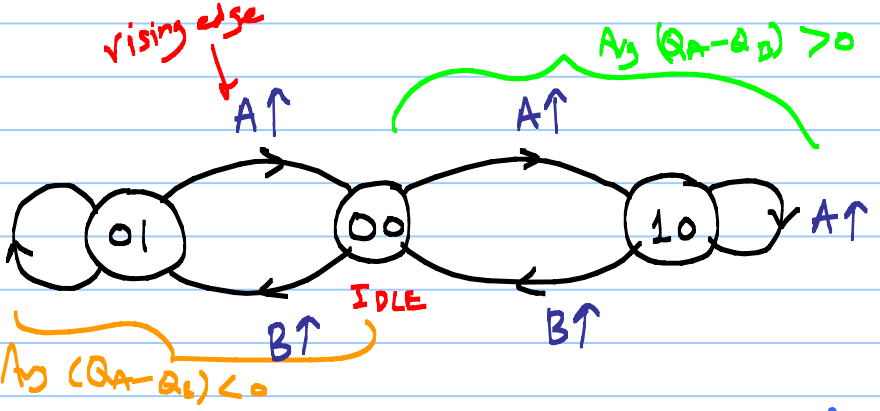
* Hysteresis

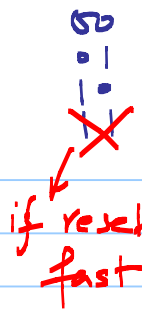
State Machine $[Q_A\ Q_B]$



Tri-state Phase Detector

↳ insensitive to duty cycle



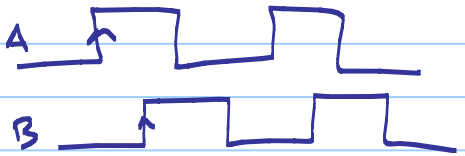


if reset is fast

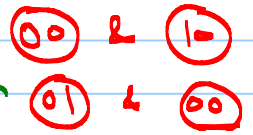
$A\uparrow \Rightarrow$ move rightwards

$B\uparrow \Rightarrow$ move leftwards

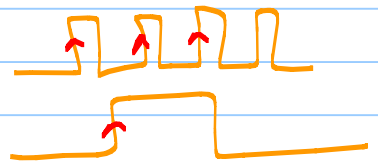
if A & B have same frequency



B leads A ←



* $f_A > f_B$
  - ↳ more A↑ than B↑
    - ⇒ PFD will circulate (00) & (10) and often between (10) to (10)



output average > 0

$\Rightarrow Avg\ (Q_A - Q_B) > 0$

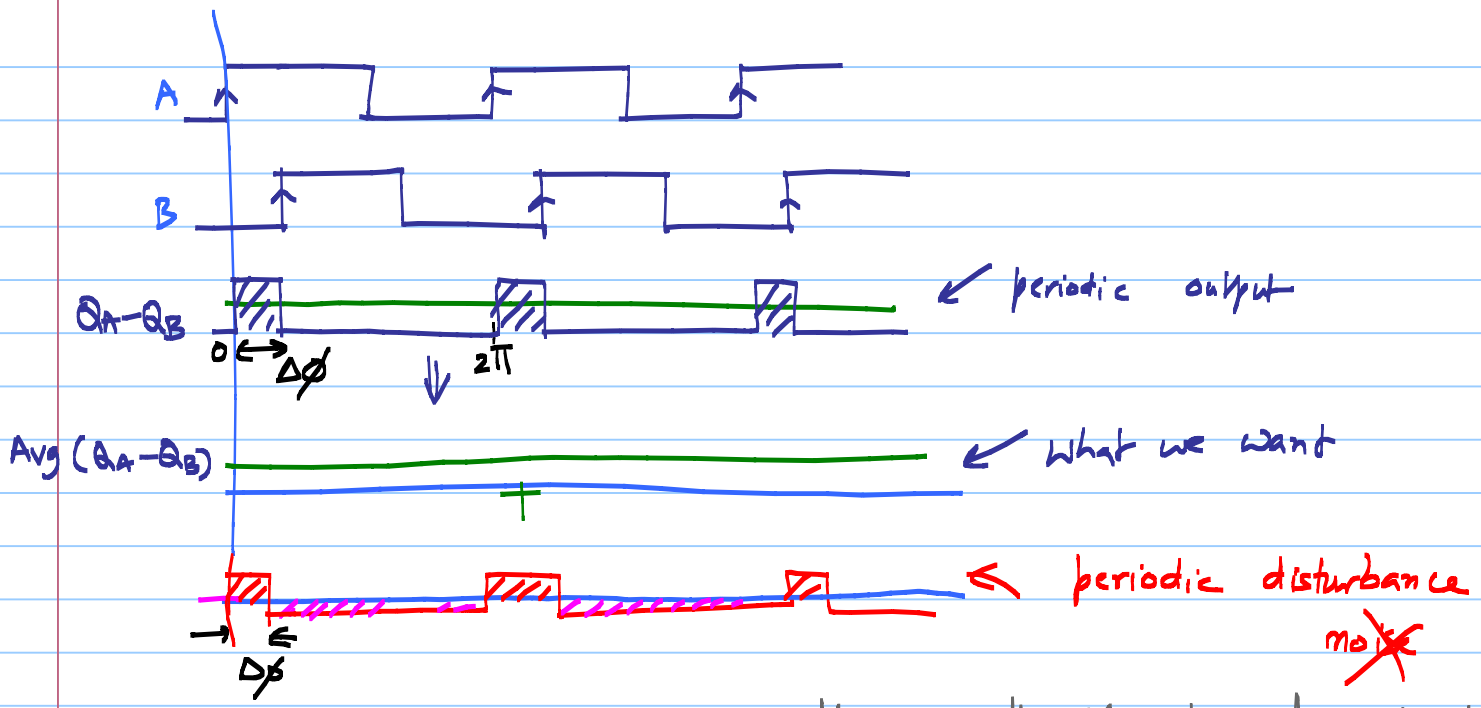
* opposite will happen for $f_A < f_B$
  - output average will be negative
* This PFD also gives frequency detection
  - * if the PLL output starts at a $f_{out} \neq f_{ref}$
    - ↳ PFD will push the PLL in one direction
* PFD is better for frequency "locking"

"PLL terminology"

Locking → for what frequency range the PLL remains locked

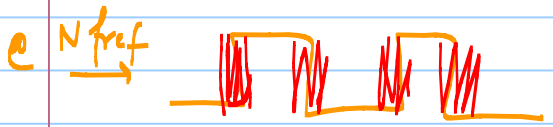
Capture → Apply some frequency and see if the PLL can lock → PFD facilitates ~ faster Capture

PFD output

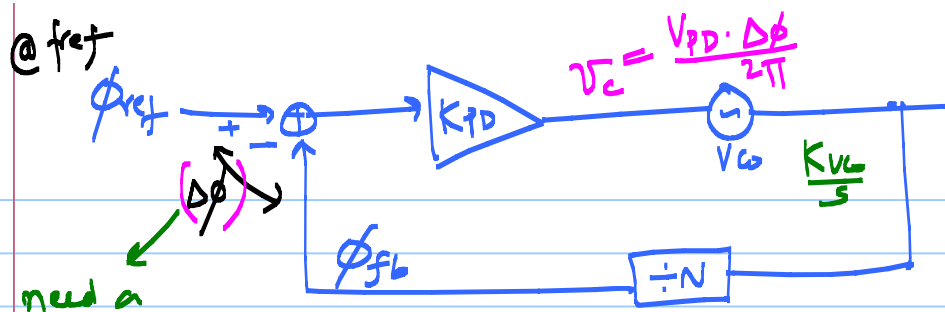


⇒ periodic disturbance ⇒ phase of the VCO is periodically disturbed

⇒ VCO's output is not periodic



@ f_{ref}



need a $|\Delta\phi| > 0$

→ periodic error

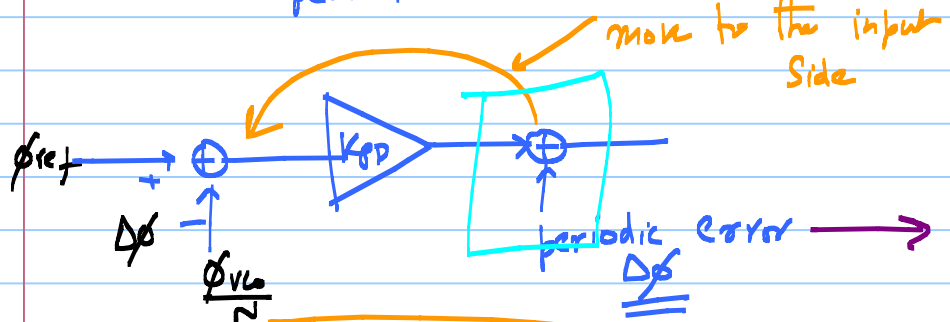
@ $f_{out} = N f_{ref}$

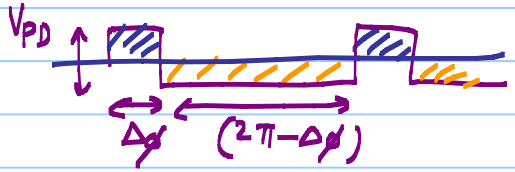
in steady-state

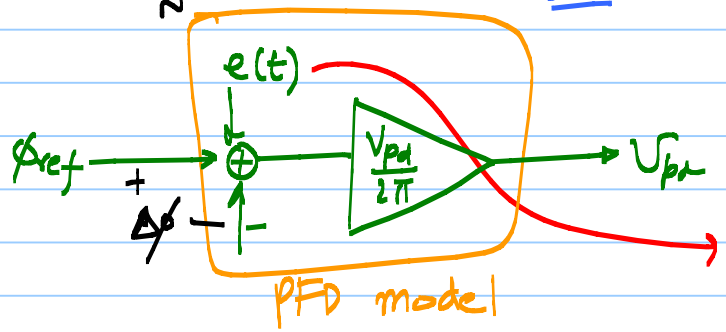
$f_{out} > f_0$

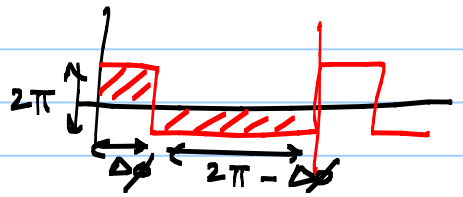
Type-I PLL

↳ # of poles at DC









Frequency content of this periodic error

↳ f_{ref}, $3f_{ref}$, $5f_{ref}$