# ECE 5/418 Memory IC Design

## Course Introduction

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# Course Outline

- **Instructor** : Vishal Saxena
- **Time** : Tue/Thu, 3:00-4:15 PM
- **Course dates** : Jan 22 – May 10, 2013.
- **Location** : ENGR 314
- **Office Hours** : Tue/Thu 4:30-5:30 PM (or by appointment)
- **Holidays** : March 26 and 28.
- **Final Exam time**: Tuesday, May 14, 2013 2:30-4:30 PM
- **Website** : http://lumerink.com/courses/ECE518/s13/ECE518.htm

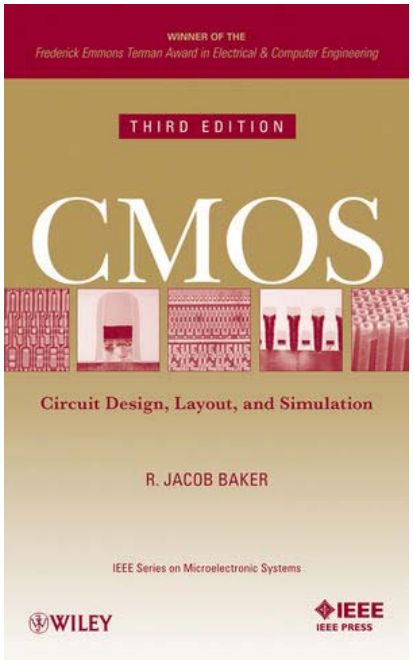
# Course Topics

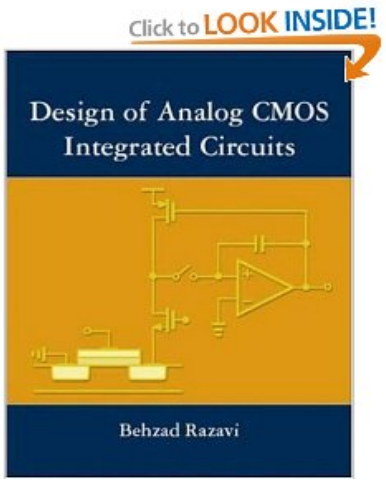
- Overview of Memory Architectures
  - ✓ DRAM, SRAM, Flash, etc.
  - ✓ Sensing and peripheral circuits
- Clock Synchronization Concepts
- Design and analysis of
  - ✓ Phase-locked Loops (**PLLs**)
  - ✓ Delay-locked Loops (**DLLs**)
- Overview of Serial I/O Links (if time permits)

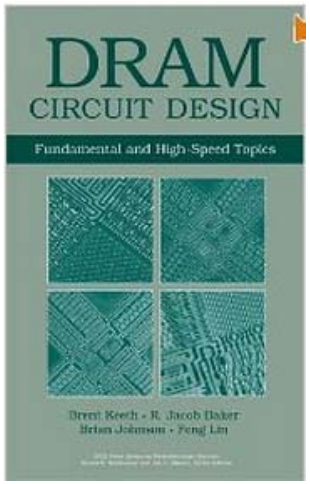
- PREREQ: ECE 5/410.

# Textbook and References

- **Textbook**: CMOS Circuit Design, Layout and Simulation – R. J. Baker, 3rd Edition, Wiley-IEEE, 2010.
- **PLL:** B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2002.
- DRAM Circuit Design: Fundamental and High-Speed Topics, B. Keeth R. J. Baker, B. Johnson, F. Lin, IEEE Press, 2007
- For detailed references and handouts see this page.



# Course Pedagogy, Grading and Policies

- Combination of lecture notes and slides
  - Lecture notes will be posted online (allow for processing delay)
  - Additional slides, Matlab code etc. will also be posted.
- Workload (Grading)
  - Homeworks (20%): Weekly assignments.
  - Midterm Exam (20%)
  - Project 1 (20%)
  - Project 2 (20%)
  - Final (20%)
- Policies
  - No late work.
  - Neither the final exam nor final project will be returned at the end of the semester.
  - No internet surfing in class on any device.
  - Plagiarism and outsourcing (!) of work is not acceptable (See BSU Policy).

# A Typical Memory Array

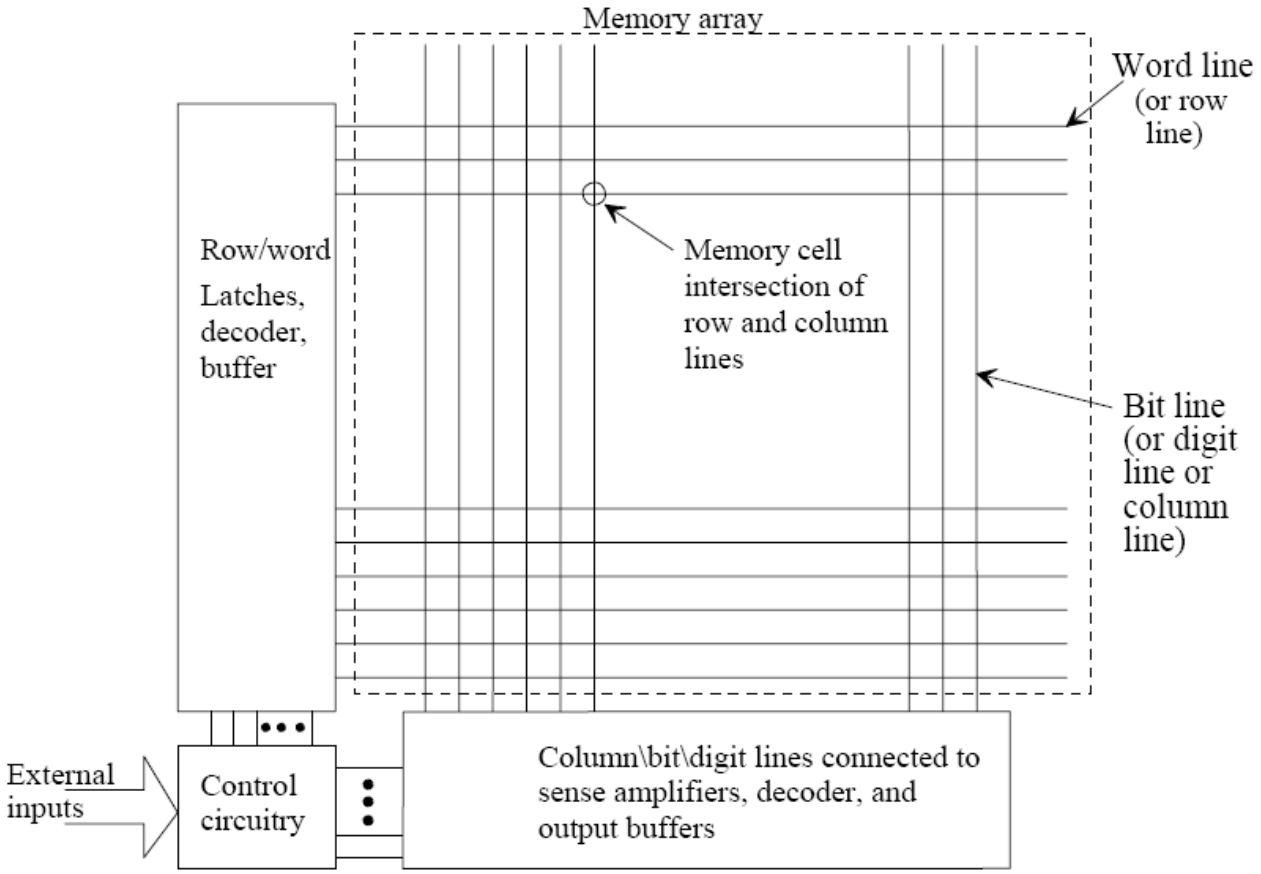



**Figure 16.1** Block diagram of random access memory.

# Open Array Architecture

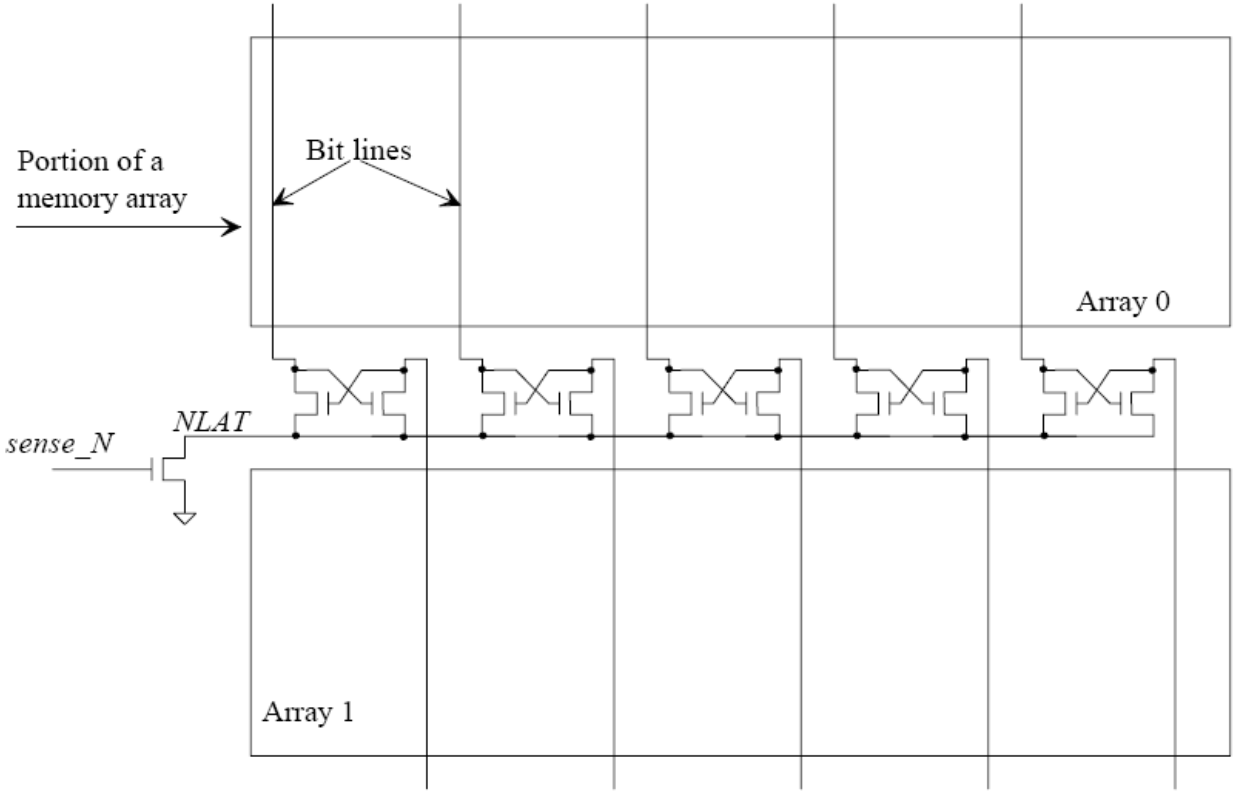



**Figure 16.6** How the NSA is placed between two memory arrays in the so-called open memory array architecture.