Project 2

ECE 5/418 – Memory/Clock Synchronization IC Design (Spring 2013)

Due on May 13, 2013.

1 Project Statement

You can choose one of the following project suggestions depending upon your interest. For all projects discussed below, you may use behavioral models for your designs, but critical components should be simulated at the transistor level.

Project #1 A DLL for DDR3 Interface (Suggested for ECE 418 Students)**:**

A delay locked loop (DLL) needs to be designed for a 200 MHz ($t_{CK} = 5\,ns$) DDR3 inteface for SDRAM. The output strobe DQS is the used to latch data lines DQ and must align with the input clock, CLK[1, 2]. The DLL should adjust the delay line (T_D) such that $t_{CK} = t_{IB} + T_D + t_{DQ}$ as shown in Fig. 1, where t_{IB} and t_{DQ} are the input and output buffer delays. Employ suitable models for the buffer delays and show DLL locking for more than one delay scenario. Ensure that the DLL recovers from false locking and stuck at min/max delay faults. Show relevant plots and characterize for power, jitter, PSRR, etc.

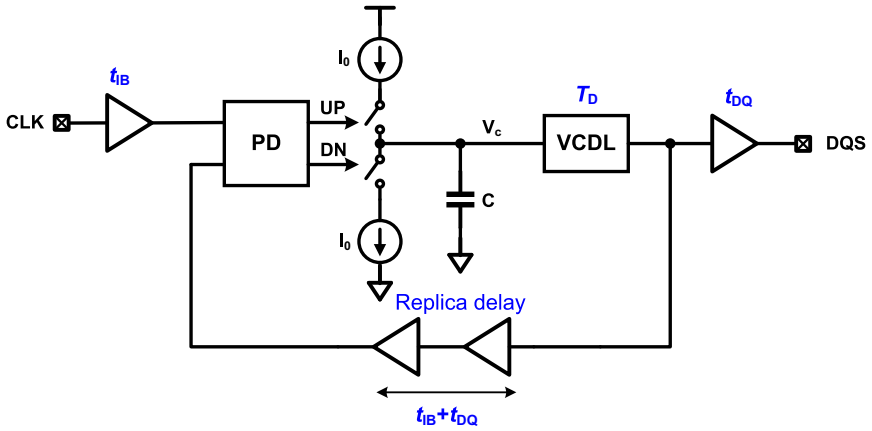

Figure 1: A DLL used in the DDR SDRAM interface.

Project #2: A Wide Tracking Range PLL

Design a split-tuned PLL, with a fixed integer divider, for use in a wide tracking range CDR[3]. The PLL should be able to generate multiphase clocks with a clock rate of 100 MHz-1 GHz. Show relevant design specifications, performance plots and characterize for power, jitter, PSRR, etc.

Project #3: Design of a Frequency Synthesizer

Design of a 2.4Ghz Frequency Synthesizer for Wireless Communications with spurs under -100 dBc. The main specifications are:

Frequency step = 6 MHz

VCO continuous tuning range > 5%
Phase noise < -110 dBc at 1 MHz offset

Project #4: 10Gb/s Clock Data Recovery (CDR) System

A CDR needs to be designed for a $10\,Gb/s$ optical interface. Your can select a sampling clock frequency between 1.25GHz – 10GHz. Compare Linear and Bang-Bang PD- based architectures, and explore dual-loop and phase-interpolation[4, 3] architectures. Comment on the phase resolution and frequency tracking range of the selected architecture. The CDR should be compliant with OC-192 mask.

Project #5: On-chip Clock generator for a High-Speed ADC

Design a clock generator for a High-Speed $\Delta\Sigma$ ADC. The main specifications are:
Frequency = 1 GHz
Jitter < 1 psec
Spurs under -90 dBc
Minimize power consumption
Load impedance = 2.5 pF

Project #6: An All-Digital PLL with DCO

Design an All-digital PLL employing a TDC and DCO-based architecture and try to meet the specifications for project #3.

Any other project suggestion is welcome.

2 Grading Scheme

Progress Report 10%

Literature Survey 25%

Functionality and performance 25%

Design characterization and presentation of results 20%

Report presentation and clarity 20%

Novelty (Bonus) 10%

References

[1] Keeth, B., Baker, R. J., Johnson, B., and Lin, F., “DRAM Circuit Design: Fundamental and High-Speed Topics,” Wiley-IEEE Press, 2008.

[2] E. Booth, MS Thesis, “Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator.” Available: [Online]

[3] P. Hanumolu, G.-Y. Wei, U.-K. Moon, “A Wide-Tracking Range Clock and Data Recovery Circuit,” IEEE JSSC, vol. 43, no. 2, Feb. 2008.

[4] Hsieh, Ming-ta, and G. Sobelman. "Architectures for multi-gigabit wire-linked clock and data recovery." Circuits and Systems Magazine, IEEE 8, no. 4 (2008): 45-57.

[5] Staszewski, Robert Bogdan, et al. "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS." Solid-State Circuits, IEEE Journal of 39.12 (2004): 2278-2291.