Project 1

ECE 5/418 – Memory/Clock Synchronization IC Design (Spring 2013)

Final report due on Thursday, April 11, 2013.

1 Problem Statement

A generic memory interface requires generation of a wide range of clock frequencies from a low-frequency stable clock reference, e.g. a crystal oscillator. The goal of this project is to design a complete phase-locked circuit operating over a wide output frequency range with a low frequency reference clock, while minimizing the overall power consumption. The target specifications for the PLL are as follows:

Table 1: PLL design specifications

Parameter	**Specified Value**
Technology	TSMC 180nm CMOS
Supply voltage, V_{DD}	1.8 V
Operating frequency (f_{out})	100 MHz fixed (*for ECE 418 students*)
	100 MHz - 500 MHz (*for ECE 518 students*)
Fixed feedback divider (N)	16
Total capacitance used	Minimum
Power consumption	Minimum
Figure of Merit	Power × Total capacitance [mW×pF]
Absolute rms jitter *Bonus points, required for research students*	0.2% of the period

Design Expectation: A typical PLL design requires trade-off between phase-noise/jitter performance and power consumption to ascertain the PLL loop-bandwidth. Research students in the class are expected to consider these specifications in their design (discuss with the instructor). However, for other students PLL design for jitter specification is optional with bonus points.

2 Progress Report

One page progress report (10% of the grade) is due on April 2, 2013. The report should briefly discuss your design approach, calculations, critical blocks to be designed, and at least behavioral level simulation results. You should also mention your plans to accomplish the project goal by the deadline.

3 Final Report Guidelines

The report should explain the design considerations made with relevant calculations and well labeled plots, and should not exceed 5 pages (use two-column IEEE format[3]). Use Lyx or MS Word to type-set your report and *submit it electronically.*

1. The first page should provide an overall description of the PLL architecture with an emphasis on system-level trade-offs and the design choices you made to decide upon the chosen architecture. Using behavioral simulation of the PLL, clearly explain how you chose the PLL loop bandwidth and phase margin to optimize the performance and power. Tabulate all the component values and appropriate simulated gain of each of the blocks and show the total PLL power. Draw a pie-chart for the power dissipation for each of the blocks.

2. Pages 2-4 should elaborate on the design of the individual blocks of the PLL. Show clearly drawn schematics[4], simulated waveforms, transfer functions, and relevant analysis for each of the blocks. Emphasize the design trade-offs and focus on the design choices made.

3. On the last page, summarize your work along with conclusions drawn from your experience. Do not forget to have a references section quoting all the work you used from the literature.

4. ***Bonus points*** *(required for research students):* A plot indicating the noise contribution of all the blocks and the overall noise performance of the PLL to illustrate your design choices.

4 Grading Scheme

Progress Report 10%

Design choices and justification 25%

Functionality and performance 25%

Design characterization and presentation of results 20%

Report presentation and clarity 20%

Novelty and Jitter Characterization (Bonus) 20%

References

[1] M. Perott, "Integer N Frequency Synthesizers," Tutorial [Online].

[2] K. Kundert, "Predicting the phase noise and jitter of PLL-based frequency synthesizers," Whitepaper [Online].

[3] IEEE Transactions Templates. Available [Online].

[4] Visio Schematic Symbols. Available [Online].