Homework 7

ECE 5/418 – Memory/Clock Synchronization IC Design (Spring 2013)

Due on Tuesday, Mar 18, 2013.

Note: Use Cadence schematic capture and Spectre simulation tools, available on the AMS servers for the homework problems. Use TSMC 180nm models with $V_{DD} = 1.8\,V$.

Problem 1- Type-II PLL Design

A Type-II charge-pump PLL needs to be designed to generate $f_{out} = 500\,MHz$ clock frequency from a $f_{ref} = 50\,MHz$ reference. Assume that the VCO has a free running frequency of $f_{c_0} = 400\,MHz$ and a linearized gain $K_{VCO} = 300\,\frac{MHz}{V}$ around the input bias point of $V_c = 0.9\,V$.

1. Select a loop bandwidth ($\omega_{u,loop} < \frac{\omega_{ref}}{10}$). Give at least two reasons for this design constraint.
2. Design the loop for a 60° phase margin. What are the closed-loop natural frequency (ω_n) and damping factor (ζ) for this design?
3. Sketch incremental phase domain model of the PLL. Plot open- and closed-loop frequency responses as well as the transient step response and properly label them.
4. Choose appropriate values for the charge-pump current (I_0) and the loop-filter components? Sketch circuit-level schematic for the PLL.
5. Using a behavioral model[1], perform transient simulation of the PLL and demonstrate locking (plot the VCO control voltage, v_c, and the VCO frequency, f_{VCO}). Does the transient settling behavior of the PLL correspond to the results in part 3? Explain.
6. In part 5, apply a frequency step of $\delta f = 1\,MHz$ and show PLL locking. Comment on the settling response.

Bonus points: Plot spectrum (using FFT) of the VCO output in the steady-state. Study the PLL settling response for different phase margin values (45°and 72°).

[1]Add the following line entry to your cds.lib and look at the example schematic PLL1. Make a local copy of the library before starting your work.
DEFINE PLL_Design /home/vsaxena/ece510/PLL_Design