Homework 5

ECE 5/418 – Memory/Clock Synchronization IC Design (Spring 2013)

Due on Tuesday, Mar 4, 2013.

Note: Use Cadence schematic capture and Spectre simulation tools, available on the AMS servers for the homework problems. Use TSMC 180nm models with $V_{DD} = 1.8\,V$.

Problem 1- Phase Detector Characterization

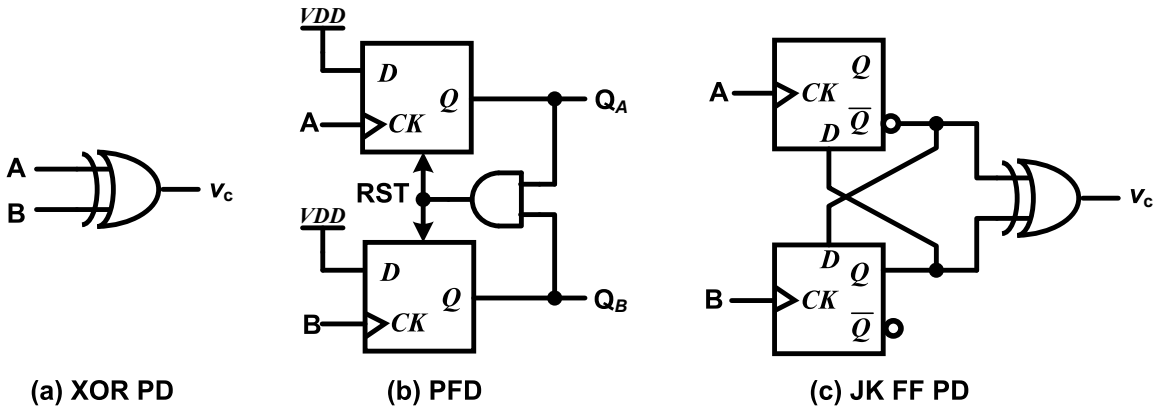

Figure 1: Phase detector topologies

Consider the phase detector topologies shown in figure 1 (XOR PD, PFD and JK Flip-Flop PD).

1. Hand-sketch the input/output characteristics of all the three PDs. Find the phase detector gain at the nominal lock point. The x-axis should be the phase difference ($\Delta\phi = \phi_A - \phi_B$) and the y-axis should be the average value of the output v_c. *Appropriately label the plot*s.

2. Use test setup shown in the figure 2 with $f_{ref} = f_{fb}$. Use CMOS level square wave clocks (say 100 MHz) with finite rise and fall times.

   (a) Plot the phase detector transfer characteristics over a phase range of $\pm 4\pi$, with sufficient phase points per curve. Use the macromodels (use and/or modify the Verilog-A behavioral models in the bmslib (or ahdlLib)[1] libraries) to generate the PD transfer curves. However, if you prefer to implement the circuits at the transistor level, feel free to do so.
   Hint: *Setup a transient simulation with an initial delay between the clocks mapped to the $\Delta\phi$ parameter, and then calculate the average PFD output using the Spectre calculator. Sweep the $\Delta\phi$ parameter using parametric analysis to obtain the desired plots.*

   (b) What is the impact of clock duty cycle on each of the PDs?

[1] Add the following line entries to your cds.lib
DEFINE bmslib $CDS610/tools/dfII/samples/artist/bmslib
DEFINE ahdlLib $CDS610/tools/dfII/samples/artist/ahdlLib

3. For the phase detectors, find the average output with $f_{fb} = 0.5$, 0.75, 1.5, *and* $2 \cdot f_{ref}$ (x-axis of the plot is f_{fb}). Assume an initial phase difference of 0°. What do these plots imply regarding the utility of these circuits as a frequency detector?

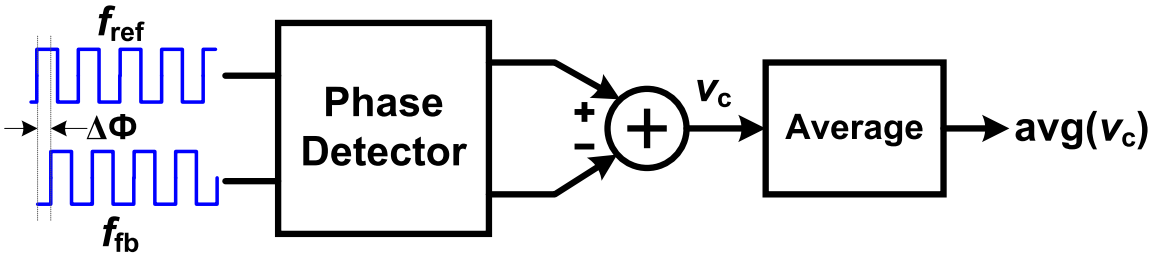

Figure 2: PD chacterization test-bench.