Homework 3

ECE 5/418 – Memory IC Design (Spring 2013)

Due on Tuesday, Feb 19, 2013.

Note: Use Cadence schematic capture and Spectre simulation tools, available on the AMS servers for the homework problems.

Problem 1: An SRAM array has 256 cells in a column, i.e. connected to a single bitline pair.

1. Using the 180nm CMOS process ($V_{DD} = 1.8V$), design a 6T SRAM cell. Discuss your transistor sizing considerations.
2. Using simulations, demonstrate read and write operations in a single SRAM cell (for both '0' and '1'). Estimate the bitline load and model it using lumped capacitors. Discuss sizing for the bitline precharge circuit and the write driver. Use ideal pulse sources for your simulations.
3. Generate the butterfly curves for the SRAM cell and estimate the static noise margin for read and write operation (this may need some thinking).
4. Repeat part (3) if the bitlines are charged to $V_{DD}/2$ before the reads. Explain your observations.
5. Design a sense-amp to speed up the read operation so that the SRAM can be read within 10 ns.
6. What is the minimum supply voltage (V_{DD}) at which the cell can be reliably read and written.

Problem 2: Do problem **16.19** at the end of the chapter in the CMOS textbook. Do a literature search and discuss the operation of other sense amplifier topologies found in NAND Flash memory.