Homework 2

ECE 5/418 – Memory IC Design (Spring 2013)

Due on Tuesday, Feb 12, 2013.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems. Use TSMC 0.18μm CMOS models for your designs.

Problem 1: Discuss, in detail, the (likely) layout of the arrays (blocks, sub-array size, page size, etc.) for the Micron 1Gb DDR3 SDRAM (datasheet). Make sure you provide details like number of I/O lines below the array and how you know this (page size and array size).

Problem 2: Row decoder/driver design

1. Design a local decoder using precharge-evaluate (PE) logic to decode a **4-bit** row address. The logic equation is given by $DEC = \bar{A_3} A_2 \bar{A_1} A_0$. Use keeper PMOS device to avoid the output from leaking away. Show simulation results.
2. Design a row driver circuit to drive the decoded wordline to a suitable pumped voltage of $V_{DDP} \geq V_{DD} + V_{THN_{body-effect}}$. Use an ideal source for V_{DDP} (i.e. don't design a charge pump). Model the wordline as an RC transmission line with 512 columns. Assume that each access transistor has 1Ω resistance across its gate and a capacitance, to ground, of $5\,fF$. Estimate and simulate the delay in completely opening the wordline. Show relevant plots and label them.