Homework 1

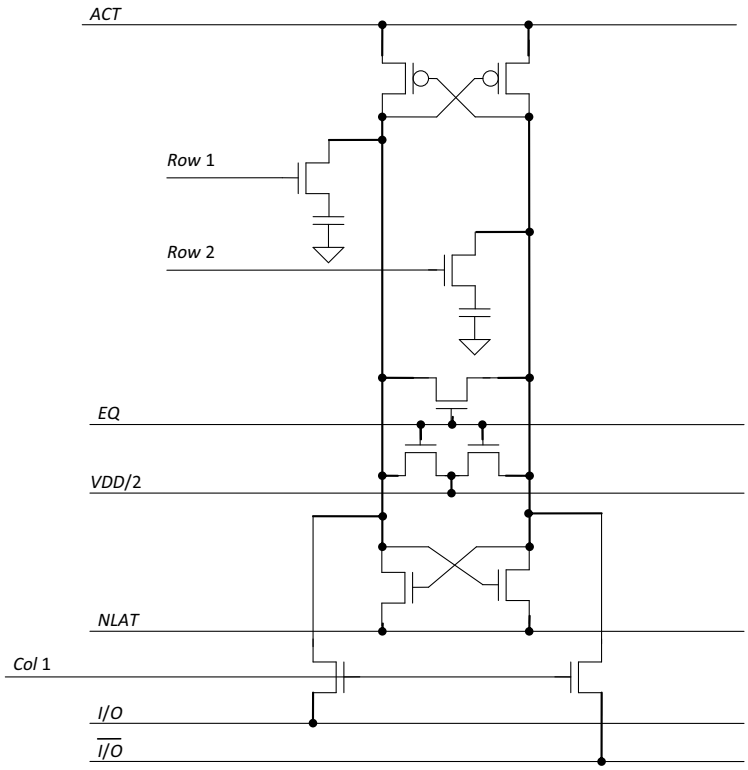
ECE 5/418 – Memory IC Design (Spring 2013)

Due on Tuesday, Feb 5, 2013.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problem 1: Estimate the bitline capacitance if the length of the column line is 40 μm, the depletion capacitance associated with an NMOS S/D to substrate is 100 aF, and the capacitance from a single column line to the 256 wordlines in the array is 200 aF. What considerations limit the number of wordlines and bitlines in a DRAM array?

Problem 2: This problem is concerned with simulating the operation of the DRAM sense (read) and write circuitry. Consider the section of a DRAM seen below. Make sure your schematics and simulation results are extremely clear and well labeled. Use $C_{mbit} = 20\,fF$ for the Mbit capacitors, $C_{BL} = 100\,fF$ for the bitline capacitance, and $C_{IO} = 200\,fF$ for the I/O line capacitances. Use the TSMC 180nm CMOS models for your designs. Use appropriate sizes for the access transistor (minimum area), the sense-amps and the I/O devices.



1. Suppose both DRAM cells contain logic zeroes. Starting with all decoder outputs at ground (that is, Row1, Row2, and Col1 are at 0 V), EQ high, NLAT floating (n_sense at ground), ACT floating (p_sense at VDD) use simulations to show how you would read out the contents in the cell associated with Row2. Show how the cell is refreshed and how the I/O lines change values. Make sure your simulation output plots are labeled (e.g. EQ shuts off, row goes to

VDD, NSA fires, etc.) Use appropriate pulse sources for the signals Col1, Row1, Row2, EQ, n-sense, p-sense. Show the waveforms when the cells contain logic ones.

2. Show how you would write a logic one to the cell on Row 2. Use pulse sources to drive the I/O lines. Your outputs should show how the sense amplifiers help regenerate full logic levels on the bitlines (to compensate for the threshold drop through the I/O devices). Note that if your I/O transistors aren't wide enough you will not be able to switch the sense amplifiers when they are on (NLAT at ground and ACT at VDD).

3. Finally, design another sense amplifier for the I/O lines. When doing a read we know that the largest voltage we can pass through the I/O lines is $V_{DD} - V_{THN}$. Use a separate equilibrate signal for your sense amplifier. Precharge the I/O lines to $V_{DD}/2$. Don't forget the 200 fF of parasitic capacitance hanging on the I/O lines. Make sure you comment on your choices (pros and cons).