ECE518 Memory/Clock Synchronization IC Design

Voltage Controlled Oscillators

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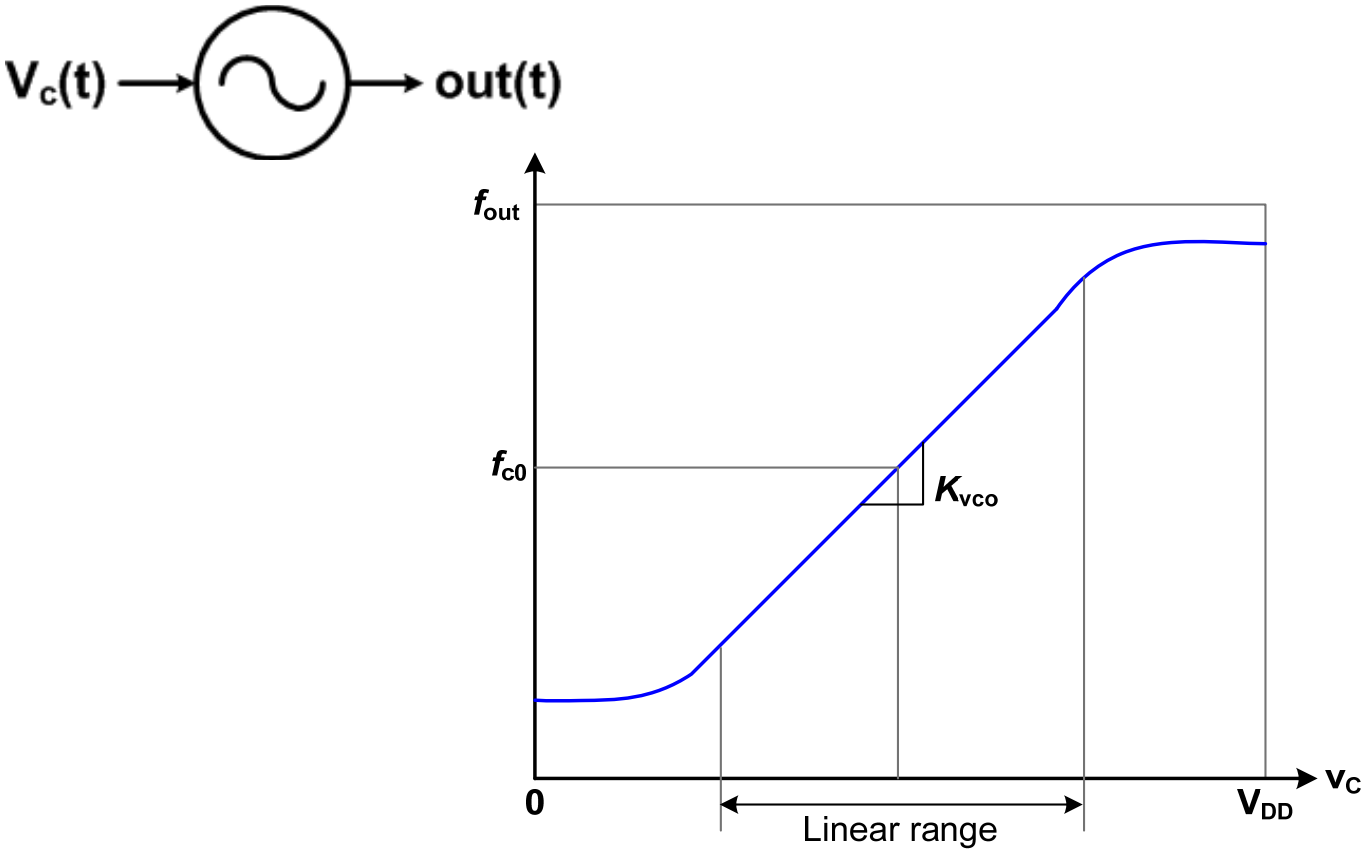
Voltage-Controlled Oscillator

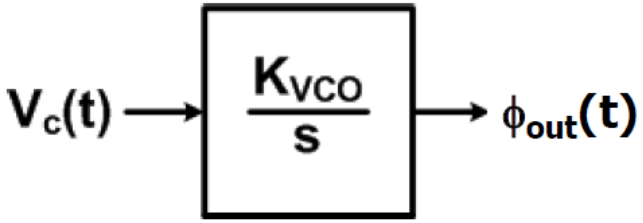


- $f_{out} = f_{c0} + K_{VCO} \cdot v_c(t)$

Voltage-Controlled Oscillator

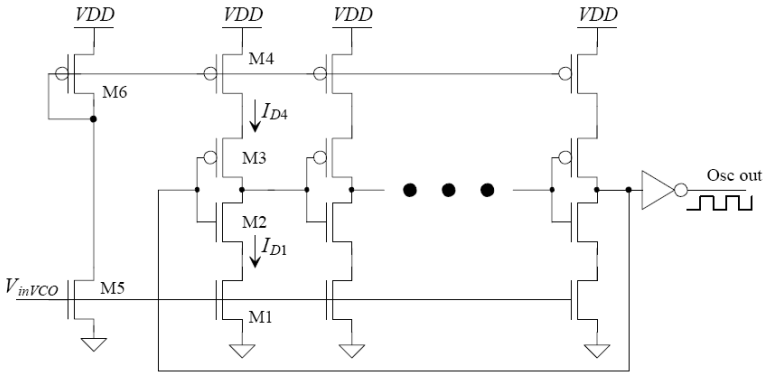
- Incremental phase-domain relationship
  - $\Phi_{out}(t) = 2\pi K_{VCO} \int v_c(t) dt$
  - $\Phi_{out}(s) = (2\pi K_{VCO}/s) V_c(s)$

Laplace Domain Model

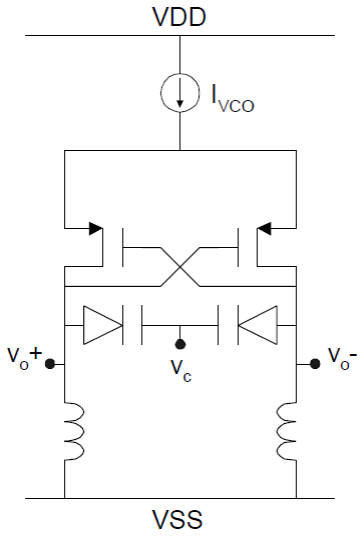


VCO Types

- Ring Oscillator VCOs
  - Easy CMOS integration
  - Wide tuning range (3-5X)
  - Poor phase noise performance



- LC Oscillator VCOs
  - Large area (on-chip inductors)
  - Narrow tuning range (20-30%)
  - Good phase noise performance
  - Higher design and characterization effort



Ring Oscillator VCOs

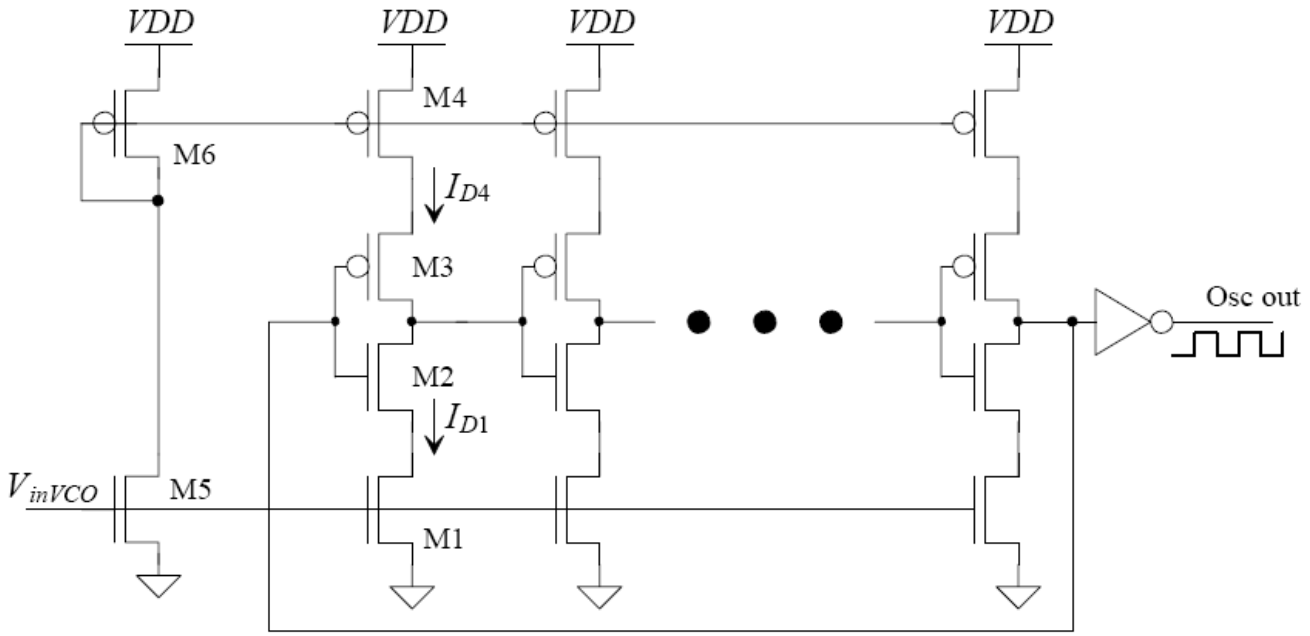
- VCO usually consists of two parts
  - Controlled voltage to current (V2I) circuit
  - Current-controlled ring oscillator (CCO)

- Can be single-ended or differential
  - Differential design allows for even number of oscillator stages if diff-amps used for delay cells

VCO Design Concerns

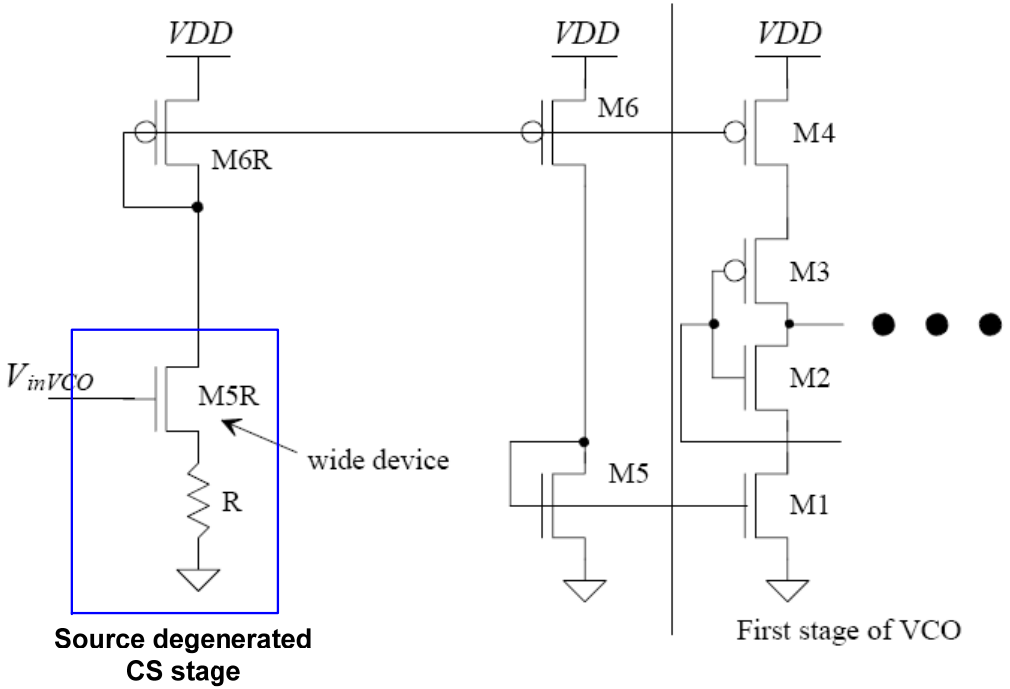
- Large frequency range to cover PVT variations
  - 3-5X typical
- Single-ended or differential?
  - Use differential for 50% duty cycle
- VCO gain (K_{VCO}) affects loop stability
  - Better to have moderate K_{VCO} over large tuning range
- More delay stages -> easier to initiate oscillation
  - DC gain >2 for 3 stages
  - DC gain > $\sqrt{2}$ for 4 stages

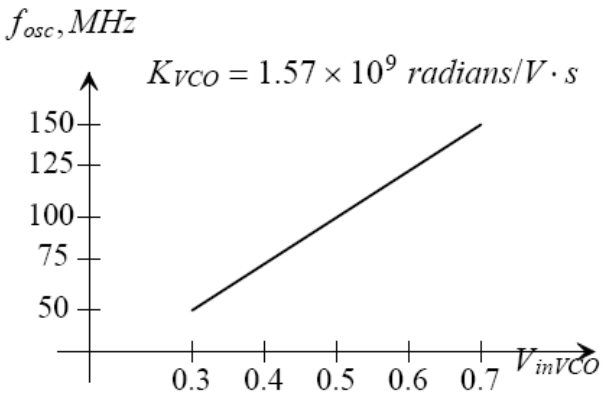
Current-Controlled Oscillator (CCO)



- Control the bias current in the inverting stages to control the delay and hence the frequency of oscillation

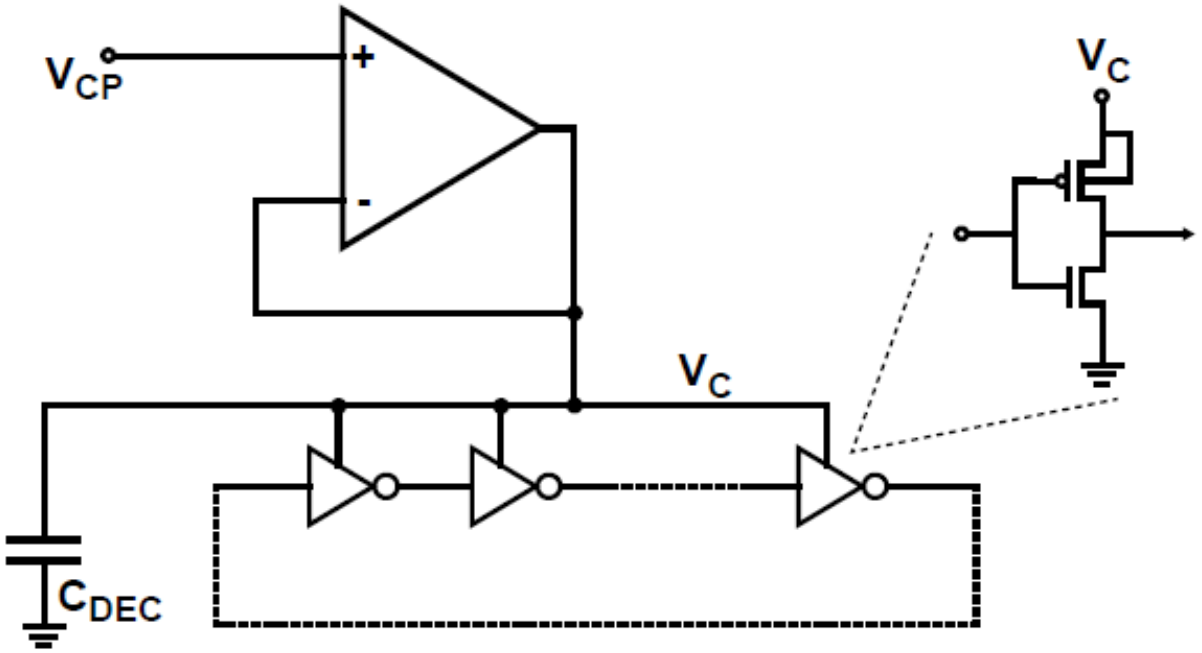
Linearized CCO





- Use a source degenerated CS stage as a linear voltage to current (V2I) converter

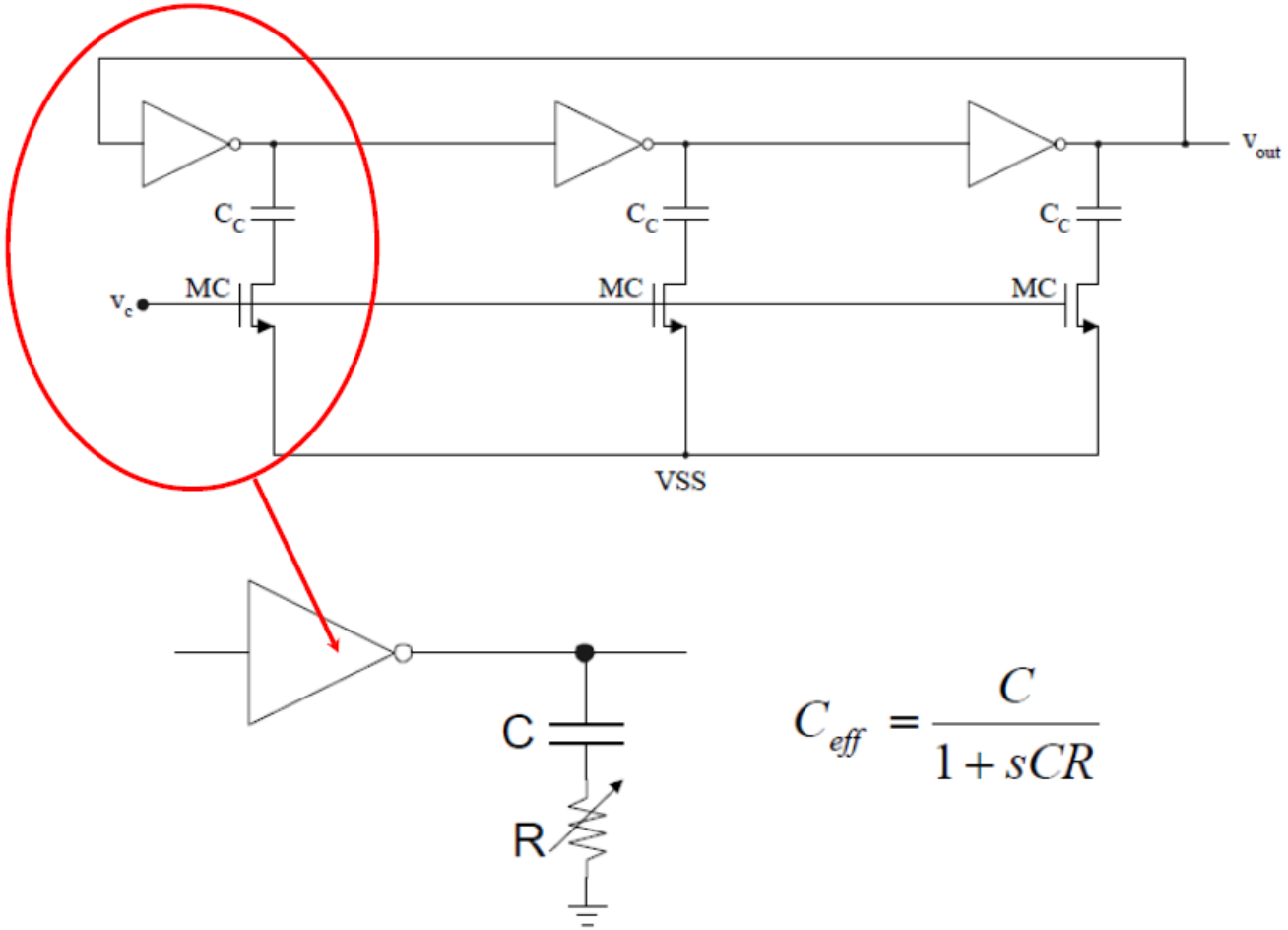
Supply-Tuned Ring Oscillator



$$T_{VCO} = 2nT_D \approx \frac{2nC_{stage}}{\beta(V_c - V_{th})}$$

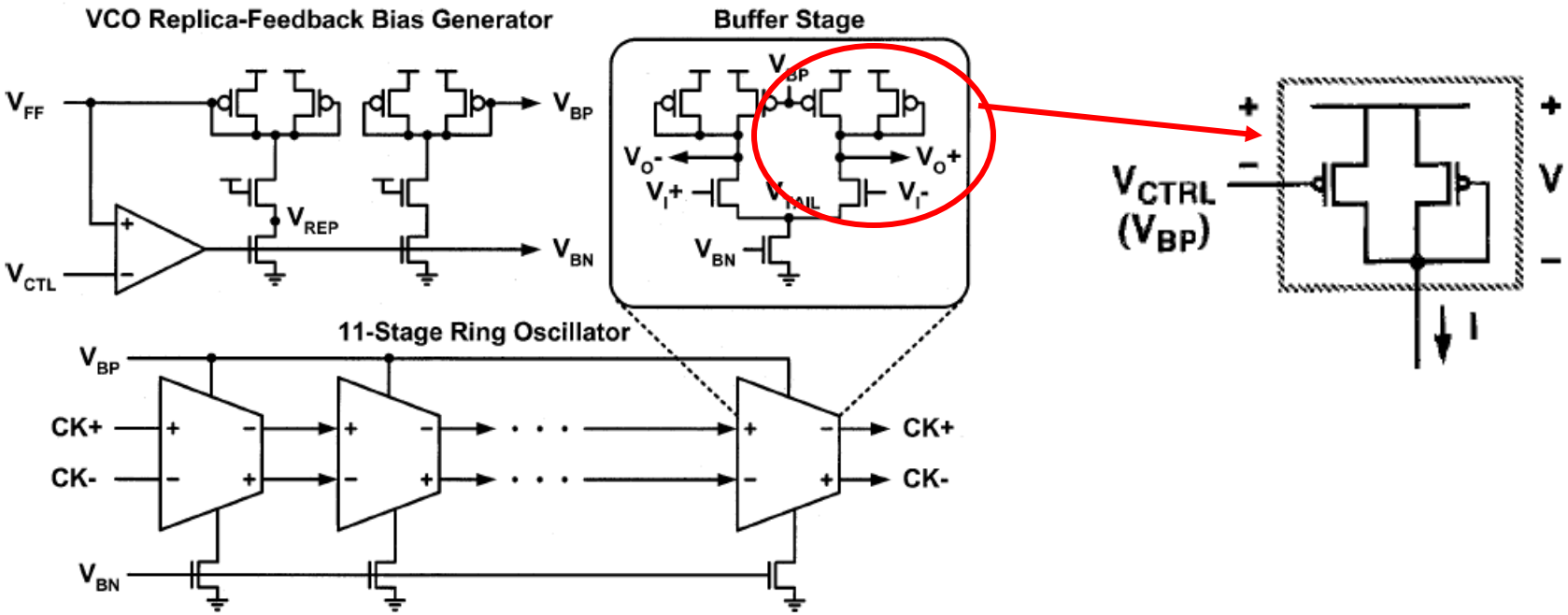
$$K_{VCO} = \frac{\partial f_{VCO}}{\partial V_c} = \frac{\beta}{2nC_{stage}}$$

Capacitive-Tuned Ring Oscillator



$$C_{eff} = \frac{C}{1 + sCR}$$

Symmetric Load Ring Oscillator



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Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques

John G. Maneatis

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 11, NOVEMBER 2003 1795

Self-Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL

John G. Maneatis, *Member, IEEE*, Jaeha Kim, *Student Member, IEEE*, Iain McClatchie, Jay Maxey, and Manjusha Shankaradas

Current Controlled Oscillator (CCO)

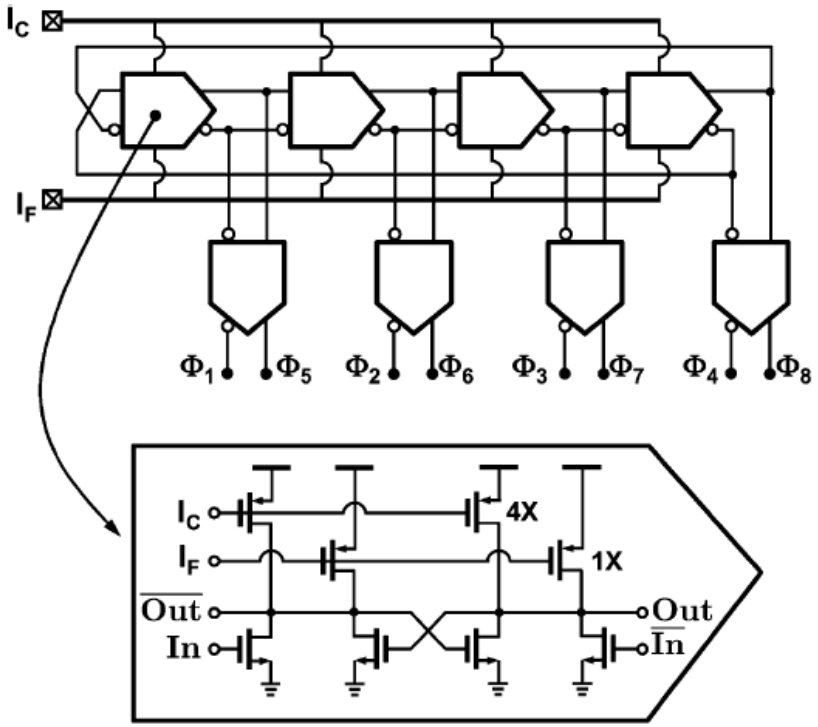


Fig. 22. Split-tuned current controlled oscillator.

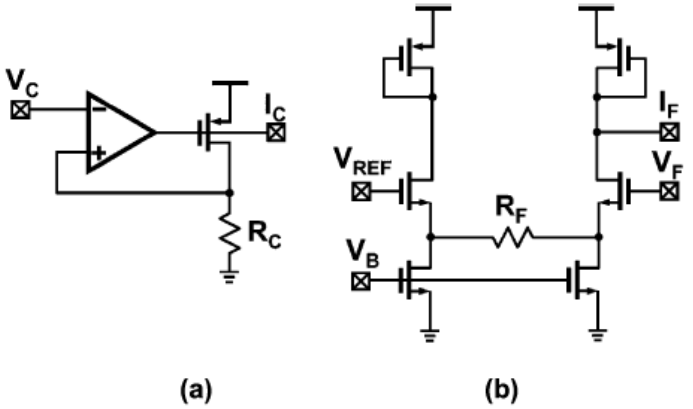
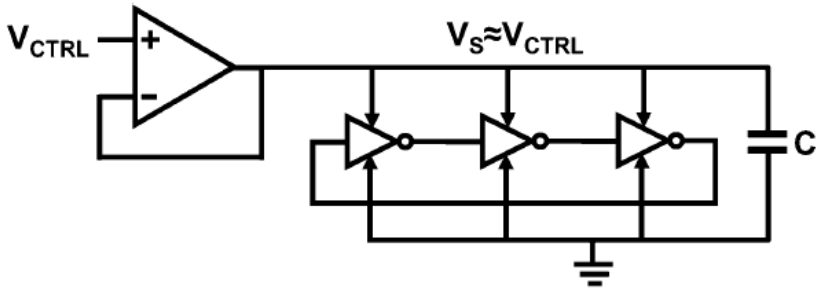


Fig. 20. V2I circuits. (a) Coarse V2I. (b) Fine V2I.

A Wide-Tracking Range Clock and Data Recovery Circuit

Pavan Kumar Hanumolu, *Member, IEEE*, Gu-Yeon Wei, *Member, IEEE*, and Un-Ku Moon, *Senior Member, IEEE*

Differential Supply Regulated VCO



. Supply regulated tuning concept.

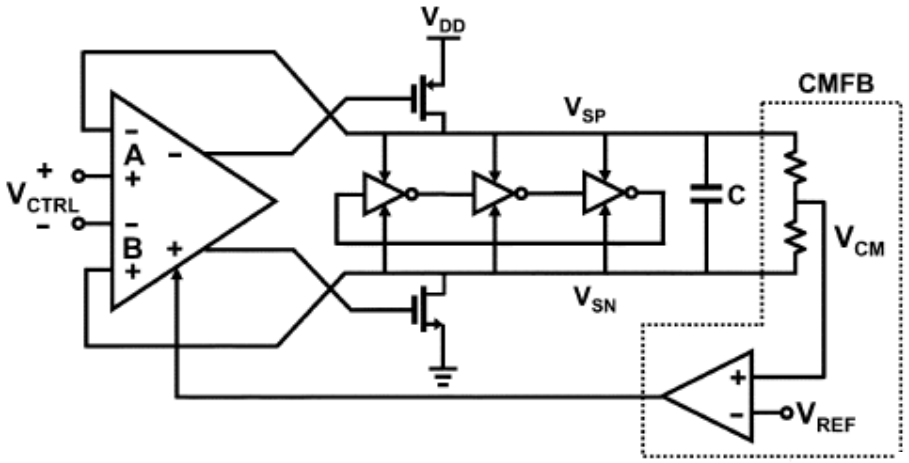


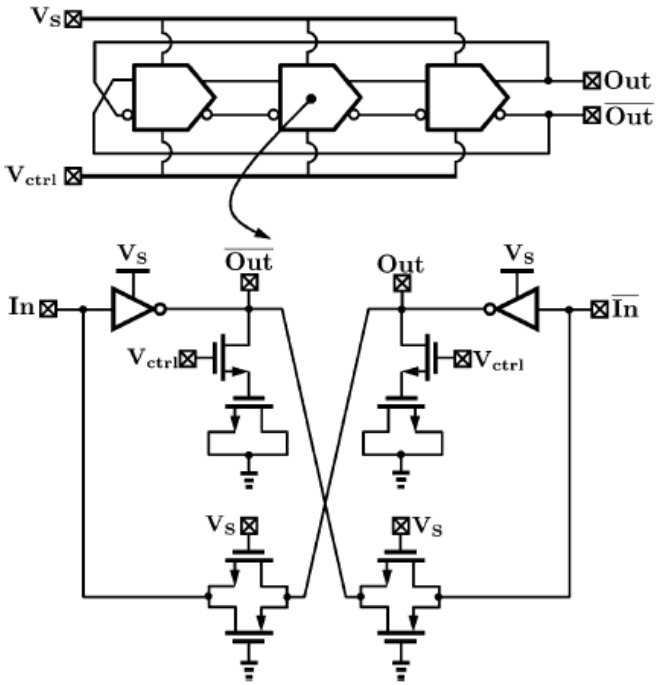
Fig. 8. Final VCO configuration.

2720 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

A 0.5-GHz to 2.5-GHz PLL With Fully Differential Supply Regulated Tuning

Merrick Brownlee, *Student Member, IEEE*, Pavan Kumar Hanumolu, *Student Member, IEEE*, Kartikeya Mayaram, *Fellow, IEEE*, and Un-Ku Moon, *Senior Member, IEEE*

Supply-Regulated Split-Tuning



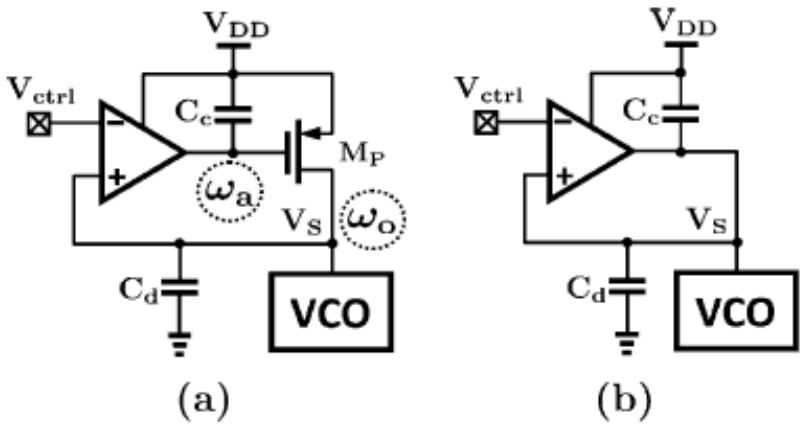


Fig. 4. Conventional regulators used in a supply-regulated PLL: (a) using a pass transistor. (b) without using the pass transistor.

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Low-Power Supply-Regulation Techniques for Ring Oscillators in Phase-Locked Loops Using a Split-Tuned Architecture

Abhijith Arakali, *Student Member, IEEE*, Srikanth Gondi, *Member, IEEE*, and Pavan Kumar Hanumolu, *Member, IEEE*

References

1. B. Razavi, “Design of CMOS Analog Integrated Circuits,” McGraw Hill, 2002.
2. B. Razavi, “RF Microelectronics,” 2nd Ed., Prentice Hall, 2012.