**ECE 5/418 Memory/Clock Synchronization IC Design**
**Sample Midterm**
**Apr 25, 2013** **Name:** _____

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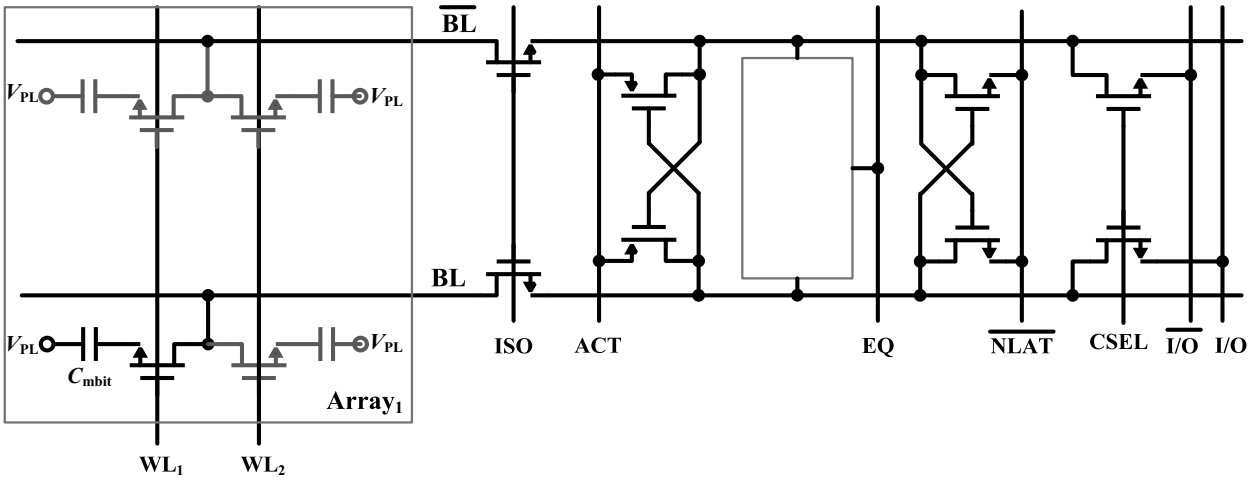
| Closed Book, Closed Notes, Closed Computer. |
| Only one page (A4 size, both sides) cheat-sheet allowed. |
| Show your steps clearly to get credit. |
| State clearly any assumptions made. |
| This exam has 3 questions, for a total of 100 points. |

1. Consider the section of a Folded-array DRAM seen below. Here, $C_{mbit} = 25\,fF$ for the Mbit capacitors, $C_{BL} = 100\,fF$ for the bitline capacitance, and $C_{IO} = 200\,fF$ for the I/O line capacitances. Further, $V_{DD} = 1V$, $V_{THN,P} = 0.3V$ and the plate voltage $V_{PL} = 0.5V$.



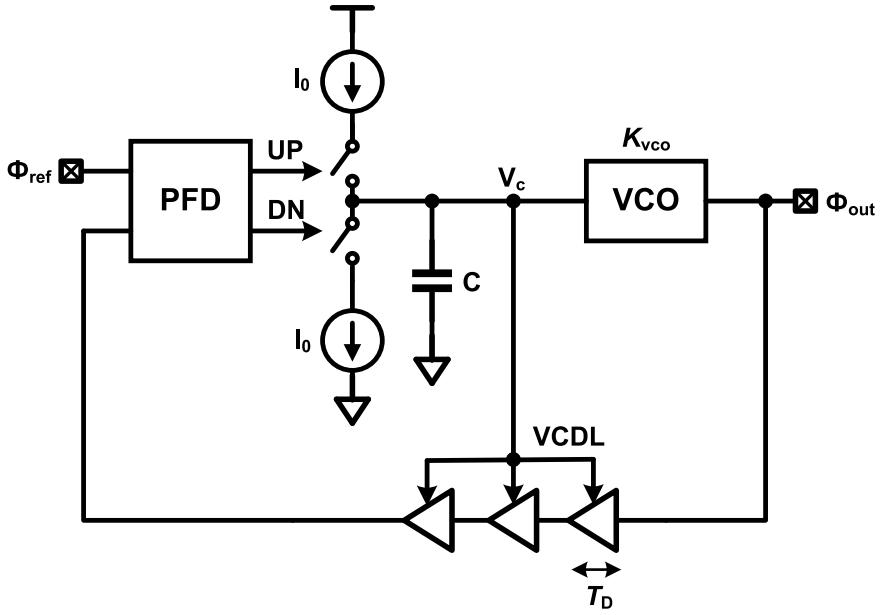

(a) (5 points) Sketch the EQ circuitry in the above figure.

(b) (10 points) Sketch the waveforms ($WL_1$, EQ, NLAT, ISO, ACT, Bitline voltage) when a stored "1" is **read** from the mbit cell on the intersection of wordline $WL_1$ and bitline $BL$. Assume $CSEL = 1$. Label your plots appropriately.

(c) (5 points) What is the sensed voltage on the bitlines after charge sharing in the read operation?

(d) (5 points) What is the purpose of the ISO transistors in the above circuit?

2. Consider an alternative PLL design shown below. Here, $K_{VCO} = 150\,\frac{MHz}{V}$, $I_0 = 100\mu A$, frequencies $f_{in} = f_{out} = 500$ MHz, and the delay of each of the elements in the VCDL is given as $T_D = 1\,\frac{ns}{V}$.




(a) (10 points) Draw the phase-domain small signal block diagram in steady state.

(b) (10 points) Find the expression for loop gain $L(s)$ and determine the pole and zero locations.

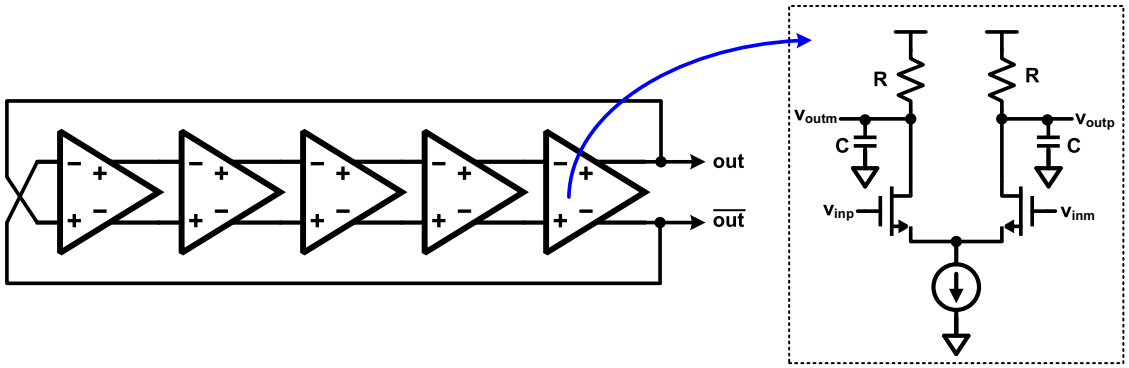
(c) (10 points) Determine the value of capacitor $C$ to achieve loop-gain phase-margin of $45^\circ$

(d) (10 points) Derive the expression for $H_{cl}(s) = \frac{\Phi_{out}}{\Phi_{ref}}$.

(e) (5 points) Sketch open- and closed-loop Bode magnitude and phase plots for the PLL.

(f) (Bonus 5 points) What is the main difference between the above proportional control and the conventional proportional path using a resistor.

3. Consider the differential ring oscillator shown below. Assume that all transistors are operating in saturation.




(a) (10 points) Find the frequency of oscillation $\omega_{osc}$ if $R = 1\,k\Omega$ and $C = 100\,fF$.

(b) (10 points) What is the minimum delay-cell transistor transconductance ($g_{m1}$) required for oscillation?

(c) (10 points) A 5-stage VCO needs to be designed based upon the above schematic. Draw schematic of a delay cell to achieve this with best possible PSRR.