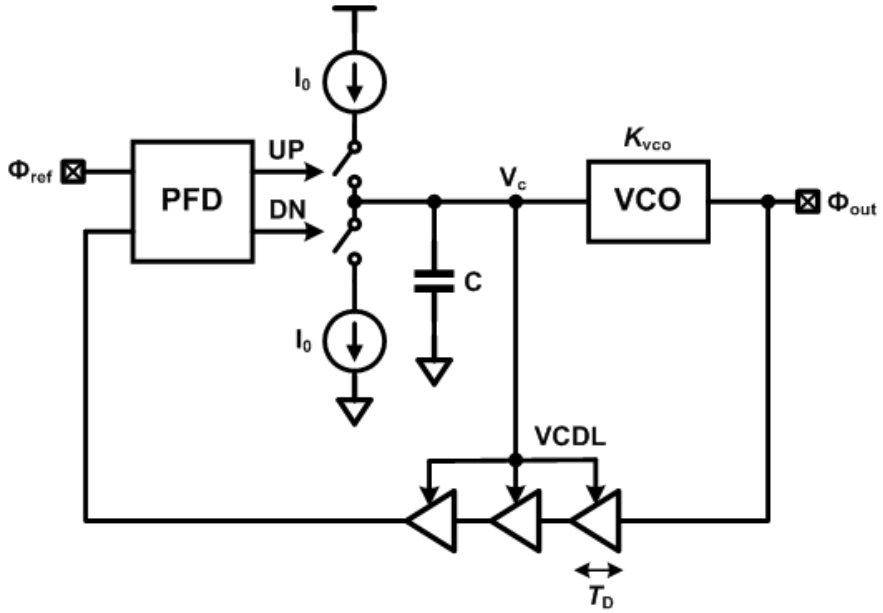
ECE 5/418 PLL and Memory IC Design
Sample Midterm
Apr 14, 2015 **Name:** _____

Closed Book, Closed Notes, Closed Computer.
Only one page (A4 size, both sides) cheat-sheet allowed.
Show your steps clearly to get credit.
State clearly any assumptions made.
This exam has 3 questions, for a total of 100 points.

1. Consider an alternative PLL design shown below. Here, $K_{VCO} = 150\,\frac{MHz}{V}$, $I_0 = 100\mu A$, frequencies $f_{in} = f_{out} = 500$ MHz, and the delay of each of the elements in the VCDL is given as $T_D = 1\,\frac{ns}{V}$.



(a) (10 points) Draw the phase-domain small signal block diagram in steady state.

(b) (10 points) Find the expression for loop gain $L(s)$ and determine the pole and zero locations.

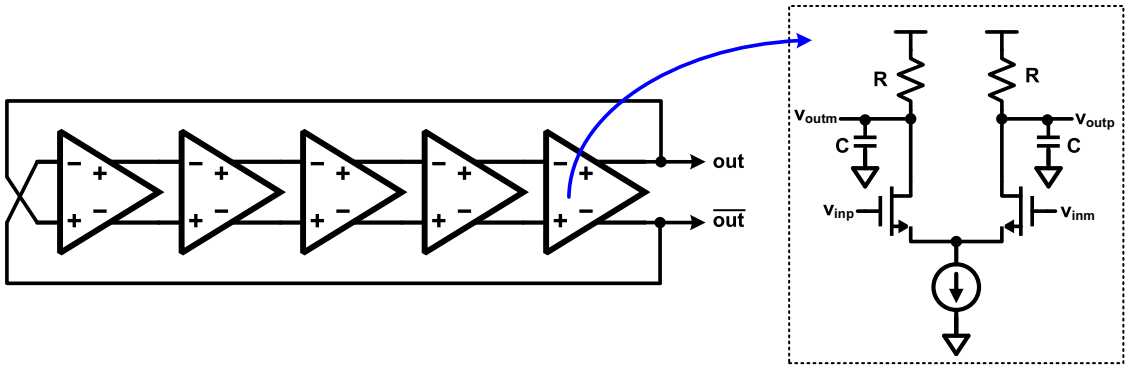
(c) (10 points) Determine the value of capacitor C to achieve loop-gain phase-margin of 45°.

(d) (10 points) Derive the expression for closed-loop transfer function $H_{cl}(s) = \frac{\Phi_{out}}{\Phi_{ref}}$.

(e) (5 points) Sketch open- and closed-loop Bode magnitude and phase plots for the PLL.

(f) (Bonus 5 points) What is the main difference between the above proportional control and the conventional proportional path using a resistor.

2. Consider the differential ring oscillator shown below. Assume that all transistors are operating in saturation.

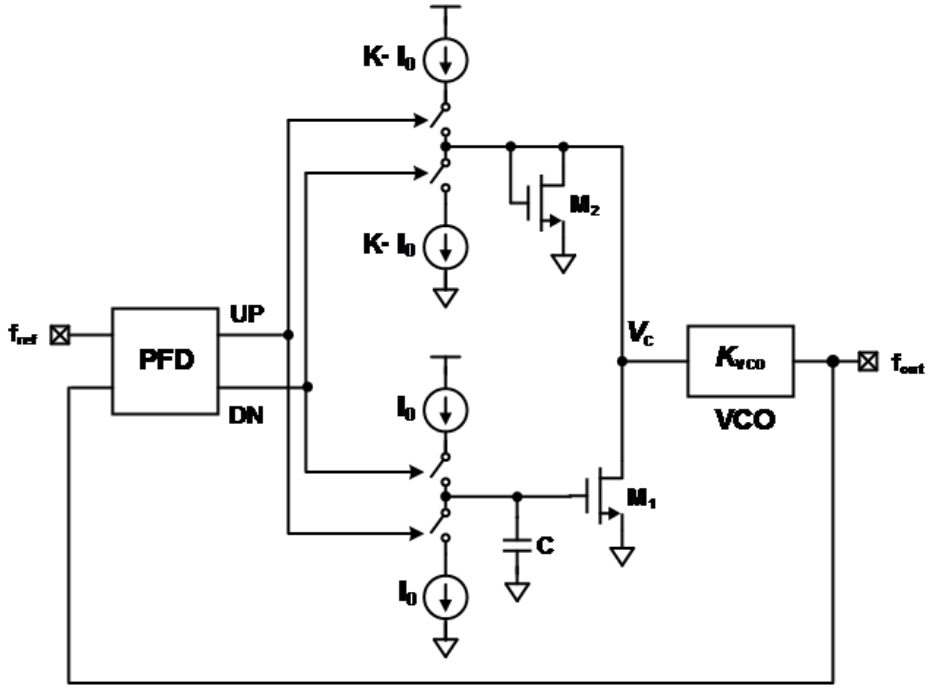


(a) (10 points) Find the frequency of oscillation ω_{osc} if $R = 1\,k\Omega$ and $C = 100\,fF$.

(b) (10 points) What is the minimum delay-cell transistor transconductance (g_{m1}) required for oscillation?

(c) (10 points) A 5-stage VCO needs to be designed based upon the above schematic. Draw schematic of a delay cell to achieve this with best possible PSRR.

3. In the resistor-less PLL shown below, assume that the VCO gain K_{VCO} is positive, all transistors operate in saturation with output resistance, $r_o = \infty$. Ignore the NMOS capacitance.



(a) (5 points) Draw the phase-domain *small-signal* block diagram in steady state.

(b) (5 points) What is the effective loop-filter transfer function, $F(s) = \frac{V_c(s)}{I_0}$?

(c) (5 points) Find the expression for loop gain $L(s)$ and determine the pole and zero locations.

(d) (5 points) Derive the expression for closed-loop transfer function $H_{cl}(s) = \frac{\Phi_{out}}{\Phi_{ref}}$.

(e) (5 points) In order to minimize the loop filter area, should K be minimized or maximized? Why?