Practical Phase-Locked Loop Design

2004 ISSCC Tutorial

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Outline

- Introduction
- Basic Feedback Loop Theory
- Circuits
- "Spectacular" Failures
- Appendices:
  - design for test
  - writing a PLL Spec
  - references
- Sorry: no DLL's in this tutorial

Intended Audience

- If you…
- Are a novice PLL designer
- Specify PLL requirements
- Integrate PLL's on-chip
- Test/debug PLL's
- Review PLL designs

Introduction

What is a PLL?

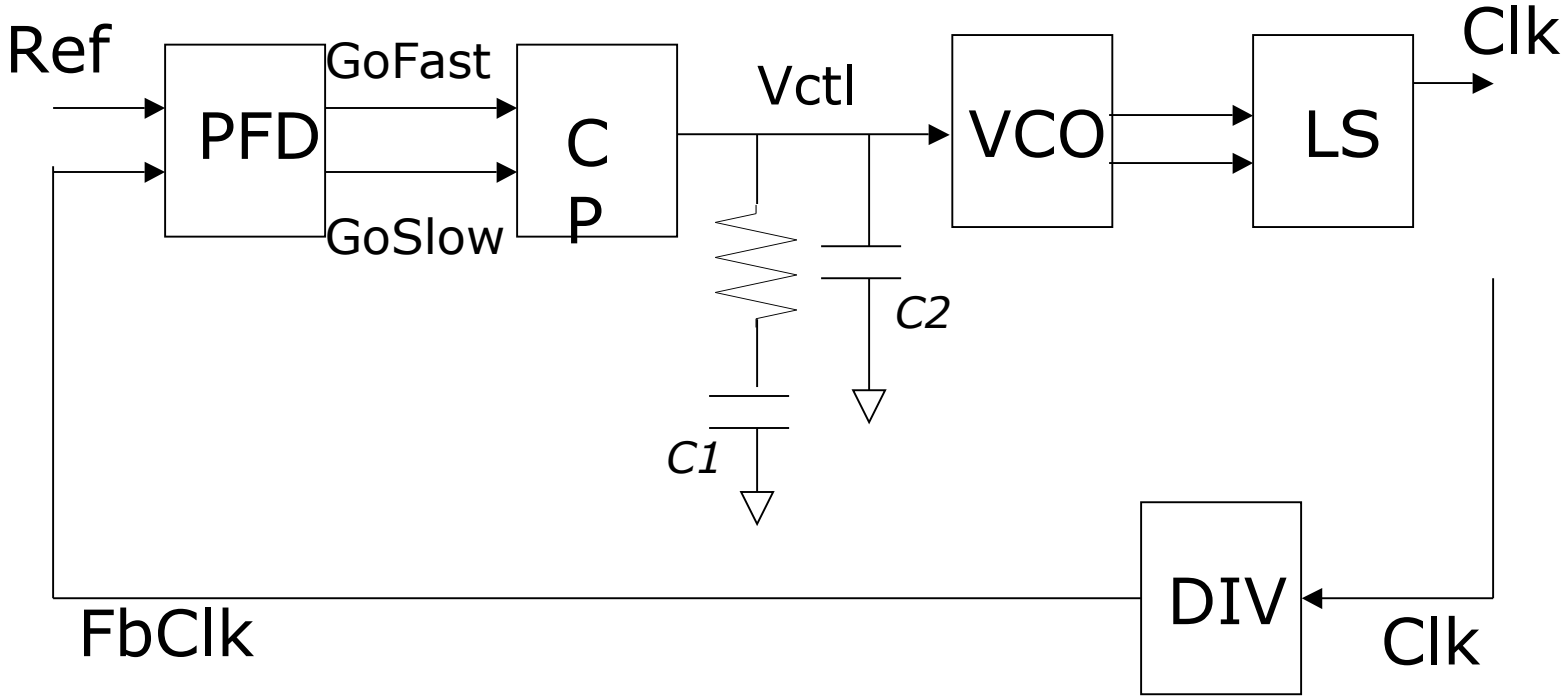
- A PLL is a negative feedback system where an oscillator-generated signal is phase and frequency locked to a reference signal.
- Analogous to a car's "cruise control"

How are PLL's Used?

- Frequency Synthesis (e.g. generating a 1 GHz clock from a 100 MHz reference)
- Skew Cancellation (e.g. phase-aligning an internal clock to the IO clock) (May use a DLL instead)
- Extracting a clock from a random data stream (e.g. serial-link receiver)

- ***Frequency Synthesis*** is the focus of this tutorial.

Charge-Pump PLL Block Diagram



Charge-Pump PLL Building Blocks

- Phase-Frequency Detector (*PFD*)
- Charge-Pump (*CP*)
- Low-Pass Filter (*LPF*)
- Voltage-Controlled Oscillator (*VCO*)
- VCO Level-Shifter (LS)
- Feedback Divider (*FBDIV*)
- Power Supply regulator/filter (*VREG*)?

Components in a Nutshell

- PFD: outputs digital pulse whose width is proportional to phase error
- CP: converts digital error pulse to analog error current
- LPF: integrates (and low-pass filters) error current to generate VCO control voltage
- VCO: low-swing oscillator with frequency proportional to control voltage
- LS: amplifies VCO levels to full-swing
- DIV: divides VCO clock to generate FBCLK clock

PLL Feedback Loop Theory

Is My PLL Stable?

- PLL is 2nd-order system similar to mass-spring-dashpot or RLC circuit.
- PLL may be stable or unstable depending on phase margin (or damping factor).
- Phase margin is determined from linear model of PLL in frequency-domain.
- Find phase margin/damping using MATLAB, loop equations, or simulations.
- Stability affects phase error, settling, jitter.

What Does PLL Bandwidth Mean?

- PLL acts as a low-pass filter with respect to the reference.
- Low-frequency reference modulation (e.g.spread-spectrum clocking) is passed to the VCO clock.
- High-frequency reference jitter is rejected.
- "Bandwidth" is the frequency at which the PLL begins to lose lock with the reference (-3dB).
- PLL acts as a high-pass filter wrt VCO noise.
- Bandwidth affects phase error, settling, jitter.

Closed-loop PLL Transfer Function

- Analyze PLL feedback in frequency-domain
- Assumes continuous-time behavior
- $H(s) = \phi_{fb} / \phi_{ref} = G(s)/(1+G(s))$ →closed-loop gain
- $G(s) = (K_{vco}/s)I_{cp}F(s)/M$ → open-loop gain

  where

  K_{vco} = VCO gain in Hz/V

  I_{cp} = charge pump current in Amps

  F(s) = loop filter transfer function

  M = feedback divisor

  C_1 = large loop-filter capacitor

Closed-loop PLL Transfer Function

- General Form (ignoring C_2):

  $H(s) = \omega_n^2 (1 + s/\omega_z) / (s^2 + 2s\zeta\omega_n + \omega_n^2)$

  where

  ω_n = natural freq = $\sqrt{K_{vco} I_{cp} / M C_1}$

  ω_z = stabilizing zero = $1 / RC_1$

  ζ = damping = $(RC_1/2) * \sqrt{K_{vco} I_{cp} / M C_1}$

- If $\zeta < 1$, complex poles at $-\zeta\omega_n \pm j\omega_n * \sqrt{1 - \zeta^2}$
  - Real → exponential delay
  - Imag → oscillation

What Determines Stability and Bandwidth?

- Damping Factor (measure of stability)
- Natural Frequency (measure of bandwidth)
- Damping and natural frequency can be set independently by LPF resistor

PLL Loop Equations

- Undamped Natural Frequency:

  $\omega_n = \mathrm{sqrt}(K_{vco} * I_{cp} / (M * C_1))$ in rad/sec

  where

  K_{vco} = VCO gain in Hz/V

  I_{cp} = charge pump current in Amps

  M = feedback divisor

  C_1 = large LPF capacitor

- For stability: $\omega_n / 2\pi$ < ~1/20 reference frequency
- Typical value: 1 MHz < $\omega_n / 2\pi$ < 10MHz.

PLL Loop Equations

- Damping Factor: usually 0.45 < ζ < ~1.5

  $\zeta = R_{lpf} * C_1 * \omega_n / 2$

- Useful Relation:

  Phase margin ~ 100 * ζ (for ζ < 0.65)

- Loop Decay Time Constant = $1/(\zeta * \omega_n)$

  - used to estimate settling time

  - 98% settling in 4 time constants

  Decay ~ $1- \exp(-t*\zeta * \omega_n)$

PLL Loop Eqns: Limits on R_{lpf}

- PFD must sample faster than loop can respond to act like continuous-time system
- Discrete Time Stability Limit (Gardner,1980):

$$\omega_n^2 < \omega_{ref}^2 / (\pi*(R_{lpf}C_1* \omega_{ref} + \pi))$$

- E.g. $\omega_{ref} = 2\pi*125MHz$, $C_1=75pF$, $\omega_n=2\pi*2MHz$

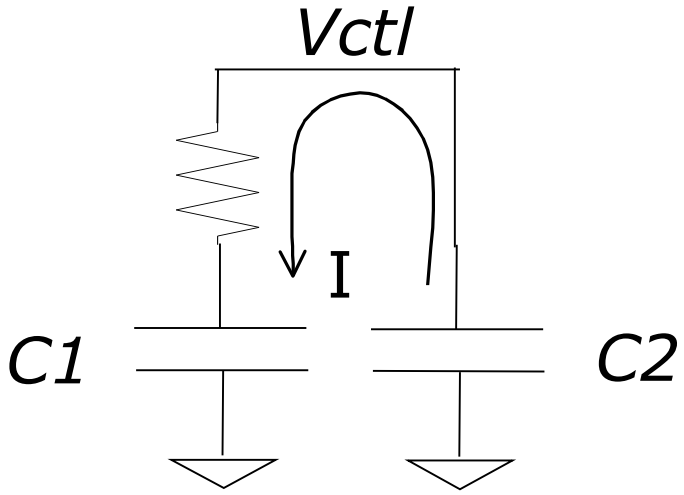
  → $R_{max} < 21$ kOhm
- $R_{lpf} < 1/5\ R_{max}$ for good phase margin
- For details: see Gardner (1980), Fig. 4

PLL Loop Eqns: Limits on R_{lpf}

- Parasitic LPF Pole: $R_{lpf} * C_2 \sim T_{ref} / \square$

→ if we want $V(C_1) \sim V(C_2)$ by end of T_{ref} (goal)

(Maneatis ISSCC '03)



$$I = (V_{c2} - V_{c1})/R$$

$$\square = RC_2$$

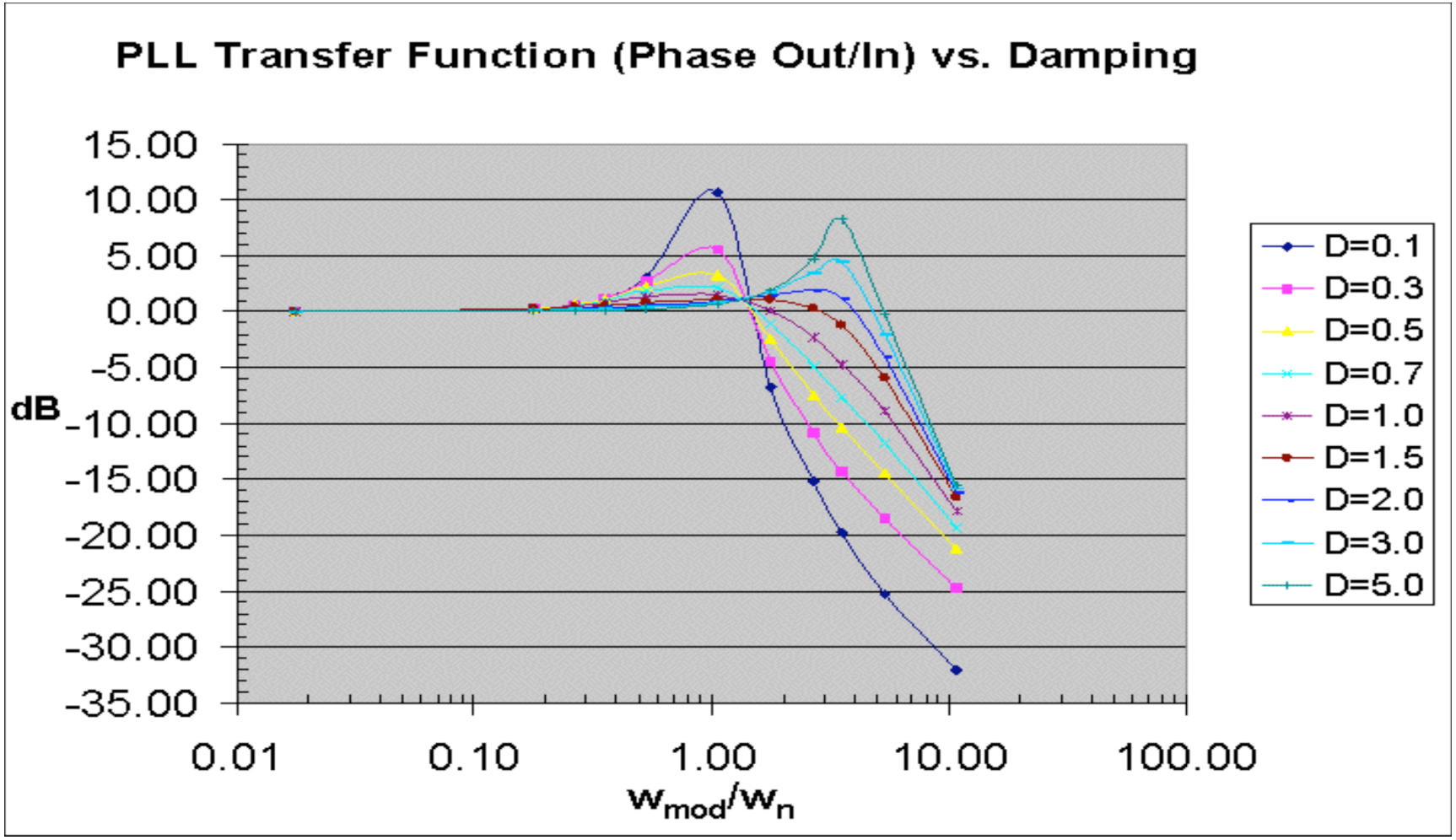
Bode Plot Primer

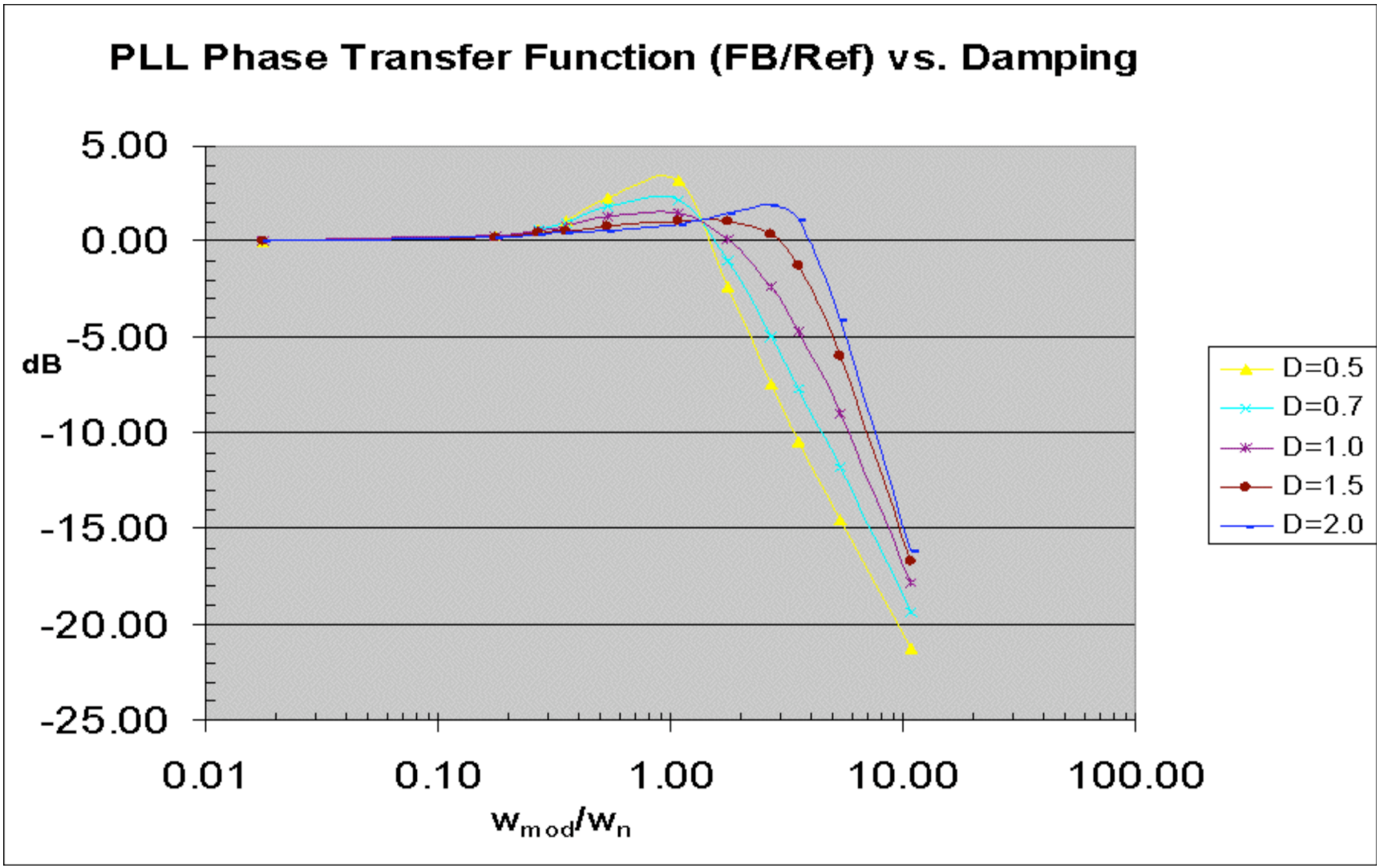
- Used to analyze frequency domain behavior
- Y-axis: gain in dB. E.g. 20dB=10X gain. 3dB=1.4X
- X-axis: frequency. Log scale
- Assuming "left-hand-plane" location:
  - Pole: -20db/dec magnitude loss and -90° phase shift. Capacitor → pole.
  - Zero: +20db/dec magnitude and +90° phase shift. Resistor → zero.

PLL Response vs. Damping

Phase Tracking vs. Damping

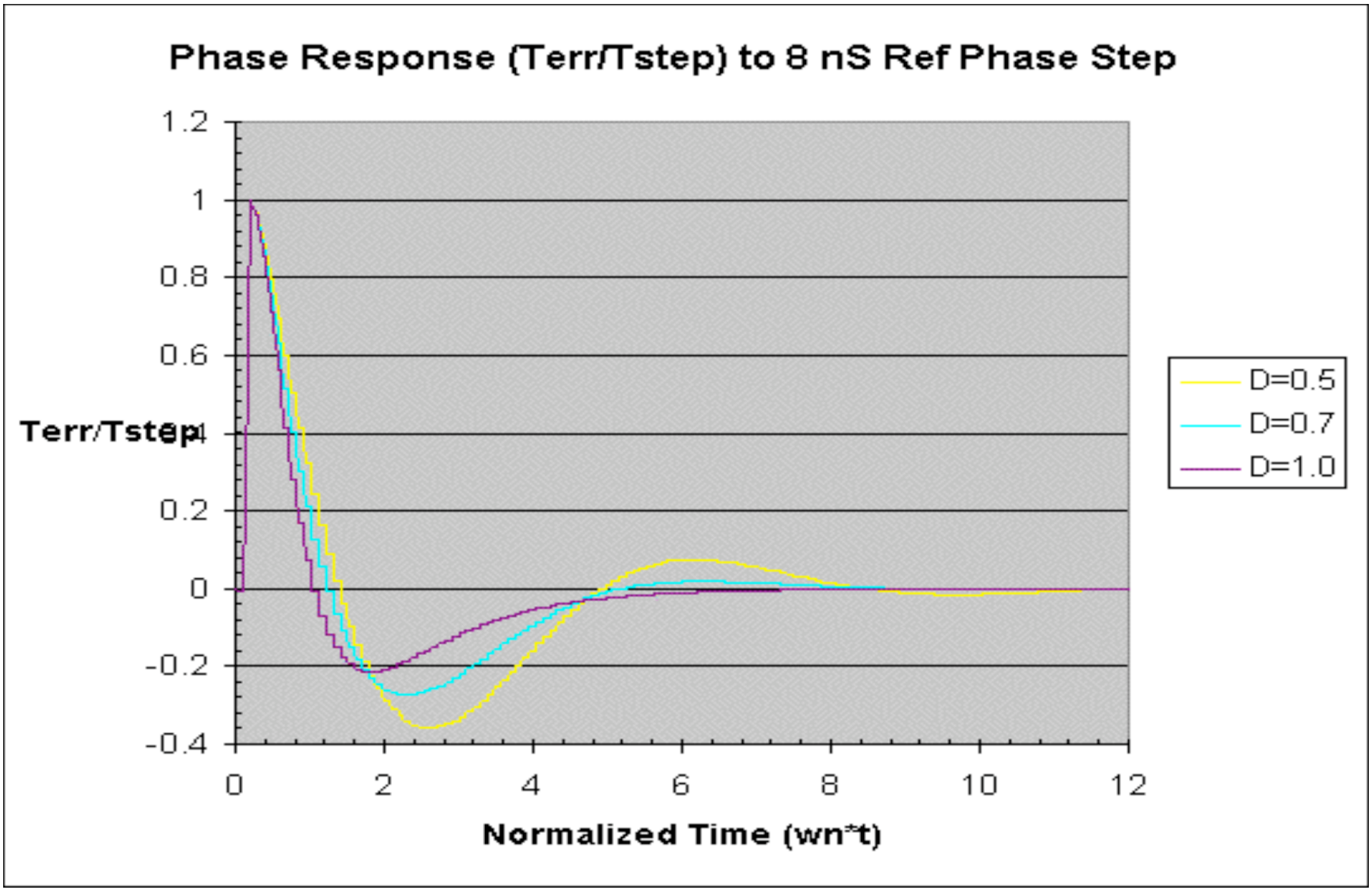
- Peaking at low and high damping factors → bad
- Damping ~ 1 → good compromise
- Phase Tracking → think "accumulated" jitter or phase error
- VCO frequency peaking (aka period jitter) similar to phase peaking

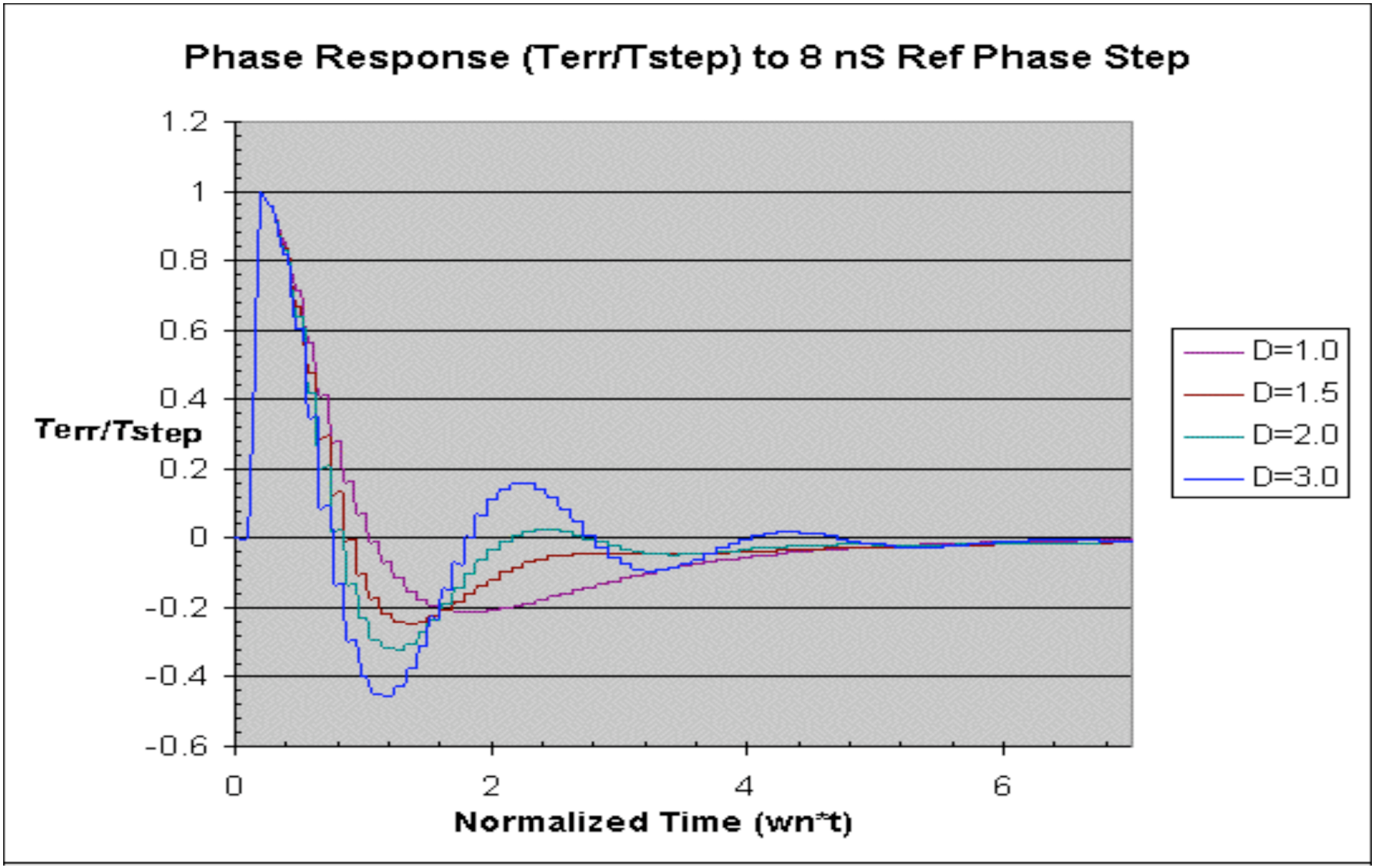




Transient: Phase Error vs.Damping

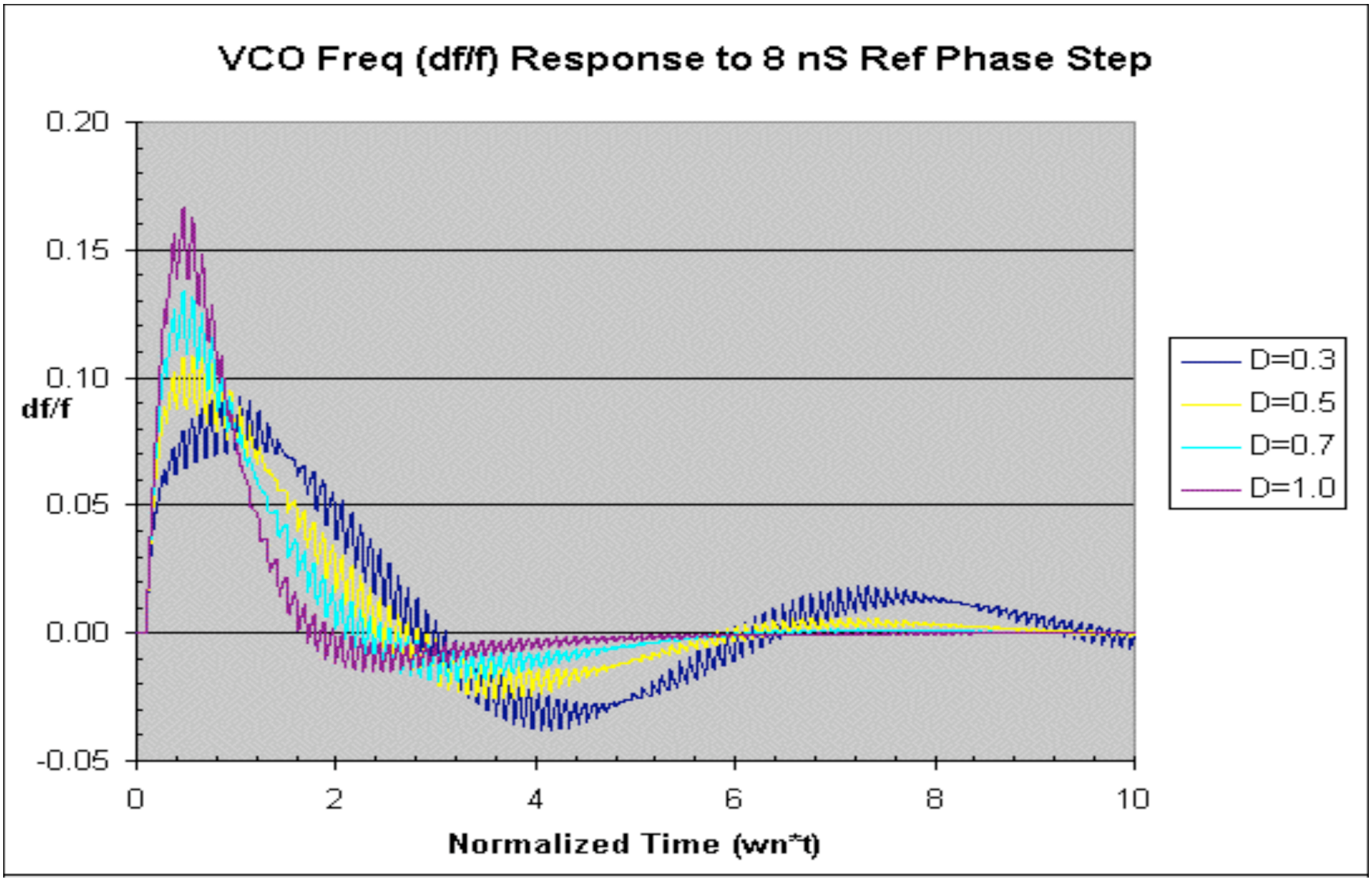
- Less ringing and overshoot as □ → 1
- Severe overdamping → ringing and overshoot
- Ringing at high damping due to low oversampling (large R) – Gardner limit.

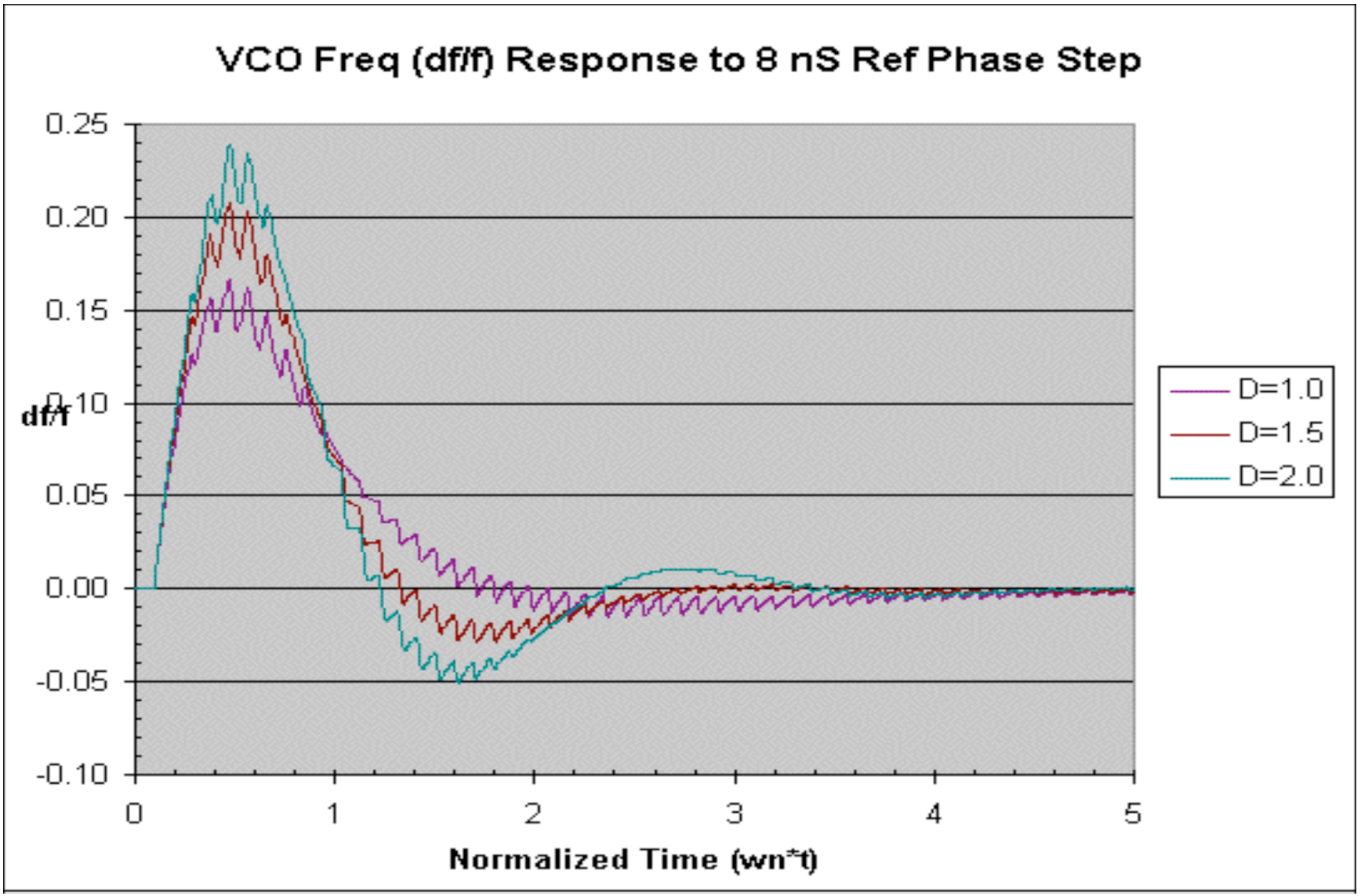




VCO Jitter (df/f) vs. Damping

- Low damping → less period jitter, slower response, more phase error
- High damping → low oversampling (large R) causes oscillation

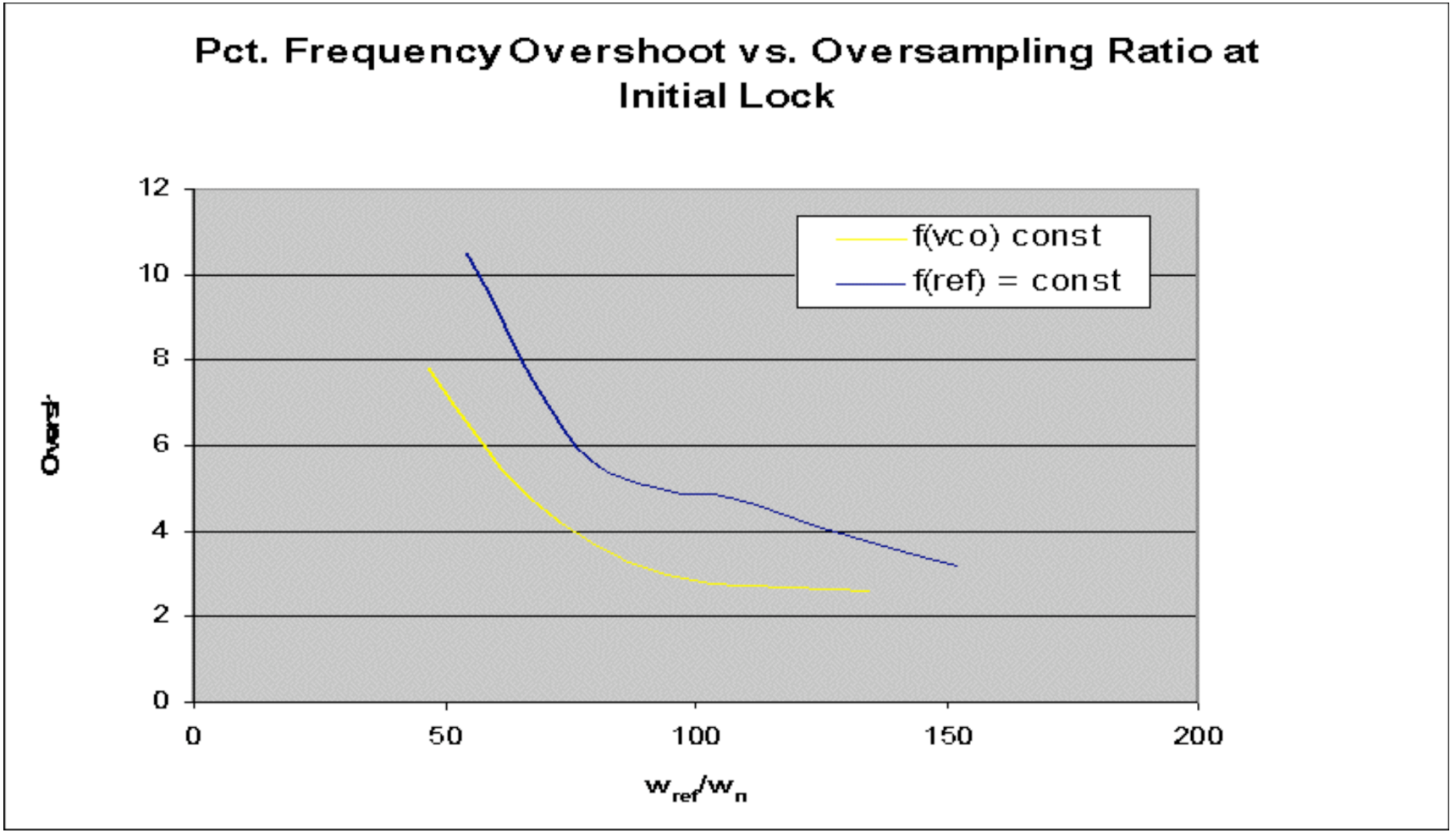




PLL Response vs. Bandwidth

VCO Freq. Overshoot vs. Bandwidth

- Lower BW → lower overshoot
- Higher OverSamplingRatio (ω_{ref}/ω_n) → lower bandwidth(BW)
- Note: ζ ~ BW in these simulations



Phase Error (due to VCO Noise) vs. BW

- For random VCO noise (I.e. thermal): lower BW → higher accumulated phase error
- Why? More jittery VCO cycles before PLL starts to correct:

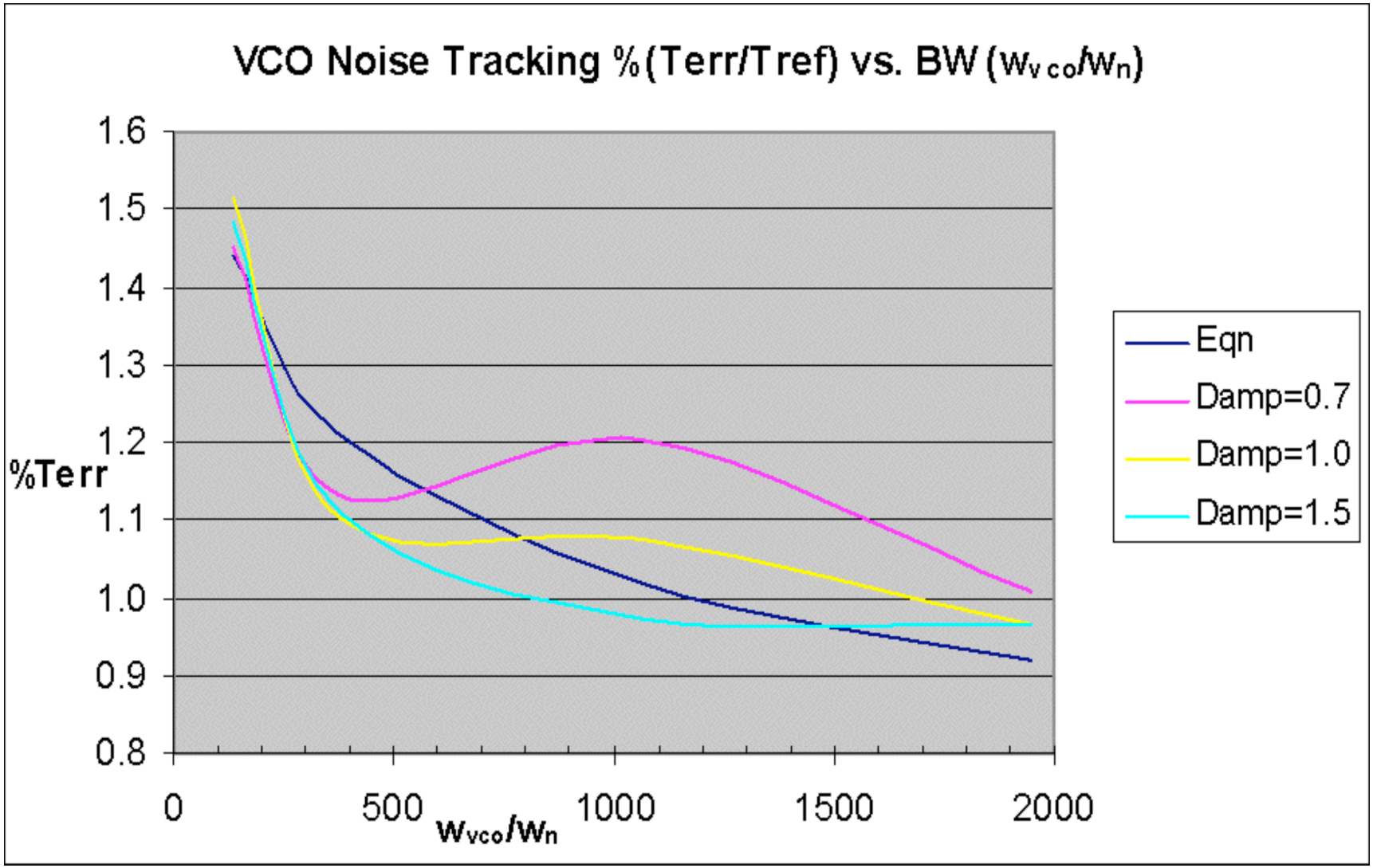
$T_{err} \sim J_{rms} * \text{sqrt}(2\zeta f_{vco}/\omega_n)$

where

J_{rms} = std dev of VCO period jitter

- valid for damping ~ 1

- assume: $J_{rms} \sim 1/f_{vco}$ → higher f, lower J_{rms}



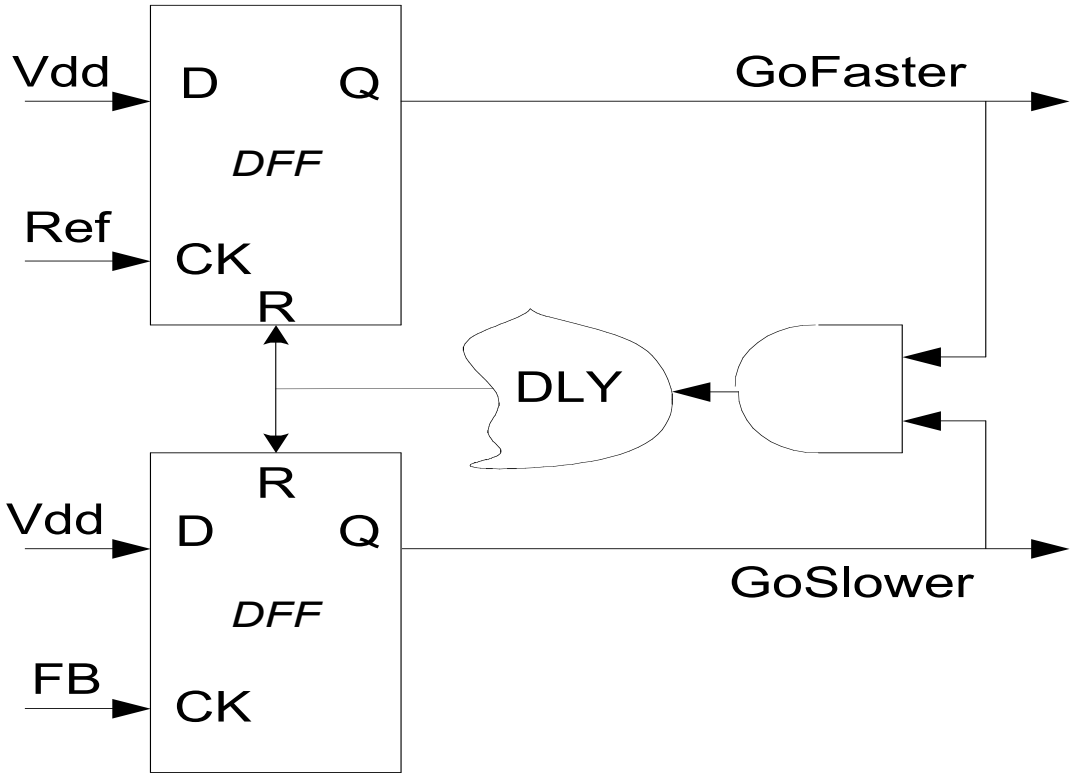
PLL Circuits

- Phase-Frequency Detector
- Charge-Pump
- Low-Pass Filter
- Voltage-Controlled Oscillator
- Level-Shifter
- Voltage Regulator

Phase-Frequency Detector(PFD)

PFD Block Diagram

- Edge-triggered - Input duty-cycle doesn't matter
- Pulse-widths proportional to phase error

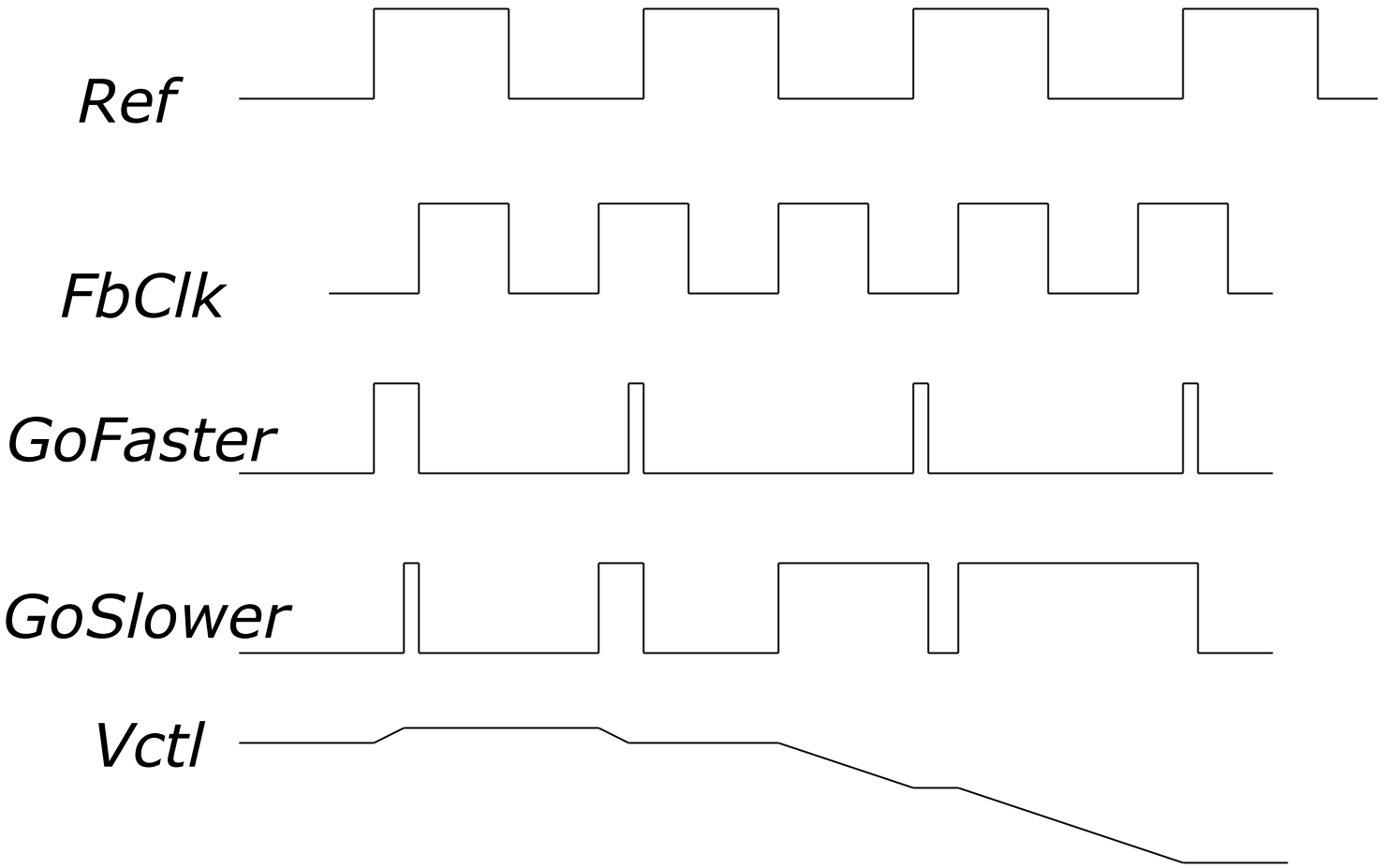


PFD Logic States

- 3 and "1/2" Output states
- States:

GoFaster	GoSlower	Effect:
0	0	No Change
0	1	Slow Down
1	0	Speed Up
1	1	Avoid Dead-Zone

Example: PFD



Avoiding the Dead-Zone

- "Dead-zone" occurs when the loop doesn't respond to small phase errors - e.g. 10 pS phase error at PFD inputs:
  - PFD cannot generate 10 pS wide *GoFaster* and *GoSlower* pulses
  - Charge-pump switches cannot turn on and off in 10 pS
  - Solution: delay reset to guarantee min. pulse width (typically > 150 pS)

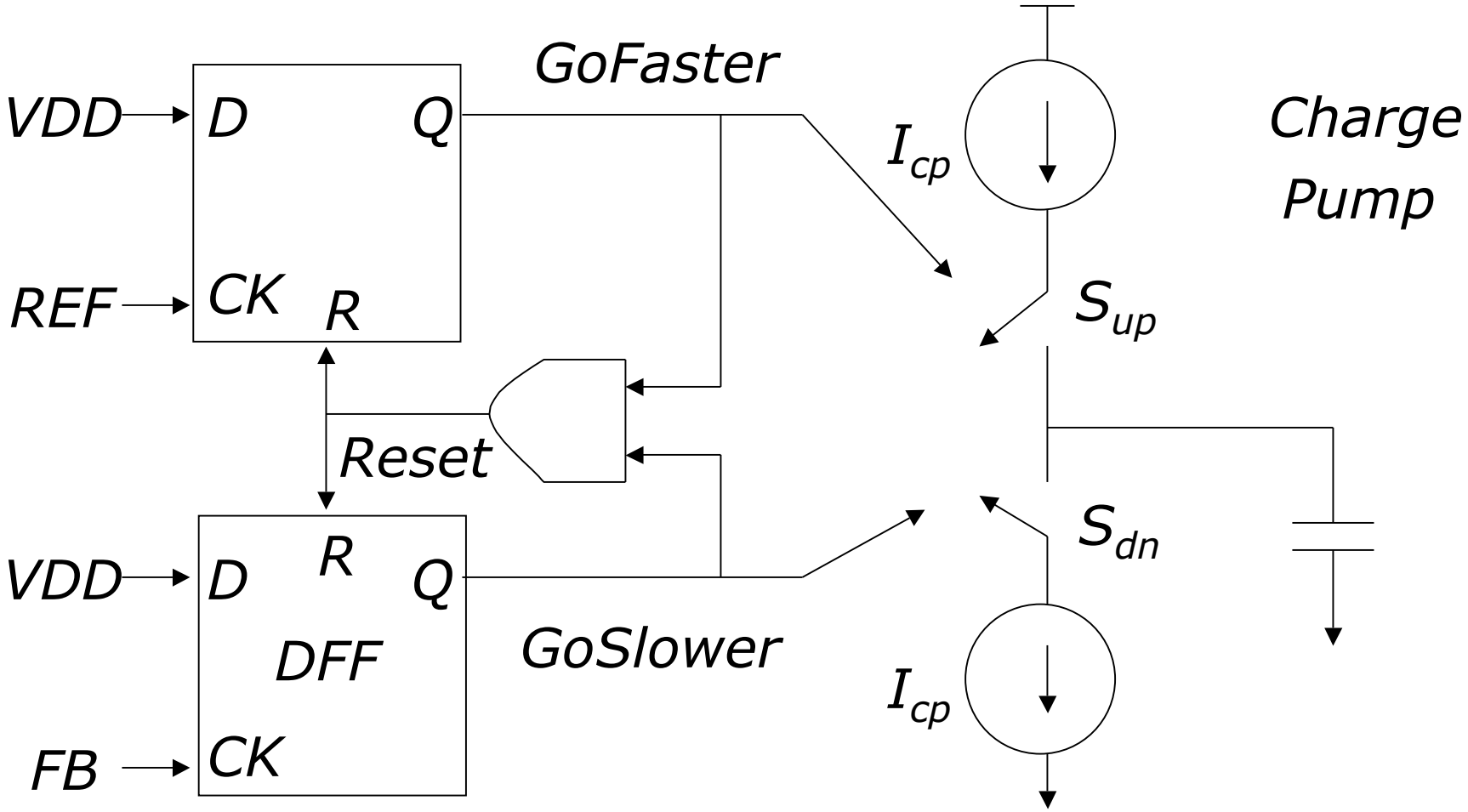
Charge Pump(CP)

Charge Pump

- Converts PFD phase error (digital) to charge (analog)
- Charge is proportional to PFD pulse widths

$$Q_{cp} = I_{up} * t_{faster} - I_{dn} * t_{slower}$$

- Q_{cp} is filtered/integrated in low-pass filter



Charge-Pump Wish List

- Equal *UP/DOWN* currents over entire control voltage range - reduce phase error.
- Minimal coupling to control voltage during switching - reduce jitter.
- Insensitive to power-supply noise and process variations – loop stability.
- Easy-to-design, PVT-insensitive reference current.
- Programmable currents to maintain loop dynamics (vs. M, f_{ref})?
- Typical: 1□A (mismatch)< I_{cp} < 50 □A (□V_{ctl})

Static Phase Error and CP Up/Down Mismatches

- Static Phase Error: in lock, net *UP* and *DOWN* currents must integrate to zero
  - If *UP* current is 2X larger, then *DOWN* current source must be on 2X as long to compensate
  - Feedback clock must lead reference for *DOWN* to be on longer
  - $T_{err} = T_{dn} - T_{up} = T_{reset} * (I_{up}/I_{dn} - 1)$

Static Phase Error and CP Up/Down Mismatches

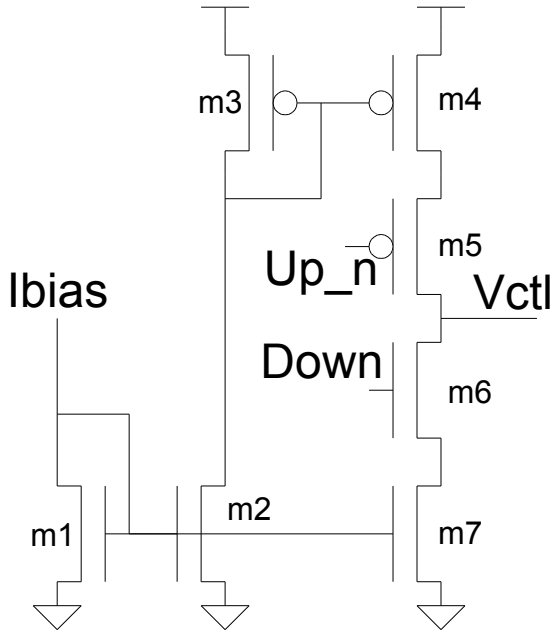
- Phase error can be extremely large at low VCO frequencies (esp. if self-biased) due to mismatch in current mirrors (low V_{gs}-V_t)
- Increase V_{gs} or decrease ΔV_t (large W*L)
- Typical static phase error < 100 pS

VCO Jitter and CP Up/Down Mismatches

- PFD-CP correct at rate of reference (e.g. 10nS).
- Most phase error correction occurs near reference rising edge and lasts < 200 pS, causing a control voltage ripple.
- This ripple affects the VCO cycles near the reference more than VCO cycles later in the ref cycle, causing VCO jitter.
- Typ. Jitter << 1% due to *Up/Down* Mismatches
- Avoid ripple by spreading correction over entire ref cycle. (Maneatis JSSC ’03)

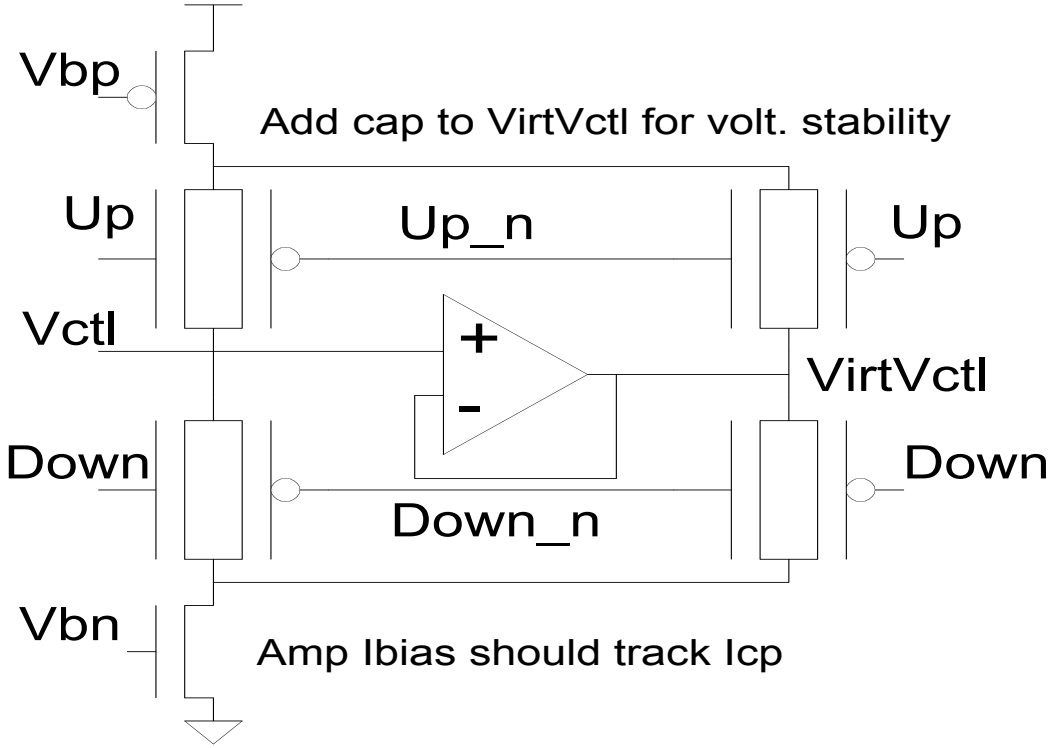
Simple Charge Pump

- R(switches) varies with V_{ctl} due to body-effect
- Use CMOS pass-gate switches for less V_{ctl} sensitivity
- Long-channel current sources for matching and higher R_{out}



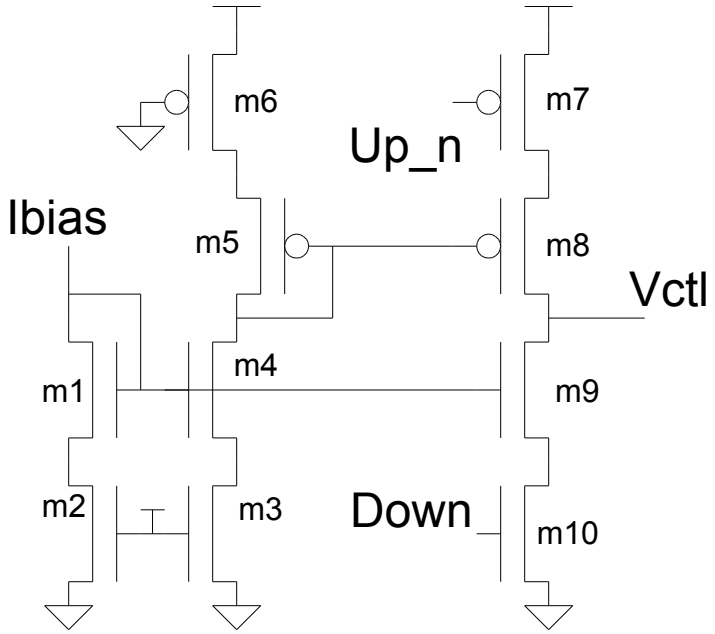
Charge Pump: const I with amp

- Amp keeps V_{ds} of current sources constant (Young '92)
- Amp sinks "waste" current when UP, DOWN off

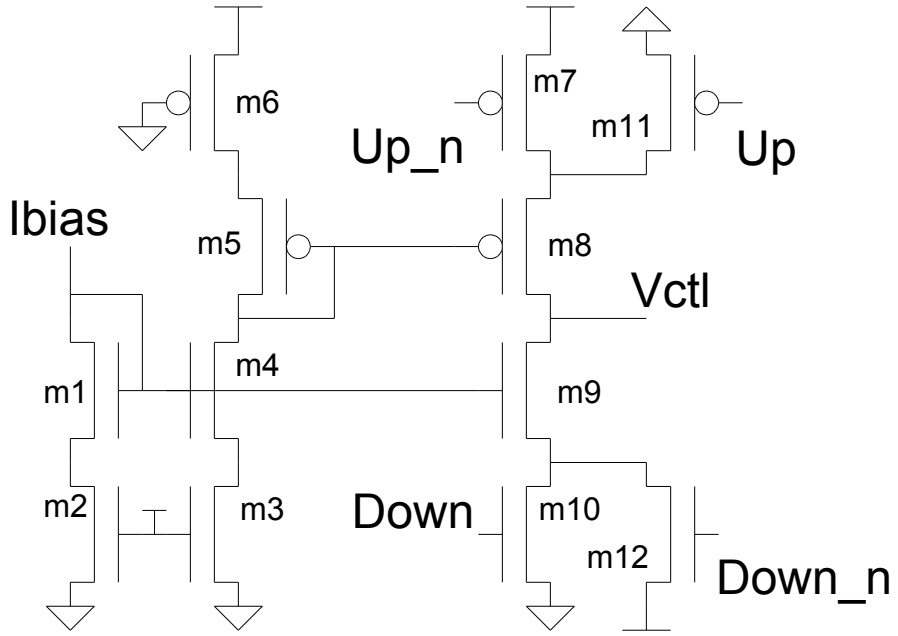


Charge Pump – switches reversed

- Switches closer to power rails reduce noise and V_{ctl} dependence → I_{cp} not constant with up/down



Charge Pump: switches reversed with fast turn-off (Ingino '01)

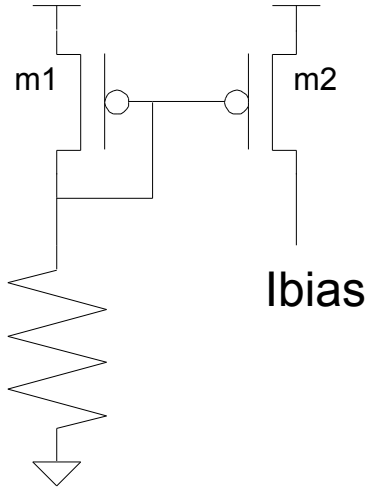


m1,m4,m5,m8,m9: long L

m11, m12: faster turn-off

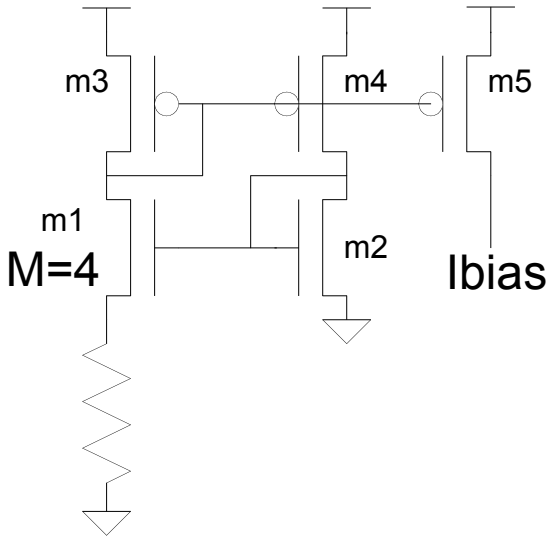
Simple Charge-Pump Bias

- $I_b \sim (V_{dd} - V_t)/R$
- I_b dependent on PVT
- Prefer low-V_t, moderate-to-long L for process insensitivity, large W/L for low gate-overdrive
- Pro: Simple, stable. Con: Vdd dependence



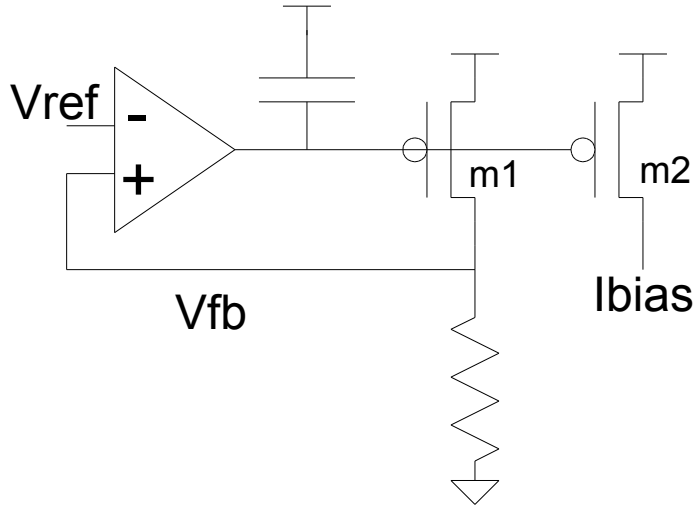
VDD-independent Ibias

- $I_b \sim 1/R^2$
- Con: requires start-up circuit not shown



Bandgap-based Ibias

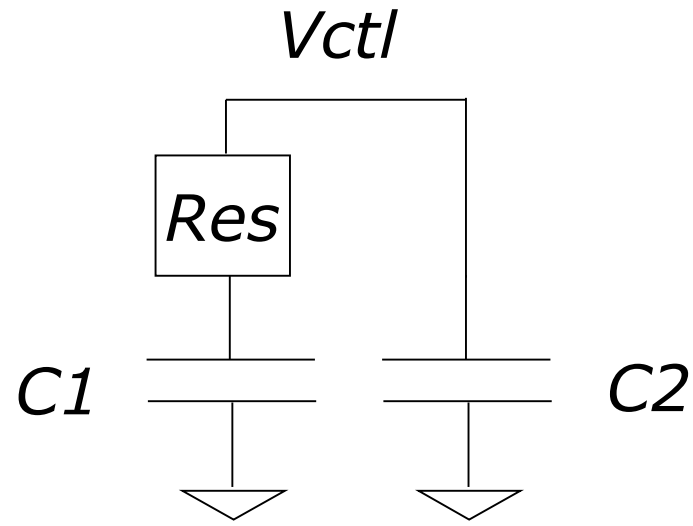
- $I_b \sim V_{ref}/R$
- Con: feedback loop may oscillate
  - cap added to improve stability
- Pro: VDD-independent, mostly Temp independent



Low-Pass Filter (LPF)

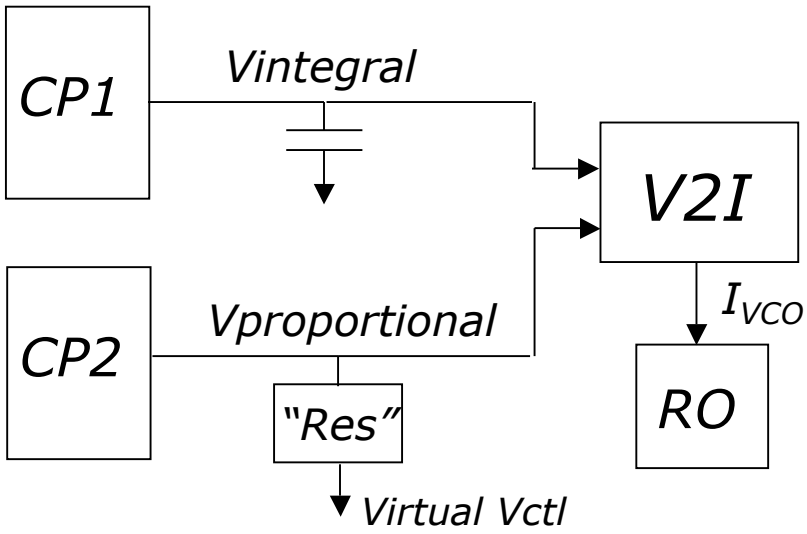
Low-Pass Filter

- Integrates charge-pump current onto C_1 cap to set average VCO frequency ("integral" path).
- Resistor provides instantaneous phase correction w/o affecting avg. freq. ("proportional" path).
- C_2 cap smoothes large IR ripple on V_{ctl}
- Typical value: 0.5k < R_{lpf} < 20kOhm



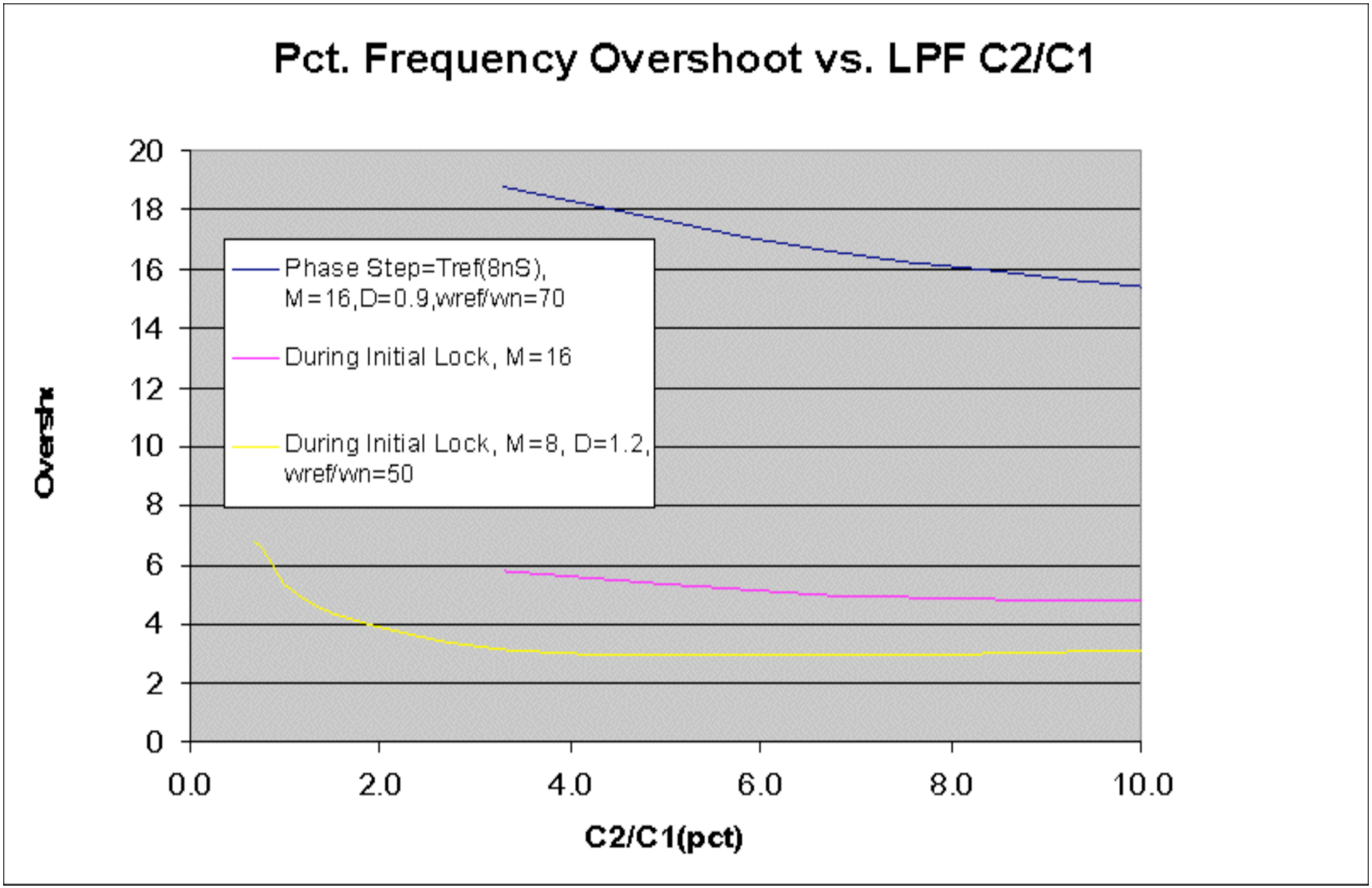
Feed-Forward Zero: eliminate R

- Resistor provides an instantaneous IR on the control voltage causing the VCO V2I to generate a current bump on the oscillator input
- Eliminate R → Add parallel CP path into V2I
- See Maneatis JSSC ’96 or ’03 for example



Low-Pass Filter Smoothing Cap(C_2)

- "Smoothing" capacitor on control voltage filters CP ripple, but may make loop unstable
- Creates parasitic pole: $\omega_p = 1/(R\ C_2)$
- $C_2 < 1/10 * C_1$ for stability
- $C_2 > 1/50 * C_1$ for low jitter
- Smoothing cap reduces "IR"-induced VCO jitter to < 0.5% from 5-10%
- $\Delta f_{vco} = K_{vco} I_{cp} T_{err} / C_2$
- Larger C_2/C_1 increases phase error slightly



Low-Pass Filter Capacitors

- At <= 130nm, thin-gate oxide leakage is huge:
  - I_{leak} ~ Vgate $^{4.5}$
  - NMOS leakier than PMOS
  - Weak temperature dependence
  - I_{leak} vs. t_{ox} → ~2-3X per Angstrom
- Use metal caps or thick-gate oxide caps to reduce leakage
- Metal caps use 10X more area than thin gate caps
  - Use minimum width/spacing parallel lines
  - Hard to LVS - Check extracted layout for correct connectivity

Low-Pass Filter Capacitors

- Even thick gate oxide may still leak too much
- Large filter cap (C_1) typically ranges from 50pF to 400 pF
- C_1 cap BW may be low as ~10X PLL BW for nearly ideal behavior
- Min C_2 BW set by T_{ref}
- Cap BW ~ $1/RC \sim 1/L^2$
- Gate cap not constant with V_{gs}

Voltage-Controlled Oscillator (VCO)

Voltage-Controlled Oscillator

- VCO usually consists of two parts: control voltage-to-control current (*V2I*) circuit and current-controlled ring oscillator (*ICO*)
- VCO may be single-ended or differential
- Differential design allows for even number of oscillator stages if differential-pair amps used for delay cells
- V2V may be used instead to generate bias voltages for diff-pair amps

PLL Suppression of VCO Noise

- PLL acts like a high-pass filter in allowing VCO noise to reach PLL output
- Need noise-immune VCO to minimize jitter
  - Feedback loop cannot react quickly.
- Power-supply noise is largest source of VCO noise

VCO Design Concerns

- Min low-frequency power-supply sensitivity
  < 0.05% per %dVDD → reduce phase error
- Min high-frequency power-supply sensitivity
  < 0.1% per %dVDD → reduce period jitter
  Note: this is 10X better than normal INV
- Low substrate-noise sensitivity → reduce ΔV_t
  – unnecessary in SOI
- Thermal noise (*kT*)
  – typically < 1% VCO period at high frequency

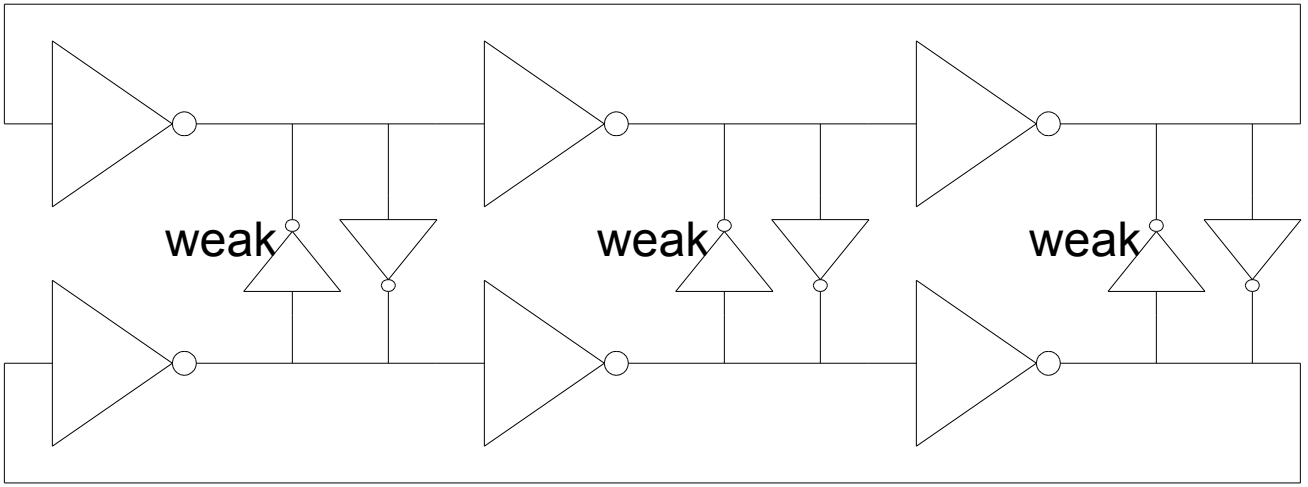
VCO Design Concerns

- Large frequency range to cover PVT variation:

  3-5X typical
- Single-ended or differential?
  - use differential for 50% duty-cycle
- Vco gain ($f_{vco} = K_{vco} * V_{ctl}$) affects loop stability
- Typical VCO gain: $K_{vco} \sim$ 1-3X * f_{max}
- More delay stages → easier to initiate oscillation
  - Gain(DC) > 2 for 3 stages
  - Gain(DC) > sqrt(2) for 4 stages

VCO w/"pseudo-differential" current-starved inverters

- Need odd # of stages
- Feedback INV → usually weaker by ~4X
- "Vdd" for inverters is regulated output of V2I

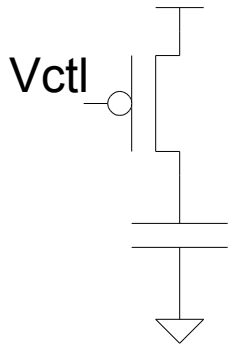


VCO V-to-I Circuits

- Converts V_{ctl} to I_{ctl}
- May generate additional V_{bias} for oscillator
- May use internal feedback to set VCO swing
- Provides power-supply rejection → fets in deep saturation or amp-based internal feedback
- Filters high-frequency V_{ctl} ripple w/another cap
- Adds parasitic pole → BW(V2I) >> BW(PLL)
- Digital *Range* settings allow for control of VCO gain and V_{ctl} range → must overlap ranges

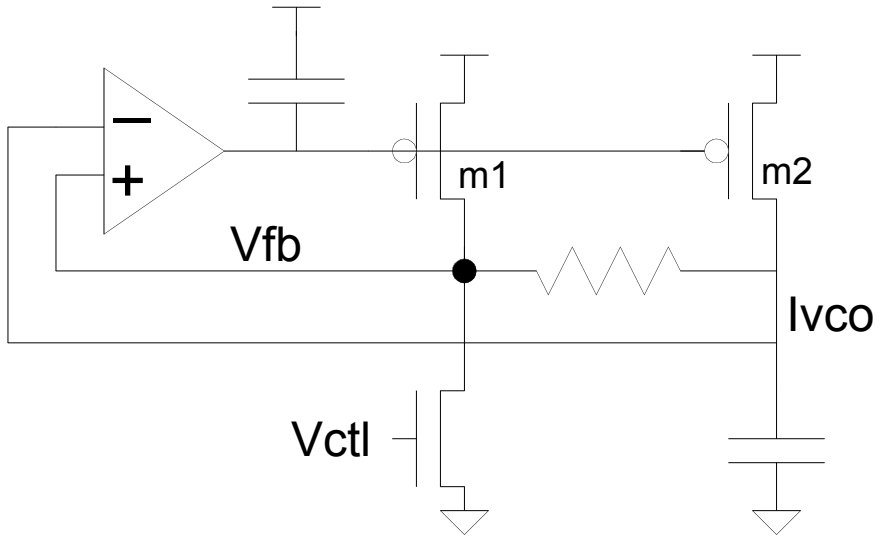
Simple V2I

- Minimal filtering of V_{ctl} ripple
- Keep long-channel current source in saturation
- Cap adds parasitic pole → $\omega_p = 1/(R_{vco}*C)$
- Typical Cap Size: 0.5 pF < C < 5 pF
- Reference V_{ctl} to same potential as LPF caps



V2I w/Feedback (V. von Kaenel (JSCC '96)

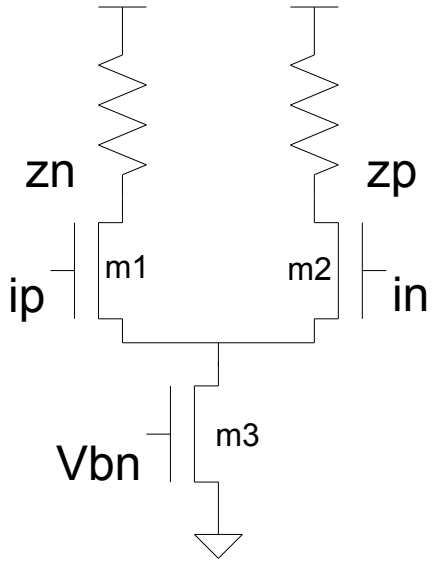
- Feedback → amp provides good low-freq power-supply rejection
- Cap to Vdd provides good high-freq rejection
- Start-up needed
- Stability concern?



Differential VCO's

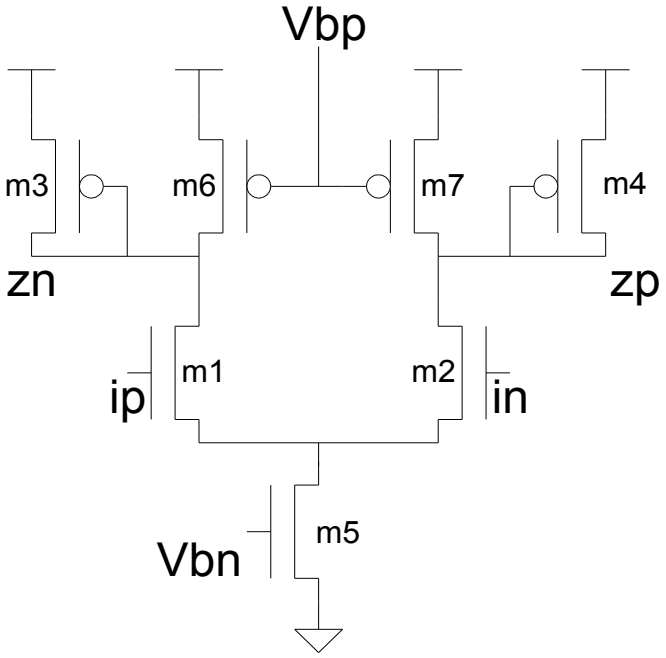
VCO: simple differential delay

- DC gain ~ g_{m1}*R
- Hard to get enough gain w/o large resistor
- Tail current controls delay – V2I needed?



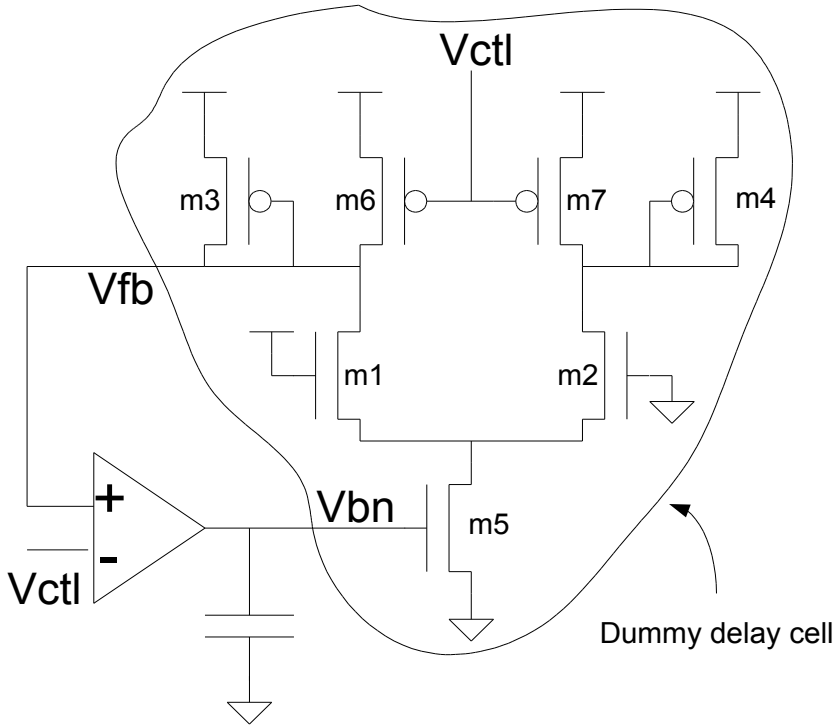
VCO: differential delay w/symmetric load (Maneatis '96)

- Loads acts like resistor over entire voltage swing
- Widely used but requires two bias voltages



V2I: replica bias - symmetric load

- $V_{swing} = V_{ctl}$ (Maneatis '96)
- Amp provides DC power-supply rejection
- Stable, but getting high BW and good PSRR tricky

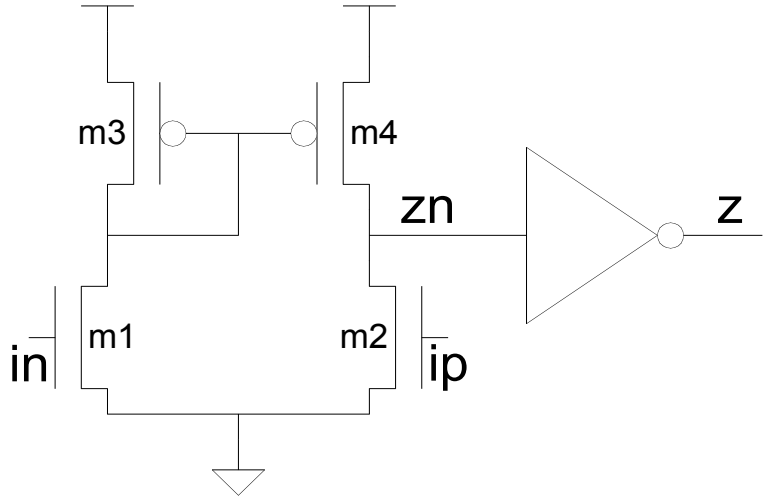


VCO Level-Shifter

- Amplify limited-swing VCO signals to full-rail
  - typically from 0.4-0.7V to VDD
- Maintain 50% duty-cycle
  - usually +/- 3%
  - difficult to do over PVT and frequency
- Insensitive to power-supply noise
  < 0.5 % per % dVDD
- Which power-supply? Analog or digital?
  - usually digital

VCO: Level-Shifter

- Need sufficient gain at low VCO frequency
- Use NMOS input pair if VCO swing referenced to VSS for better power-supply rejection
- Net "zn" should swing almost full-rail to switch output inverter



Feedback Divider

Feedback Divider (FBDIV)

- Divide VCO by N → $f_{ref} = f_{vco}/N$
- Divider may be internal to PLL or after CPU clock tree
- Max FBDIV frequency should be greater than max VCO frequency to avoid "run-away"
- Minimize FBDIV latency to reduce VDD-induced jitter seen at phase detector
- Loop Phase Margin Degradation ~ $\Delta_n T_{dly}$
  - usually insignificant

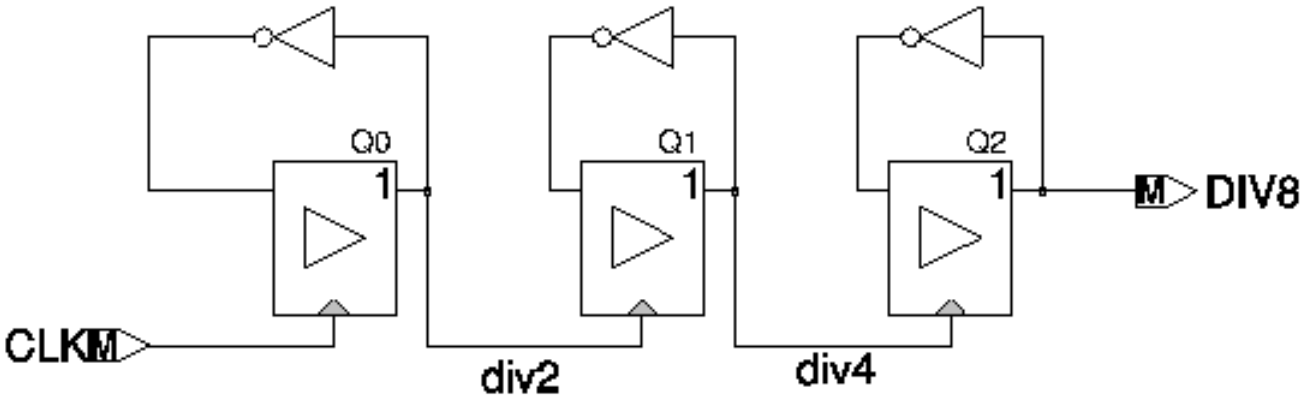
Feedback Divider

- Two common types of dividers:
  - Asynchronous cascade of div-by-2's
  - Synchronous counter – typically used

Asynchronous Divide-by-2

- Pro: fast, simple
- Pro: small area
- Con: long latency for large divisors
- Con: divide by powers of 2 only
- Can be used as front-end to synchronous counter divider to reduce speed requirements

Feedback Divider: cascade of div-by-2's



Counter-Based Divider

- Pro: divide by any integer N
- Pro: constant latency vs. N
- Pro: low latency
- Pro: small area → Binary-encoded.
- Con: slow if using ripple counter → don't
- Con: output may glitch → delay (re-sample) output by one cycle to clean up glitch

VDDA Voltage Regulator

Voltage Regulator/Filter

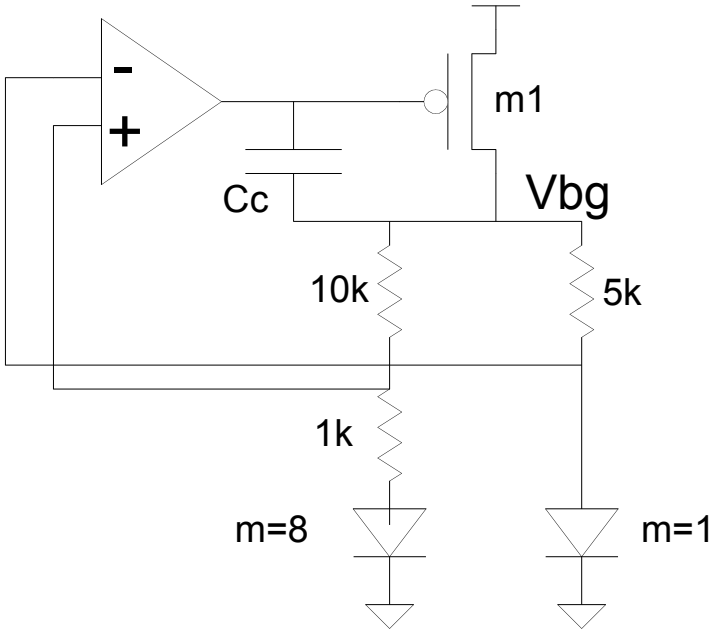
- Used to filter power-supply noise
  - typically > 20 dB (10x) PSRR over entire frequency range
  - desire 30+ dB
- Secondary purpose is to set precise voltage level for PLL power supply
  - usually set by bandgap reference

Voltage Regulator

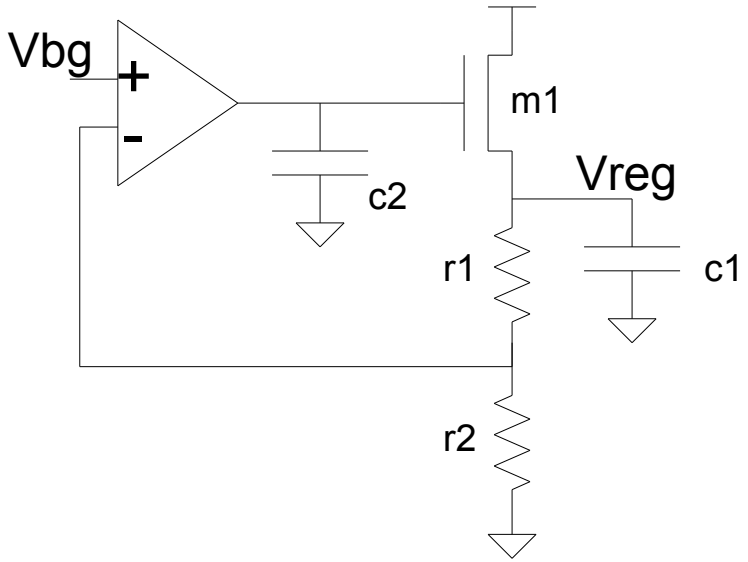
- Bandgap reference generates a voltage reference (~1.2V) that is independent of PVT
  - relies on parasitic diodes (vertical PNP)
- Regulator output stage may be source-follower (NFET) or common-source amp (PFET)
  - source-follower requires more headroom (and area?) but is more stable
  - common-source amp may be unstable without Miller capacitor or other compensation
- Beware of large, fast current spikes in PLL load (i.e. when changing PLL frequency range)

Bandgap Reference w/Miller Cap

- Stability and PSRR may be poor w/o Miller cap
- Miller cap splits poles. Can also add R in series w/Cc for more stability (Razavi ’00)



Voltage Regulator for VDDA



Advanced Concepts: Self-Biased PLL

- Conventional PLL: loop dynamics depends on I_{cp}, R_{lpf}, C_{lpf}, K_{vco} and FBDiv. These do not necessarily track.
- Why not generate all bias currents from the I(vco) and use a feed-forward zero to eliminate the resistor. Everything tracks. (Maneatis JSCC '03)
- Con: start-up, stability
- Pro: reduces PVT sensitivity

Example Circuit Parameters

- VDD=1.2V, f(max)-f(min) = 3 GHz
- K_{vco} = 5GHz/V → usable V_{ctl} range (0.6V)
- I_{cp} = 20 uA
- R_{lpf}=2500 Ohm
- C_1=75 pF → Area(metal) ~ 275um x 275um
- C_2=5 pF
- 0.85 < □ < 1.2
- 1.5 MHz < □$_n$/2□ < 2.1 MHz
- T_{acq} ~ 5 uS →T_{aqc} =~ 2CdV/I

Real-world PLL Failures

PLL Problem

- Problem: 3-stage PMOS diff-pair VCO wouldn't oscillate at low frequencies. When VCO finally started up at high Vctl, it outran FBDIV.
- Cause: leaky, mis-manufactured loads in delay cell reduced gain of delay element < 2
- Solutions:
  - increase L of load devices for higher gain
  - add more VCO stages to reduce gain requirements

PLL Problem

- Problem: VCO stuck at max frequency at power-on.
- Cause: PLL tried to lock before VDD was stable. Because VCO couldn't run fast enough to lock at low VDD, V_{ctl} saturated. When VDD finally stabilized, V_{ctl} = VDD, causing a maxed-out VCO to outrun FBDIV.
- Solution: maintain PLL RESET high until VDD is stable to keep V_{ctl} at 0V.

PLL Problem

- Problem: VCO stuck at max frequency after changing power-modes.
- Cause: Feedback DIV could not run fast enough to handle VCO overshoot when locking to a new frequency or facing a reference phase step.
- Solutions:
  - limit size of frequency steps
  - increase speed of Feedback DIV

PLL Problem

- Problem: PLL would not lock.
- Cause: Feedback DIV generated glitches causing PFD to get confused.
- Solution: add re-sampling flop to output of feedback DIV to remove glitches.

PLL Problem

- Problem: PLL output clock occasionally skipped edges at low VCO frequencies
- Cause: VCO level-shifter had insufficient gain when VCO swing was close to V_t.
- Solutions:
  - increase W of diff-pair inputs
  - use low-V_t devices

PLL Problem

- Problem: VCO jitter was huge at some divider settings and fine at others.
- Cause: Integration team connected programmable current sources backward.
- Solution: write accurate verilog model that complains when inputs are out-of-range.

PLL Problem

- Problem: PLL jitter was poor at low freq and good at high freq.
- Cause: V_{ctl} was too close to V_t at low frequency.
- Solution: Run VCO at 2X and divide it down to generate slow clocks.

PLL Problem

- Problem: RAMDAC PLL had large accumulated phase error which showed up as jitter on CRT screen.
- Cause: PLL bandwidth was too low, allowing random VCO jitter to accumulate.
- Solution: increase bandwidth so that loop corrects before VCO jitter accumulates.

PLL Problem

- Problem: PLL had poor peak-peak jitter, but good RMS jitter.
- Cause: digital VDD pin in package adjacent to PLL's analog VDD coupled digital VDD noise to analog VDD during certain test patterns.
- Solution: Remove wirebond for adjacent digital VDD pin.

PLL Problem

- Problem: large static offset.
- Cause: designer did not account for gate leakage in LPF caps.
- Solutions:
  - switch to thick-gate oxide caps
  - switch to metal caps

PLL Problem

- Problem: VCO period jitter = +/- 20%, modulated at a fixed frequency.
- Cause: Unstable V2I internal feedback loop caused by incorrect processing of stabilizing caps.
- Solutions:
  - correct manufacturing of capacitors
  - add more caps

PLL Problem

- Problem: bandgap reference was stable in one process but oscillated in a different process with similar feature sizes.
- Cause: compensation caps for 2-pole feedback system with self-bias were too small.
- Solution: make compensation caps 3X larger.

Uncle D's PLL Top 5 List

- 5. Maintain damping factor ~ 1
- 4. VDD-induced VCO noise – loop can't do the work for you
- 3. Leaky gate caps will cost you your job
- 2. Make FBDIV run faster than VCO
- 1. Observe VCO,FBCLK,REF,clkTree on differential I/O pins – you can't fix what you can't see!

Appendices

Appendices

- Appendix A: Design for Test
- Appendix B: Writing a PLL spec
- Appendix C: Additional PLL material
- Appendix D: Paper References
- Appendix E: Monograph References

Design for Test

Design for Test Overview

- Measuring Jitter
- Analog Observation
- Probing

Measuring Jitter: Power-Supply Noise Sensitivity

- Induce noise on-chip with VDD-VSS short
  - need off-chip frequency source or on-chip FSM to control noise generator
  - How to measure induced noise magnitude?
- Induce noise on board
  - capacitively couple to VDDA
  - hard to get it past filtering and attenuation
  - how much makes it to PLL?
  - VDDA inductance? – wire-bond, flip-chip

Routing: From PLL to Board

- Differential IO outputs highly desirable
- Types of IO – use highest-speed available
- Divide VCO to reduce board attenuation only if necessary → make divider programmable
- Measuring duty-cycle
  - Divide-by-odd-integer
  - Mux to select either true or inverted clock
- Minimize delay on-chip from PLL to IO
- Ability to disable neighboring IO when measuring jitter
- Avoid coupling in package and board

General Test Hardware

- High-bandwidth scope:
  - 4-6 GHz real-time
  - $50-60k
  - e.g. Agilent, Tektronix, LeCroy
- Differential high-speed probes:
  - 3-6 GHz BW
  - $3-6k
- Active pico-probes and passive (DC) probes for micro-probing PLL
- Avoid large GND loops on probes

Jitter Hardware/Software

- Jitter Analysis tools:
  - e.g. Wavecrest, Tek(Jit2), Amherst Design
- Jitter measurement types:
  - Period jitter histogram
  - Long-term jitter
  - Cycle-to-adjacent cycle jitter
  - Half-period jitter
  - Jitter FFT - limited by Nyquist – aliasing
- Scope memory depth

Miscellaneous Jitter Measurements

- Open-loop vs. Closed-loop Jitter
  - disable loop-filter → does PLL jitter change?
- Mux *Ref* into PLL observation path for jitter calibration
  - Is *Ref* jitter worse after coming from PLL compared to before it enters the chip?
- Observe "end-of-clock tree" for jitter and duty-cycle distortion
- Observe *Fbclk* for jitter and missing edges

Measuring PLL Loop Dynamics

- Modulate reference frequency, measuring long-term PLL jitter. Sweep modulation frequency to determine bandwidth and damping.
  - e.g. Wavecrest
- Spectrum analyzer
  - look for noise suppression in frequency range close to signal peak
  - difficult if noisy setup

Measuring Phase Error

- Hard to do!
- *Fbclk* available for observation?
- Need to acct. for *Fbclk* delay from PLL to IO –depends on PVT.
- Solutions:
  - route Fbclk off-chip to pkg and match input delay with *Ref*. *Fbclk/Ref* skew at pins ~ Terr at PFD.
  - measure Terr on-chip – send out narrow pulses – narrow pulses disappear.
  - measure Terr on-chip with A/D. Complex.
  - mux Fbclk and ref into same path. Compare both to external reference.

Analog Observation

- Analog observation IO pins for debug and characterization
  - may force internal analog nets as well if bi-directional pin
  - low-bandwidth requirements → low MHz or kHz
  - isolate analog nets with unity-gain buffer or resistor and pass-gates w/solid pull-down
  - drive analog pins to known value when not in use
  - tri-state analog pin for ESD leakage testing
  - ESD protection (CDM and HBM) may cause IO leakage

Probing On-chip

- If not flip-chip, then put probe pads on top-layer metal.
- Probe pad size >1um x 1um. Prefer > 2um x 2um.
- Place probe pad on a side-branch of the analog signal to avoid breaking wire with probe.
- Separate probe pads to allow room for multiple probes.
- FIB: can add probe pad, add or remove wires.
  - need room and luck
- FIB: can FIB SOI flip-chip from back of wafer if enough room around lower-level wires.

Writing a PLL Spec

Spec Overview

- Area, physical integration
- Technology issues
- Power-supply voltage
- Performance metrics
- Logic interface

Physical Integration

- Area, aspect ratio?
- What metal layers are available?
- Digital signal routing allowed over PLL?
- Where is PLL located on chip?
- Wire-bond or flip-chip?

Semiconductor Process

- 90nm, 130nm, 180nm?
- Bulk vs. SOI? SOI body-ties?
- Nwell vs. twin-well?
- Epi substrate?
- Accumulation-mode capacitors?
- Gate-oxide thickness? Capacitance density and leakage.
- Dual-gate oxide available? Leakage.
- Poly density requirements?
- Low-V_t available?
- Resistor types? Poly? Diffusion?

Power-Supply

- Separate analog VDDA? What voltage? 1.8V? 2.5V? Higher than core voltage?
- Separate analog VSSA?
- Wire-bond or flip-chip? Package Type?
- What type of VDDA filtering on board? Ferrite bead? What cap sizes?
- Min, max VDDA? DC variation? AC variation? Natural frequency (1/LC) of VDDA?

Performance

- Reference clock frequency? Range?
- Min/Max VCO Frequency?
- Duty cycle?
- Period Jitter?
- Fixed jitter spec or pct of period?
- Cycle-to-adjacent cycle jitter spec?
- Half-cycle jitter spec?

Performance

- Max Frequency overshoot while settling?
- Static phase error?
- Dynamic phase error?
- Loop bandwidth?
- Time to acquire initial lock?
- Time to re-acquire lock after frequency change?
- Power Dissipation?

Logic Interface

- *Reset* available?
- *PowerOK* available?
- VCO/CP/R range settings allowed?
- Clock glitching allowed when switching VCO frequency ranges?
- Level-shift and buffer PLL inputs/outputs?
- Different power domains?

Example Design Specs

- f(*ref*) = 125 MHz
- 8 < *FBDiv* < 16 → 1 GHz < f(*vco*) < 2 GHz
- ζ > 0.7 – not constant w/*FBDiv*
- 1 MHz < $\omega_n/2\pi$ < f(*ref*) /20
- Pk-Pk Jitter < +/- 2.5% w/dVdd = 50mV
- T_{lock} < 10 uS
- FreqOvershoot < 15% w/1-ref-cycle phase step
- Static Phase Error < +/- 200 pS → Icp mismatch < 50%?

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