

ECE518 Memory/Clock Synchronization IC Design

Integer-N Frequency Synthesizers

Dr. Vishal Saxena

Electrical and Computer Engineering Department Boise State University, Boise, ID





General Considerations: Why Do We Need Synthesizers?



□ The synthesizer performs the precise setting of LO frequency



A slight shift leads to significant spillage of a high-power interferer in to a desired channel

Wireless Standards

Parameter	DECT	GSM	802.11
Modulation	GFSK	GFSK	GFSK
Data Rate	1.152Mbps	270.8Kbps	1-2Mbps
Frequency	1800MHz	900MHz	2.4-2.5GHz
Channels	10	124	75
Spacing	1.782MHz	200KHz	1MHz

- ➢ Difficult LO design → narrower channel spacing and stringent phase noise/spur requirements
- LO for GSM receiver is the hardest

Reciprocal Mixing



Example of Reciprocal Mixing and Intermodulation

A receiver with an IIP₃ of -15 dBm senses a desired signal and two interferers as shown in figure below. The LO also exhibits a sideband at ω_s , corrupting the downconversion. What relative LO sideband magnitude creates as much corruption as intermodulation does?



To compute the level of the resulting intermodulation product that falls into the desired channel, we write the difference between the interferer level and the IM₃ level in dB as

$$\Delta P = 2(\mathrm{IIP}_3 - P_{in})$$

 $= 50 \, \mathrm{dB}.$

(The IM₃ level is equal to -90 dBm.) Thus, if the sideband is 50 dB below the carrier, then the two mechanisms lead to equal corruptions.



The lock time is typically specified as the time required for the output frequency to reach within a certain margin around its final value

Example of Lock Time

During synthesizer settling, the power amplifier in a transmitter is turned off. Explain why.



If the power amplifier remains on, then the LO frequency variations produce large fluctuations in the transmitted carrier during the settling time. Shown in figure above, this effect can considerably corrupt other users' channels.

Basic Integer-N Synthesizer



- Integer-N synthesizer produce an output frequency that is an integer multiple of the reference frequency.
- > The choice of f_{REF} : it must be equal to the desired channel spacing and it must be the greatest common divisor of f_1 and f_2 .

Example of Reference Frequency and Divide Ratio Selection

Compute the required reference frequency and range of divide ratios for an integer-*N* synthesizer designed for a Bluetooth receiver. Consider two cases: (a) direct conversion, (b) sliding-IF downconversion with $f_{LO} = (2/3)f_{RF}$



(a)Shown in (a), the LO range extends from the center of the first channel, 2400.5 MHz, to that of the last, 2479.5 MHz. Thus, even though the channel spacing is 1 MHz, f_{REF} must be chosen equal to 500 kHz. Consequently, $N_1 = 4801$ and $N_2 = 4959$.

(b) As illustrated in (b), in this case the channel spacing and the center frequencies are multiplied by 2/3. Thus, $f_{REF} = 1/3$ MHz, $N_1 = 4801$, and $N_2 = 4959$.

Choosing N_1 and N_2

F
$$f_{ref}$$
 = 19.68MHz and f_{out} = 2.402GHz → f_{in} = 40 kHz

>
$$f_{ref} = 19.68MHz$$
 and $f_{in} = 40kHz \rightarrow N_1 = 492$

>
$$f_{in} = 40$$
kHz and $f_{out} = 2.042$ GHz → $N_2 = 60050$

- > Need programmable: 2.042GHz $\leq f_{out} \leq 2.480GHz$
- > $f_{out} = 2.480GHz + m$ MHz with 2 ≤m≤78

 \rightarrow N2 = 60050 + 25•m

Settling Behavior: Channel Switching

$$X(s) \xrightarrow{+} H(s) \xrightarrow{} Y(s)$$

$$Y(s) = \frac{H(s)}{1 + (A + \epsilon)H(s)}X(s)$$

$$\approx \frac{H(s)}{1 + AH(s)} \cdot \frac{1}{1 + \epsilon/A}X(s)$$

$$\approx \frac{H(s)}{1 + AH(s)} \left(1 - \frac{\epsilon}{A}\right)X(s)$$

we can view multiplication by $(1 - \epsilon/A)$ as a step function from f_0 to $f_0(1 - \epsilon/A)$, i.e., a frequency jump of $-(\epsilon/A)f_0$.

When the divide ratio changes, the loop responds as if an input frequency step were applied

Worst Case Settling and Example of Error



The worse case occurs when the synthesizer output frequency must go from the first channel, $N_1 f_{REF}$, to the last, $N_2 f_{REF}$, or vice versa

In synthesizer settling, the quantity of interest is the frequency error, $\Delta \omega_{out}$, with respect to the final value. Determine the transfer function from the input frequency to this error.

The error is equal to $\omega_{in}[N-H(s)]$, where H(s) is the transfer function of a type-II PLL (Chapter 9). Thus,

$$\frac{\Delta\omega_{out}}{\omega_{in}} = N \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Calculation of Settling Time

Assuming $N_2 - N_1 \ll N_1$

If the divide ratio jumps from N_1 to N_2 , this change is equivalent to an input frequency step of $\Delta \omega_{in} = (N_2 - N_1) \omega_{REF} = N_1$.

For the normalized error to fall below a certain amount, *a*, we have

Example of Settling Time Calculation

A 900-MHz GSM synthesizer operates with $f_{REF} = 200$ kHz and provides 128 channels. If $\zeta = \sqrt{2/2}$, determine the settling time required for a frequency error of 10 ppm.

The divide ratio is approximately equal to 4500 and varies by 128, i.e., $N_1 \approx 4500$ and $N_2 - N_1 = 128$. Thus,

$$t_s \approx \sqrt{2} \frac{8.3}{\omega_n} \quad \text{or} \quad t_s = \frac{8.3}{\zeta \omega_n}$$

While this relation has been derived for $\zeta = \sqrt{2/2}$, it provides a reasonable approximation for other values of ζ up to about unity. How is the value of $\zeta \omega_n$ chosen? From Chapter 9, we note that the loop time constant is roughly equal to one-tenth of the input period. It follows that $(\zeta \omega_n)-1 \approx 10T_{REF}$ and hence

$$t_s \approx 83T_{REF}$$

In practice, the settling time is longer and a rule of thumb for the settling of PLLs is 100 times the reference period.

Spur Reduction Techniques: Will Scaling Down Transistor Widths Work?

A student reasons that if the transistor widths and drain currents in a charge pump are scaled down, so is the ripple. Is that true?

Solution:

This is true because the ripple is proportional to the absolute value of the unwanted charge pump injections rather than their relative value. This reasoning, however, can lead to the wrong conclusion that scaling the CP down reduces the output sideband level. Since a reduction in I_P must be compensated by a proportional increase in K_{VCO} so as to maintain _ constant, the sideband level is almost unchanged.

Spur Reduction Techniques: Masking the Ripple by Insertion of a Switch



- V_{cont} is disturbed for a short duration (at the phase comparison instant) and remains relatively constant for the rest of the input period.
- > The arrangement of (a) leads to an unstable PLL
- Topology of (b) can yield a stable PLL

Stabilization of PLL by Adding K₁ to the Transfer Function of VCO (I)



Open-loop transfer function of a type-II second-order PLL

$$H_{open}(s) = \frac{I_P}{2\pi} \left(R_1 + \frac{1}{C_1 s} \right) \frac{K_{VCO}}{s}$$
$$H_{open}(s) = \frac{I_P}{2\pi} \frac{1}{C_1 s} \left(\frac{K_{VCO}}{s} + K_1 \right) \qquad \text{to obtain a zero?}$$
$$\phi_1 \quad (\cdot) \quad K_{VCO} + K_1$$

Can we realize:

 $\frac{1}{V_{cont}}(s) = \frac{1}{s} + K_1$ Indeed, K_1 represents a variable-delay stage having a "gain" of K_1 :

$$K_1 = \frac{\Delta T_d}{\Delta V_{cont}}$$

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Stabilization of PLL by Adding K_1 to the Transfer Function of VCO (II)



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Stabilization of PLL by Adding K₁ to the Transfer Function of VCO: Modified Architecture



A retiming flipflop can be inserted between the delay line and the PFD to remove the phase noise of the former

PLL-Based Modulation: In-Loop Modulation



- On top depicts a general case where the filter smoothes the time-domain transitions to some extent, thereby reducing the required bandwidth.
- On bottom, such a system first disables the baseband data path and enables the PLL. Next, the PLL is disabled and signal is applied to the VCO

Drawbacks of Previous Arrangement and Modification



- Architecture above requires periodic "idle" times during the communication to phase-lock the VCO
- The output signal bandwidth depends on K_{VCO}, a poorlycontrolled parameter.
- The free-running VCO frequency may shift from Nf_{REF} due to a change in its load capacitance or supply voltage

To alleviate the foregoing issues, the VCO can remain locked while sensing the baseband data

The design must select a very slow loop so that the desired phase modulation at the output is not corrected by the PLL

Calculation of Transfer Function of Previous Arrangement

It follows that

The effect of the PLL in the architecture of VCO in-loop modulation on the data can also be studied in the frequency domain. Neglecting the effect of the filter in the data path, determine the transfer function from $x_{BB}(t)$ to ϕ_{out} .

Beginning from the output, we write the feedback signal arriving at the PFD as ϕ_{out}/N , subtract it from 0 (the input phase), and multiply the result by $I_P/(2\pi)[R_1 + (C_1s)-1]$, obtaining the signal at node A. We then add X_{BB} to this signal and multiply the sum by K_{VCO}/s :

$$\begin{bmatrix} -\frac{\phi_{out}}{N} \cdot \frac{I_P}{2\pi} \left(R_1 + \frac{1}{C_1 s} \right) + X_{BB} \end{bmatrix} \frac{K_{VCO}}{s} = \phi_{out}.$$

$$\frac{\phi_{out}}{X_{BB}}(s) = \frac{K_{VCO}s}{s^2 + \frac{I_P K_{VCO} R_1}{2\pi N} s + \frac{I_P K_{VCO}}{2\pi N C_1}}$$

$$\begin{bmatrix} \frac{\phi_{out}}{x_{BB}} \end{bmatrix}_{\frac{K_{VCO}}{2\zeta \omega_n}}$$

Modulation by Offset PLLs



 \succ The noise transmitted by user C corrupts the desired signal around f_1



In direct-conversion transmitters, each stage in the signal path contributes noise, producing high output noise in the RX band even if the baseband LPF suppresses the out-of-channel DAC output noise

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Example of Noise Floor at Previous Arrangement

If the signal level is around 632 mV_{pp} (= 0 dBm in a 50- Ω system) at node X figure above, determine the maximum tolerable noise floor at this point. Assume the following stages are noiseless.

Solution:

The noise floor must be 30 dB lower than that at the PA output, i.e., -159 dBm/Hz in a 50- Ω system. Such a low level dictates very small load resistors for the upconversion mixers. In other words, it is simply impractical to maintain a sufficiently low noise floor at each point along the TX chain.

Noise Filtration by Means of a PLL



This architecture need only minimize broadband noise of one building block. But dictates the PFD and CP operate at carrier frequency



The PLL multiplies the phase by a factor of N, altering the signal bandwidth and modulation

Offset-PLL Architecture



With the loop locked, $x_1(t)$ must become a faithful replica of the reference input, thus containing no modulation. Consequently, $y_1(t)$ and $y_Q(t)$ "absorb" the modulation information of the baseband signal.

Example of Offset-PLL Architecture

If $x_{l}(t) = A\cos[\phi(t)]$ and $x_{Q}(t) = A\sin[\phi(t)]$, derive expressions for $y_{l}(t)$ and $y_{Q}(t)$.

Solution:

Centered around f_{REF} , y_I and y_Q can be respectively expressed as

$$y_I(t) = a \cos[\omega_{REF}t + \phi_y(t)]$$

$$y_Q(t) = a \sin[\omega_{REF}t + \phi_y(t)],$$

where $\omega_{REF} = 2\pi f_{REF}$ and $\Phi_y(t)$ denotes the phase modulation information. Carrying the quadrature upconversion operation and equating the result to an unmodulated tone, $x_1(t) = A\cos \omega_{REF} t$, we have

 $A_1 a \cos[\phi(t)] \cos[\omega_{REF}t + \phi_y(t)] - A_1 a \sin[\phi(t)] \sin[\omega_{REF}t + \phi_y(t)] = A \cos \omega_{REF}t.$

It follows that $A_1 a \cos[\omega_{REF}t + \phi(t) + \phi_y(t)] = A \cos \omega_{REF}t$

And hence

$$\phi_y(t) = -\phi(t)$$

Note that $x_{out}(t)$ also contains the same phase information

Another Example of Offset-PLL Architecture

In the architecture above, the PA output spectrum is centered around the VCO center frequency. Is the VCO injection-pulled by the PA?

Solution:

To the first order, it is not. This is because, unlike TX architectures studied in Chapter 4, this arrangement impresses the same modulated waveform on the VCO and the PA. In other words, the instantaneous output voltage of the PA is simply an amplified replica of that of the VCO. Thus, the leakage from the PA arrives in-phase with the VCO waveform—as if a fraction of the VCO output were fed back to the VCO. In practice, the delay through the PA introduces some phase shift, but the overall effect on the VCO is typically negligible.



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Divider Design: Requirements

- The divider modulus, N, must change in unity steps
- The first stage of the divider must operates as fast as the VCO
- The divider input capacitance and required input swing must be commensurate with the VCO drive capability
- The divider must consume low power, preferably less than the VCO



Pulse Swallow Divider



- Sensing the high-frequency input, the prescaler proves the most challenging of the three building blocks.
- As a rule of thumb, dual-modulus prescalers are about a factor of two slower than +2 circuits

Pulse Swallow Divider



- S pulses counted with a (N+1) modulus, and remaining (P-S) pulses counted with a N modulus
- Adding the total number of pulses at the prescalar input in the two modes
 (N+1)S + N(P-S) = NP + S
- Thus, for every NP+S pulse at the main input, the PC generates one pulse at the output.

Example of Preceding the Pulse Swallow Divider by a ÷2

In order to relax the speed required of the dual-modulus prescaler, the pulse swallow divider can be preceded by a +2. Explain the pros and cons of this approach.



Here, $f_{out} = 2(NP + S)f_{REF}$. Thus, a channel spacing of f_{ch} dictates $f_{REF} = f_{ch} = 2$. The lock speed and the loop bandwidth are therefore scaled down by a factor of two, making the VCO phase noise more pronounced. One advantage of this approach is that the reference sideband lies at the edge of the adjacent channel rather than in the middle of it. Mixed with little spurious energy, the sidebands can be quite larger than those in the standard architecture.

Swallow Counter Realization



The swallow counter is typically designed as an asynchronous circuit for the sake of simplicity and power saving

Modular Divider Realizing Multiple Divider Ratios



This method incorporates ÷2/3 stages in a modular form so as to reduce the design complexity. Each ÷2/3 block receives a modulus control from the next stage. The digital inputs set the overall divide ratio according to:

$$N = 2^{n} + D_{n}2^{n-1} + D_{n-1}2^{n-2} + \dots + 2D_{2} + D_{1}$$

Divide- by-3 Circuit:



Suppose the circuit begins with $Q_1 \overline{Q}_2 = 00$. next three cycles, $Q_1 \overline{Q}_2$ goes to 10, 11, and 01. Note that the state $Q_1 \overline{Q}_2 = 00$ does not occur again because it would require the previous values of \overline{Q}_2 and X to be ZERO and ONE, respectively,

Example of a +3 Circuit Using a NOR Gate rather than a AND Gate

Design a +3 circuit using a NOR gate rather than an AND gate.



We begin with the previous topology, sense the Q output of FF_2 , and add "bubbles" to compensate for the logical inversion. The inversion at the input of FF_1 can now be moved to its output and hence realized as a bubble at the corresponding input of the AND gate. Finally, the AND gate with two bubbles at its input can be replaced with a NOR gate. The reader can prove that this circuit cycles through the following three states: $Q_1Q_2 = 00$; 01; 10.
Speed Limitation of the +3 Stage

Analyze the speed limitations of the +3 stage shown in Fig. 10.28



We draw the circuit as above, explicitly showing the two latches within FF_2 . Suppose *CK* is initially low, L_1 is opaque (in the latch mode), and L_2 is transparent (in the sense mode). In other words, $\overline{\alpha_2}$ has just changed. When *CK* goes high and L_1 begins to sense, the value of Q_2 must propagate through G_1 and L_1 before *CK* can fall again. Thus, the delay of G_1 enters the critical path. Moreover, L_2 must drive the input capacitance of FF_1 , G_1 , and an output buffer. These effects degrade the speed considerably, requiring that *CK* remain high long enough for \overline{Q}_2 to propagate to *Y*.

Divide-by-2/3 Circuit



The ÷2/3 circuit employs an OR gate to permit ÷3 operation if the modulus control, MC, is low or ÷2 operation if it is high

A student seeking a low-power prescaler design surmises that FF_1 in the \div 3 circuit can be turned off when MC goes high. Explain whether this is a good idea.

While saving power, turning off FF_1 may prohibit instantaneous modulus change because when FF_1 turns on, its initial state is undefined, possibly requiring an additional clock cycle to reach the desired value. For example, the overall circuit may begin with $Q_1 \overline{Q}_2 = 00$.

Divide-by-2/3 Circuit with Higher Speed and Divideby-3/4 Circuit





When MC=ONE, the circuit divides by 4; If MC=0, it divides by 3

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Divide-by-8/9 Circuit



- For higher moduli, a synchronous core having small moduli is combined with asynchronous divider stages.
- ▶ If MC_2 is low, MC_1 is high, the overall circuit operates as a +8 circuit; if MC_2 is high, the circuit divides by 9.

Example: Design of a Divide-by-15/16 Circuit

Design a +15/16 circuit using the synchronous +3/4 stage.



Since the \div 3/4 stage (D34) divides by 4 when *MC* is high, we surmise that only two more \div 2 circuits must follow to provide \div 16. To create \div 15, we must force D34 to divide by 3 for one clock cycle. Shown in the figure above, the circuit senses the outputs of the asynchronous \div 2 stages by an OR gate and lowers *MF* when *AB* = 00. Thus, if *MC* is high, the circuit divides by 16. If *MC* is low and the \div 2 stages begin from 11, *MF* remains high and D34 divides by 4 until *AB* = 00. At this point, *MF* falls and D34 divides by 3 for one clock cycle before *A* goes high.

Potential Race Conditions



- First suppose FF_3 and FF_4 change their output state on the rising edge of their clock inputs. If MC is low, the circuit continues to divide by 16. As in (a), state 00 is skipped. The propagation delay through FF_3 and G_3 need not be less than a cycle of CK_{in}
- In the case FF₃ and FF₄ change their output state on the falling edge of their clock inputs, the ÷3/4 circuit must skip the state 00. This is in general difficult to achieve, complicating the design and demanding higher power dissipation. Thus the first choice is preferable.

Example of Choice of Prescaler Modulus

Consider the detailed view of a pulse swallow divider shown below. Identify the critical feedback path through the swallow counter.



When the ÷9 operation of the prescaler begins, the circuit has at most seven input cycles to change its modulus to 8. Thus, the last pulse generated by the prescaler in the previous ÷8 mode (just before the ÷9 mode begins) must propagate through the first ÷2 stage in the swallow counter, the subsequent logic, and the RS latch in fewer than seven input cycles.

Divider Logic Styles: True Single-Phase Clocking



When CK is high, the first stage operates as an inverter, impressing D at A and E. When CK goes low, the first stage is disabled and the second stage becomes transparent, writing A at B and C and hence making Q equal to A. The logical high at E and the logical low at B are degraded but the levels at A and C ensure proper operation of the circuit.

TSPC Divide-by-2 Circuit / Incorporating a NAND Gate





- This topology achieves relatively high speeds with low power dissipation, but, unlike CML dividers, it requires rail-torail clock swings for proper operation.
- The circuit consumes no static power and as a dynamic logic topology, the divider fails at very low clock frequencies due to the leakage of the transistors.
 - A NAND gate can be merged with the master latch.
 - In the design of TSPC circuit, one observes that wider clocked devices raises the maximum speed, but at the cost of loading the preceding stage.

TSPC Using Ratioed Logic



The first stage in figure above is not completely disabled when *CK* is low. Explain what happens if *D* changes in this mode.

Solution:

If *D* goes from low to high, *A* does not change. If *D* falls, *A* rises, but since M_4 turns off, it cannot change the state at *B*. Thus, *D* does not alter the state stored by the slave latch.

Divider Logic Styles-Current Steering Circuit



- CML operates with moderate input and output swings, and provides differential outputs and hence a natural inversion.
- The circuit above is typically designed for a single-ended output swing of R_DI_{SS} = 300mV, and the transistors are sized such that they experience complete switching with such input swings

Problem of Common-Mode Compatibility at NAND Inputs



NAND gate is preceded by two representative CML stages.

► R_T shifts the CM level of B and \overline{B} by $R_T I_{SS2}$. The addition of R_T appears simple, but now the high level of F and \overline{F} is constrained if M_5 and M_6 must not enter the triode region

Choice at Low Supply Voltages



The CML NOR/OR gate, avoid stacking. This stage operates only with singleended inputs.

Should $M_1 - M_3$ in figure above have equal widths?

One may postulate that, if both M_1 and M_2 are on, they operate as a single transistor and absorb all of I_{SS1} , i.e., W_1 and W_2 need not exceed $W_3/2$. However, the worst case occurs if only M_1 or M_2 is on. Thus, for either transistor to "overcome" M_3 , we require that $W_1 = W_2 \ge W_3$.

CML XOR Implementation



While lending itself to low supply voltage, this topology senses each of the inputs in single-ended form, facing issues similar to those of the NOR gate.

Speed Attributes of CML Latch



Speed advantage of CML circuits is especially pronounced in latches.

► The latch operates properly even with a limited bandwidth at X and Y if (a) in the sense mode V_X and V_Y begin from their full levels and cross, and (b) in the latch mode, the initial difference between V_X and V_Y can be amplified to a final value of $I_{SS}R_D$

Example to Formulate Regenerative Amplification (I)

Formulate the regenerative amplification of the above circuit in regeneration mode if V_x - V_y begins with an initial value of V_{xyo} .



If V_{XY0} is small, M_3 and M_4 are near equilibrium and the small-signal equivalent circuit can be constructed as shown above. Here, C_D represents the total capacitance seen at X and Y to ground, including $C_{GD1} + C_{DB1} + C_{GS3} + C_{DB3} + 4C_{GD3}$ and the input capacitance of the next stage. The gate-drain capacitance is multiplied by a factor of 4 because it arises from both M_3 and M_4 and it is driven by differential voltages. Writing a KCL at node X gives

$$\frac{V_X}{R_D} + C_D \frac{dV_X}{dt} + g_{m3,4} V_Y = 0$$

Example to Formulate Regenerative Amplification (II)

Similarly,
$$\frac{V_Y}{R_D} + C_D \frac{dV_Y}{dt} + g_{m3,4}V_X = 0$$



Subtracting and grouping the terms, we have

$$-R_D C_D \frac{d(V_X - V_Y)}{dt} = (1 - g_{m3,4} R_D)(V_X - V_Y)$$

We denote $V_X - V_Y$ by V_{XY} , divide both sides by $-R_D C_D V_{XY}$, multiply both sides by dt, and integrate with the initial condition V_{XY} (t = 0) = V_{XY0} . Thus,

$$V_{XY} = V_{XY0} \exp \frac{(g_{m3,4}R_D - 1)t}{R_D C_D}$$

Interestingly, V_{XY} grows exponentially with time, exhibiting a "regeneration time constant" of $\tau_{rea} = \frac{R_D C_D}{T_{rea}}$

$$\overline{r_{reg}} = \frac{R_D \otimes D}{g_{m3,4}R_D - 1}$$

Of course, as V_{XY} increases, one transistor begins to turn off and its g_m falls toward zero. Note that, if $g_{m3,4}R_D >> 1$, then $\tau_{reg} \approx C_D/g_{m3,4}$.

Example to Derive Relation Between Circuit Parameters and Clock Period

Suppose the *D* latch of the CML latch must run with a minimum clock period of T_{ck} , spending half of the period in each mode. Derive a relation between the circuit parameters and T_{ck} . Assume the swings in the latch mode must reach at least 90% of their final value.

Initial voltage difference

$$V_{XY0} = 0.9I_{SS}R_D \exp{rac{0.5T_{ck}}{ au_{reg}}}$$

The minimum initial voltage must be established by the input differential pair in the sense mode [just before t = t3]. In the worst case, when the sense mode begins, V_X and V_Y are at the opposite extremes and must cross and reach V_{XY0} in $0.5T_{ck}$ seconds. For example, V_Y begins at V_{DD} and falls according to

$$V_{Y}(t) = V_{DD} - I_{SS}R_{D} \left(1 - \exp \frac{-t}{R_{D}C_{D}}\right)$$

$$V_{Z}(t) = V_{DD} - I_{SS}R_{D} \exp \frac{-t}{R_{D}C_{D}}$$

$$V_{DD} - I_{SS}R_{D} \left(1 - \exp \frac{-t}{R_{D}C_{D}}\right)$$

$$V_{DD} - I_{SS}R_{D} \left(1 - \exp \frac{-t}{R_{D}C_{D}}\right)$$

$$V_{DD} - I_{SS}R_{D} \left(1 - \exp \frac{-t}{R_{D}C_{D}}\right)$$

$$V_{Z}(t) = V_{DD} - I_{SS}R_{D} \exp \frac{-t}{R_{D}C_{D}}$$

$$CK$$

$$T_{CK} = T_{CK}$$

$$T_{CK}$$

Merging Logic with Latch



It is possible to merge logic with a latch, thus reducing both the delay and the power dissipation. For example, the NOR and the master latch of *FF₁* depicted in previous high-speed divide-by-2/3 circuit can be realized as shown above. The circuit performs a NOR/OR operation on *A* and *B* in the sense mode, and stores the result in the latch mode.

Design Procedure



(1)Select I_{SS} based on the power budget (2)Select $R_D I_{SS} \approx 300 \text{mV}$ (3)Select $(W/L)_{1,2}$ such that the diff. pair experiences nearly complete switching for a diff. input of 300mV (4)Select $(W/L)_{3,4}$ so that small-signal gain around regenerative loop exceeds unity (5)Select $(W/L)_{5,6}$ such that the clocked pair steers most of the tail current with the specified clock swing

Example of the Sensitivity of the +2 Circuit (I)

The performance of high-speed dividers is typically characterized by plotting the minimum required clock voltage swing ("sensitivity") as a function of the clock frequency. Sketch the sensitivity for the ÷ 2 circuit of the figure above.



For a clock with abrupt edges, we expect the required clock swing to remain relatively constant up to the point where the internal time constants begin to manifest themselves. Beyond this point, the required swing must increase. The overall behavior, however, appears as shown in figure above. Interestingly, the required clock swing falls to zero at some frequency, f_1 . Since for zero input swings, I_{SS} is simply split equally between M_5 and M_6 in figure above, the circuit reduces to that depicted in the figure below. We recognize that the result resembles a two-stage ring oscillator. In other words, in the absence of an input clock, the circuit simply oscillates at a frequency of $f_1/2$.

Example of the Sensitivity of the +2 Circuit (II)



This observation provides another perspective on the operation of the divider: the circuit behaves as an oscillator that is injection-locked to the input clock. This viewpoint also explains why the clock swing cannot be arbitrarily small at low frequencies. Even with square clock waveforms, a small swing fails to steer all of the tail current, thereby keeping M_2 - M_3 and M_3 - M_4 simultaneously on. The circuit may therefore oscillate at $f_1/2$ (or injection-pulled by the clock).

The "self-oscillation" of the divider also proves helpful in the design process: if the choice of device dimensions does not allow self-oscillation, then the divider fails to operate properly. We thus first test the circuit with a zero clock swing to ensure that it oscillates.

Class-AB Latch



- The bias of the clocked pair is defined by a current mirror and the clock is coupled capacitively.
- > Large clock swings allow transistors M_5 and M_6 to operate in the class AB mode, i.e., their peak current well exceed their bias current. This attribute improves the speed of the divider.

Example of Choosing Coupling Capacitance

A student designs a VCO with relatively large swings to minimize relative phase noise and a CML ÷ 2 circuit that requires only moderate clock swings. How should the coupling capacitors be chosen?



Suppose the VCO output swing is twice that required by the divider. We simply choose each coupling capacitor to be equal to the input capacitance of the divider. This minimizes the size of the coupling capacitors, the load capacitance seen by the VCO (half of the divider input capacitance), and the effect of divider input capacitance variation on the VCO.

CML Using Inductive Peaking



Example of Inductive Peaking

What is the minimum tolerable value of ζ if the frequency response must exhibit no peaking?

Solution:

Peaking occurs if the magnitude of the transfer function reaches a local maximum at some frequency. Taking the derivative of the magnitude squared of the transfer function with respect to ω and setting the result to zero, we have

$$\omega^4 + 8\zeta^2 \omega_n^2 \omega^2 + [4\zeta^2 (4\zeta^2 - 2) - 1]\omega_n^4 = 0$$

A solution exists if

$$-4\zeta^2 + \sqrt{8\zeta^2 + 1} \ge 0$$

And hence if

$$\zeta \geq \sqrt{\frac{1+\sqrt{2}}{4}} \approx 0.78$$

 $\omega_{-3dB} \leq 1$

This bound on ζ translates to

1.73

Series Peaking



The -3 dB bandwidth is computed as

$$\omega_{-3dB}^2 = \left[-(2\zeta^2 - 1) + \sqrt{(2\zeta^2 - 1)^2 + 1} \right] \omega_n^2,$$

Series peaking increases the bandwidth by about 40%

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Example of Series Peaking

Having understood shunt peaking intuitively, a student reasons that series peaking degrades the bandwidth because, at high frequencies, inductor L_D in figure above impedes the flow of current, forcing a larger fraction of I_{in} to flow through C_D . Since a smaller current flows though L_D and R_D , V_{out} falls at higher frequencies. Explain the flaw in this argument.



Let us study the behavior of the circuit at $\omega_n = 1/\sqrt{L_D C_D}$. As shown above, the Thevenin equivalent of I_{in} , C_D , and L_D is constructed by noting that (a) the open-circuit output voltage is equal to $I_{in}/(C_D s)$, and (b) the output impedance (with I_{in} set to zero) is zero because C_D and L_D resonate at ω_n . It follows that $V_{out} = I_{in} = (C_D s)$ at $\omega = \omega_n$, i.e., as if the circuit consisted of only I_{in} and C_D . Since I_{in} appears to flow entirely through C_D , it yields a larger magnitude for V_{out} than if it must split between C_D and R_D .

Series Peaking Circuit Driving Load Capacitance



Compared to shunt peaking, series peaking typically requires a smaller inductor value



As the value of L_D becomes large enough, the circuit begins to fail at low frequencies. This is because the circuit approaches a quadrature LC oscillator that is injection-locked to the input clock

Miller Divider



- If the required speed exceeds that provided by CML circuits, one can consider the "Miller divider", also known as the "dynamic divider"
- The Miller divider can achieve high speeds for two reasons: (1) the low-pass behavior can simply be due to the intrinsic time constant at the output node of the mixer and (2) the circuit does not rely on latching and hence fails more gradually than flipflops as the input frequency increases

Example of Miller Divider with Feedback

Is it possible to construct a Miller divider by returning the output to the LO port of the mixer?



Shown above, such a topology senses the input at the RF port of the mixer. (Strangely enough, M_3 and M_4 now appear as diode-connected devices.) We will see below that this circuit fails to divide.

Why the Component at 3*f_{in}*/2 Must be Sufficiently Small?



This sum exhibits additional zero crossings, prohibiting frequency division if traveling through the LPF unchanged.

Example of Miller Divider Using First-order Low-pass Filter

Does the arrangement shown below operate as a divider?

Since the voltage drop across R_1 is equal to $R_1C_1dV_{out}/dt$, we have $V_x = R_1C_1dV_{out}/dt + V_{out}$ Also, $V_X = \alpha V_{in} V_{out}$ If $V_{in} = V_0 \cos \omega_{in} t$, then

$$R_1 C_1 \frac{dV_{out}}{dt} + V_{out} = \alpha (V_0 \cos \omega_{in} t) V_{out}$$

It follows that

$$R_1 C_1 \frac{dV_{out}}{V_{out}} = (\alpha V_0 \cos \omega_{in} t - 1)dt$$

We integrate the left-hand side from V_{outo} (initial condition at the output) to V_{out} and the right-hand side from 0 to t: τZ 1

hus
$$R_1 C_1 \ln \frac{V_{out}}{V_{out0}} = \frac{1}{\omega_{in}} \alpha V_0 \sin \omega_{in} t - t$$
$$V_{out}(t) = V_{out0} \exp \left(\frac{-t}{R_1 C_1} + \frac{\alpha V_0}{R_1 C_1 \omega_{in}} \sin \omega_{in} t\right)$$

т

Interestingly, the exponential term drives the output to zero regardless of the values of α or ω_{in} . The circuit fails because a one-pole filter does not sufficiently attenuate the third harmonic with respect to the first harmonic. An important corollary of this analysis is that the topology of Miller divider with feedback to switching quad cannot divide: the single-pole loop does not adequately suppress the third harmonic at the output.

Introducing Phase Shift in Miller Divider



The Miller divider operates properly if the third harmonic is attenuated and shifted so as to avoid the additional zero crossings.

Miller Divider with Inductive Load



The input frequency range across which the circuit operates properly is given by

$$\Delta\omega = \frac{2\omega_0}{Q} \left(\frac{2}{\pi}g_{m1,2}R_p\right)^2$$

If the load resistors are replaced with inductors, the gain-headroom and gain-speed trade-offs are greatly relaxed, but the lower end of the frequency range rises. Also the inductor complicates the layout.

Example of Miller Divider with Inductive Loads

Does the previous Miller divider with feedback to switching quad operate as a divider if the load resistors are replaced with inductors?



Depicted above left, such an arrangement in fact resembles an oscillator. Redrawing the circuit as shown right, we note M_5 and M_6 act as a cross-coupled pair and M_3 and M_4 as diode-connected devices. In other words, the oscillator consisting of M_5 - M_6 and L_1 - L_2 is heavily loaded by M_3 - M_4 , failing to oscillate (unless the Q of the tank is infinite or M_3 and M_4 are weaker than M_5 and M_6). This configuration does operate as a divider but across a narrower frequency range.
Miller Divider with Passive Mixers



Since the output CM level is near V_{DD}, the feedback path incorporates capacitive coupling, allowing the sources and drains of M₁-M₄ to remain about 0.4V above the ground. The cross-coupled pair M₇-M₈ can be added to increase the gain by virtue of its negative resistance.

Miller Divider with Other Moduli



A $\div N$ circuit in the feedback path creates $f_b = f_{out}/N$, yielding $f_{in} \pm f_{out}/N$ at X. If the sum is suppressed by the LPF, then $f_{out} = f_{in} - f_{out}/N$ and hence

$$f_{out} = \frac{N}{N+1} f_{in} \qquad f_b = \frac{1}{N+1} f_{in}$$

- The sum component at X comes closer to the difference component as N increases, dictating a sharper LPF roll-off.
- Another critical issue relates to the port-to-port feedthroughs of the mixer

Example of Effect of Feedthrough

Assume N = 2 in figure above and study the effect of feedthrough from each input port of the mixer to its output.



Figure above shows the circuit. The feedthrough from the main input to node X produces a spur at f_{in} . Similarly, the feedthrough from Y to X creates a component at $f_{in}/3$. The output therefore contains two spurs around the desired frequency. Interestingly, the signal at Y exhibits no spurs: as the spectrum of figure above travels through the divider, the main frequency component is divided while the spurs maintain their spacing with respect to the carrier (Chapter 9). Shown above on right the spectrum at Y contains only harmonics and a dc offset. The reader can prove that these results are valid for any value of *N*.

Miller Divider Using SSB Mixer



- The Miller divider frequency range can be extended through the use of a single-sideband mixer. But this approach requires a broadband 90°phase shift, a very difficult design.
- The use of SSB mixing prove useful if the loop contains a divider that generates quadrature outputs. Topology in (b) achieves a wide frequency range and generates quadrature outputs. But it requires quadrature LO phases.

Injection-Locked Dividers



- Based on oscillators that are injectionlocked to a harmonic of their oscillation frequency
- If f_{in} varies across a certain "lock range", the oscillator remains injection-locked to the f_{out} - f_{in} component at node X

Determine the divide ratio of the topology shown below if the oscillator remains locked.

The mixer yields two components at node X, namely, $f_{in} - f_{out}/N$ and $f_{in} + f_{out}/N$. If the oscillator locks to the former, then $f_{in} - f_{out}/N = f_{out}$ and hence

$$f_{out} = \frac{N}{N+1} f_{in}$$

 ΛT

Similarly, if the oscillator locks to the latter then

$$f_{out} = \frac{N}{N-1} f_{in}$$



The oscillator lock range must therefore be narrow enough to lock to only one of the two components.

Implementation of ILD



The output frequency range across which the circuit remains locked is given by

$$\Delta \omega_{out} = \frac{\omega_0}{Q} \left(\frac{2}{\pi} \frac{I_{in}}{I_{osc}} \right)$$

The input lock range is twice this value:

$$\Delta\omega_{in} = \frac{\omega_0}{Q} \left(\frac{4}{\pi} \frac{I_{in}}{I_{osc}}\right)$$

Divider Delay and Phase Noise: Effect of Divider Delay



The zero has two undesirable effects: it flattens the gain, pushing the gain crossover frequency to higher values (in principle, infinity), and it bends the phase profile downward.

This zero must remain well above the original
unity-gain bandwidth of the loop:
$$\frac{1}{\Delta T}$$
 \approx $5\omega_u$ \approx $5(2\zeta^2 + \sqrt{4\zeta^4 + 1})\omega_n^2$ \otimes Vishal Saxena-79-

Effect of Divider Phase Noise



> The output phase noise of the divider directly adds to the input phase noise, experiencing the same low-pass response as it propagates to ϕ_{out} . In other words, $\phi_{n,div}$ is also multiplied by a factor of N within the loop bandwidth.

For the divider to contribute negligible phase noise, we must have

$$\phi_{n,div} \ll \phi_{n,in}$$

Use of Retiming FF to Remove Divider Phase Noise



If the divider phase noise is significant, a retiming flipflop can be used to suppress its effect.

In essence, the retiming operation bypasses the phase noise accumulated in the divider chain.

Examples of Retiming to Remove Divider Phase Noise

Compare the output phase noise of the above circuit with that of a similar loop that employs noiseless dividers and no retiming flipflop. Consider only the input phase noise.

Solution:

The phase noise is similar. Invoking the time-domain view, we note that a (slow) displacement of the input edges by ΔT seconds still requires that the edges at Y be displaced by ΔT , which is possible only if the VCO edges are shifted by the same amount.

Does the retiming operation in figure above remove the effect of the divider delay?

Solution:

No, it does not. An edge entering the divider still takes a certain amount of time before it appears at X and hence at Y. In fact, figure above indicates that V_Y is delayed with respect to V_X by at most one VCO cycle. That is, the overall feedback delay is slightly longer in this case.

Integer-N Synthesis Drawbacks

- Improved resolution always comes at the expense of reduced update rate (ii.e. lower f_{ref})
- ► Lower update rate →lower bandwidth
- Larger contribution of the VCO phase noise → larger power
- ► Large settling time → increase channel switching times
- Need: Large bandwidth and fine frequency resolution
 - Fractional-N Synthesis

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