



ECE518 Memory/Clock Synchronization IC Design

Fractional-N Frequency Synthesizers

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Outline

Randomization and Noise Shaping

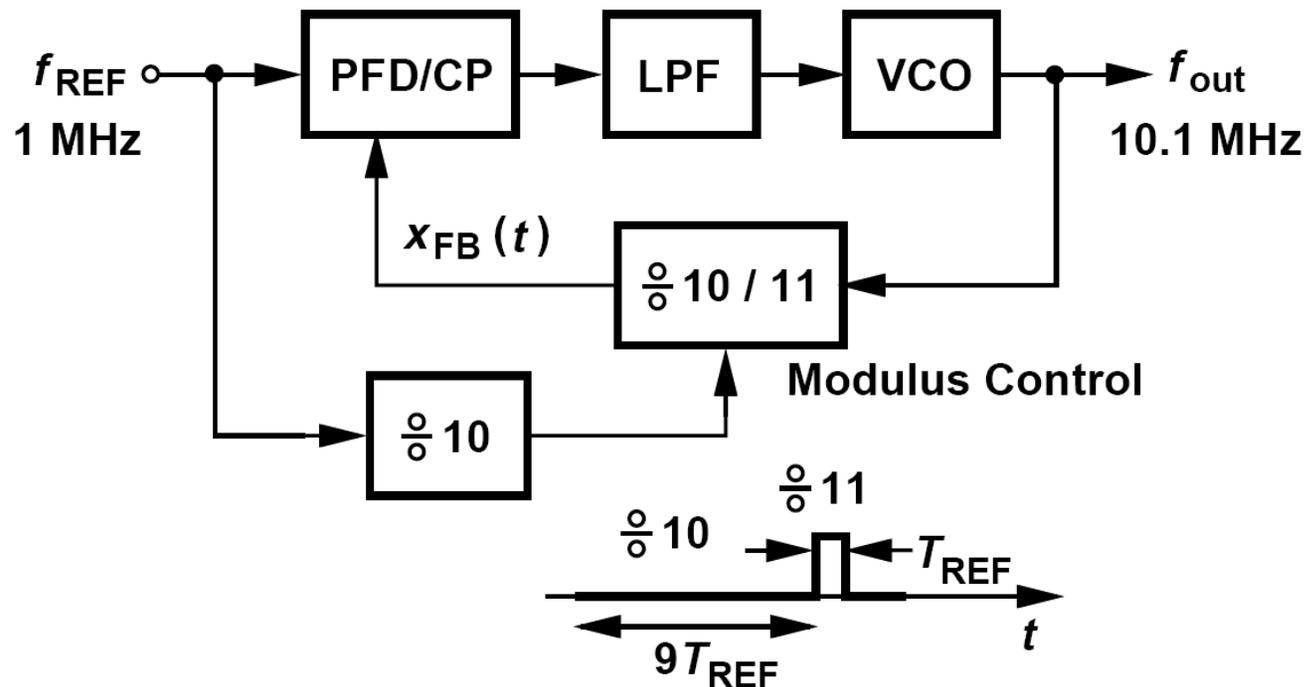
- ✓ Modulus Randomization
- ✓ Basic Noise Shaping
- ✓ Higher-Order Noise Shaping
- ✓ Out-of-Band Noise
- ✓ Charge Pump Mismatch



Quantization Noise Reduction

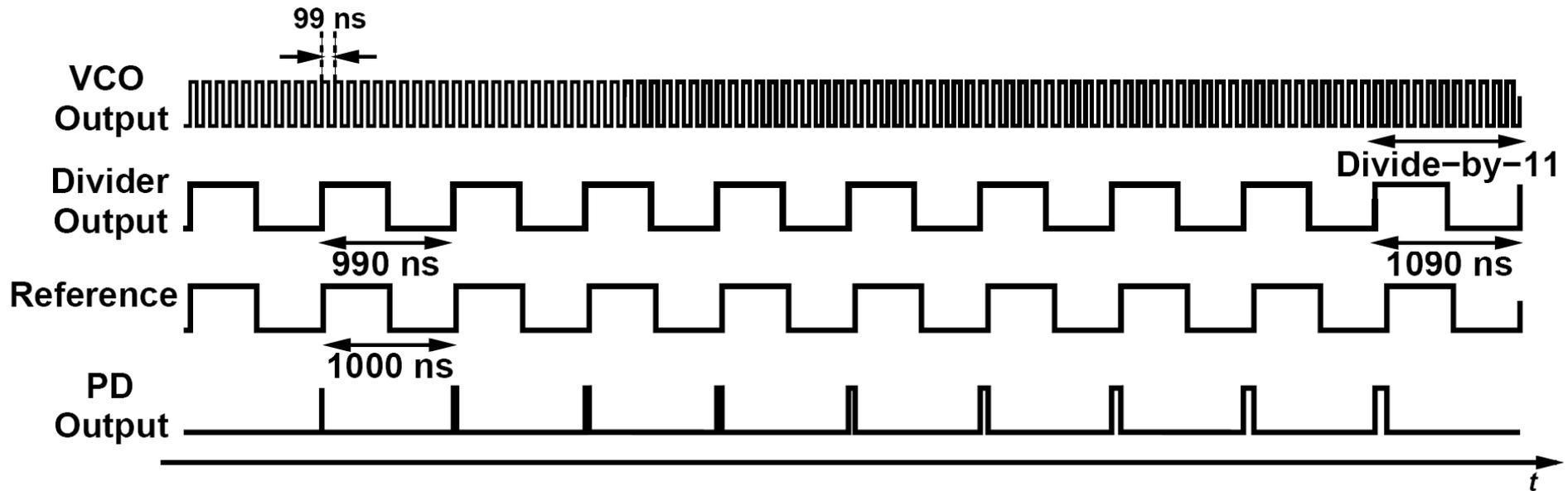
- ✓ DAC Feedforward
- ✓ Fractional Divider
- ✓ Reference Doubling
- ✓ Multi-Phase Division

Basic Concepts: Example of Fractional-N Loop



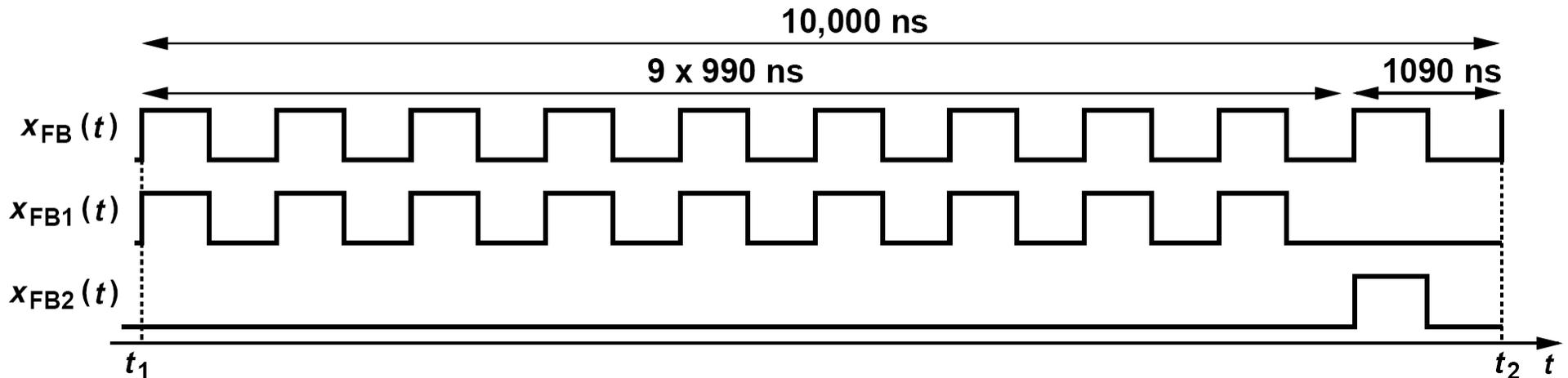
- We expect to obtain other fractional ratios between N and $N+1$ by simply changing the percentage of the time during which the divider divides by N or $N+1$
- In addition to a wider loop bandwidth than that of integer- N architectures, this approach also reduces the inband “amplification” of the reference phase noise because it requires a smaller N .

Fraction Spurs



- In above example, VCO is modulated at a rate of 0.1MHz and producing sidebands at $\pm 0.1\text{MHz} \times n$ around 10.1MHz, where n denotes the harmonic number. These sidebands are called *fractional spurs*.
- For a nominal output frequency of $(N+\alpha)f_{REF}$, the LPF output exhibits a repetitive waveform with a period of $1/(\alpha f_{REF})$

Fraction Spurs: Another Perspective



- The overall feedback signal, $x_{FB}(t)$ can be written as the sum of two waveforms, each of which repeat every 10,000 ns. The first waveform consists of nine periods of 990 ns and a “dead” time of 1090 ns, while the second is simply a pulse of width 1090/2 ns. Since each waveform repeats every 10,000 ns, its Fourier series consists of only harmonics at 0.1 MHz, 0.2 MHz, etc.
- The sidebands can be considered FM (and AM) components, leading to periodic phase modulation:

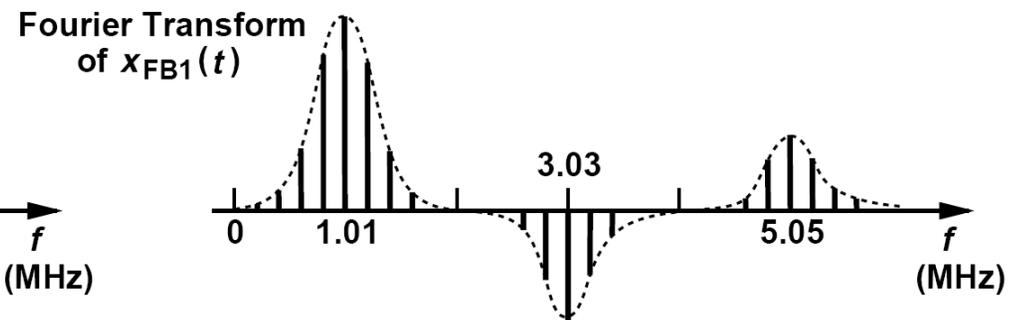
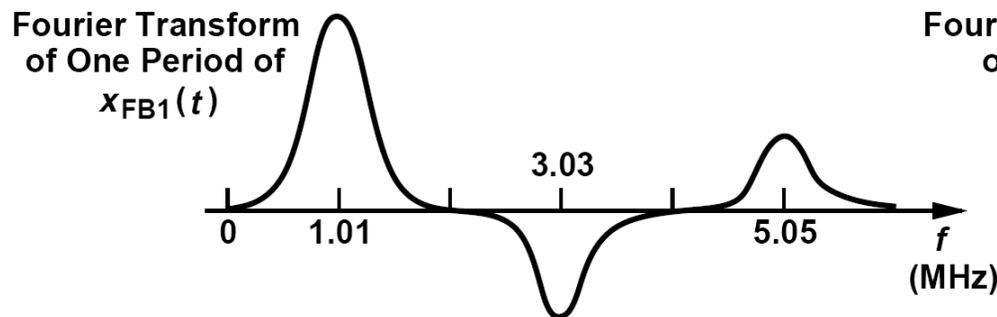
$$x_{FB}(t) \approx A \cos[\omega_{REF}t + \phi(t)]$$

Example: Spectrum of Fractional Spur

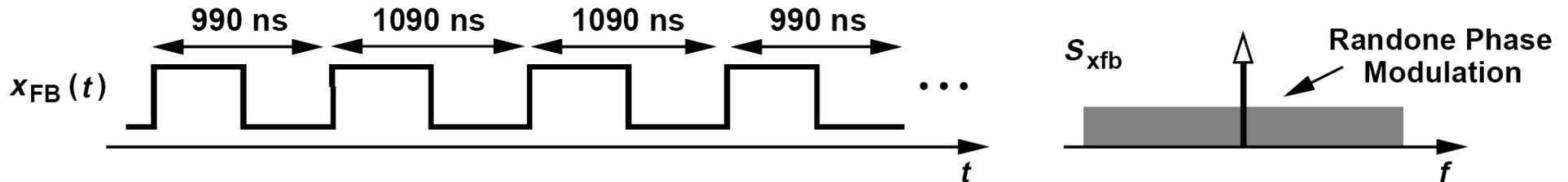
Determine the spectrum of $x_{FB1}(t)$ in figure below.

Solution:

Let us first find the Fourier transform of one period of the waveform (from t_1 to t_2). This waveform consists of nine 990-ns cycles. If we had an infinite number of such cycles, the Fourier transform would contain only harmonics of 1.01 MHz. With nine cycles, the energy is spread out of the impulses. If this waveform is repeated every 10 μ s, its Fourier transform is multiplied by a train of impulses located at integer multiples of 0.1 MHz. The spectrum thus appears as shown in figure below.



Randomization and Noise Shaping: Modulus Randomization



$x_{FB}(t)$ exhibits a random sequence of 990-ns and 1090-ns periods

$x_{FB}(t)$ now contains random phase modulation:

$$x_{FB}(t) = A \cos[\omega_{REF}t + \phi_n(t)]$$

The modulus breaks the periodicity in the loop behavior, converting the deterministic sidebands to *noise*

The instantaneous frequency of the feedback signal is therefore expressed as:

$$f_{FB}(t) = \frac{f_{out}}{N + b(t)}$$

where $b(t)$ randomly assumes a value of 0 or 1 and has an average value of α

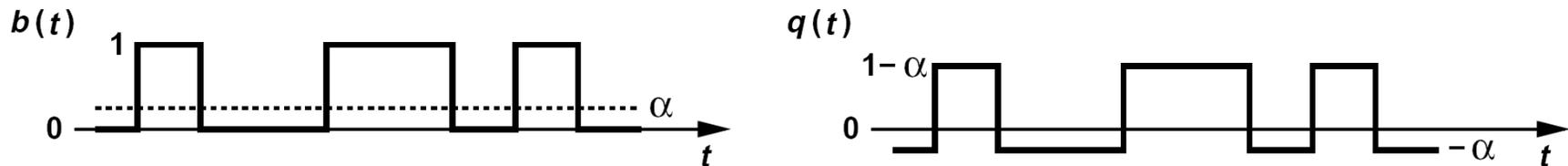
In terms of its mean and another random variable with a zero mean:

$$b(t) = \alpha + q(t)$$

More about Randomization

Plot $b(t)$ and $q(t)$ as a function of time.

The sequence $b(t)$ contains an occasional square pulse so that the average is α . Subtracting α from $b(t)$ yields the noise waveform, $q(t)$.



If $q(t) \ll N + \alpha$, we have

$$f_{FB}(t) = \frac{f_{out}}{N + \alpha + q(t)} \approx \frac{f_{out}}{N + \alpha} \left[1 - \frac{q(t)}{N + \alpha} \right] \approx \frac{f_{out}}{N + \alpha} - \frac{f_{out}}{(N + \alpha)^2} q(t)$$

The feedback waveform arriving at the PFD

$$V_{FB}(t) \approx V_0 \cos \left[\frac{2\pi f_{out}}{N + \alpha} t - \frac{2\pi f_{out}}{(N + \alpha)^2} \int q(t) dt \right]$$

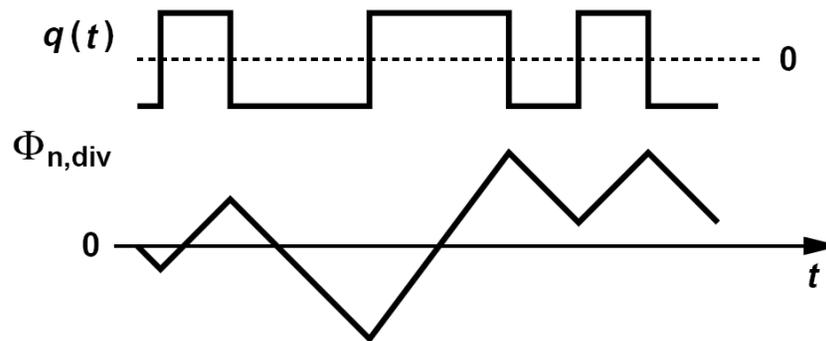
Phase noise given by:

$$\phi_{n,div}(t) = -\frac{2\pi f_{out}}{(N + \alpha)^2} \int q(t) dt$$

More Examples of Phase Noise

Plot the previous formulated phase noise a function of time.

With the aid of the wave form obtained last Example for $q(t)$, we arrive at the random triangular waveform shown below:



Determine the spectrum of $\phi_{n,div}(t)$.

The time integral of a function leads to a factor of $1/s$ in the frequency domain. Thus, the power spectral density of $q(t)$ must be multiplied by $[2\pi f_{out}/(N + \alpha)]^2$,

$$\overline{\phi_{n,div}^2}(f) = \frac{1}{(N + \alpha)^4} \left(\frac{f_{out}}{f} \right)^2 S_q(f)$$

where $S_q(f)$ is the spectrum of the quantization noise, $q(t)$. Note that this noise can be “referred” to the other PFD input—as if it existed in the reference waveform rather than the divider output.

Synthesizer Output Phase Noise within the Loop Bandwidth

$$\overline{\phi_{n,out}^2} = \left[\frac{f_{out}}{(N + \alpha)f} \right]^2 S_q(f)$$

Alternatively, since $f_{out} = (N + \alpha)f_{REF}$

$$\overline{\phi_{n,out}^2} = \left(\frac{f_{REF}}{f} \right)^2 S_q(f)$$

Compute $S_q(f)$ if $b(t)$ consists of square pulses of width T_b that randomly repeat at a rate of $1/T_b$

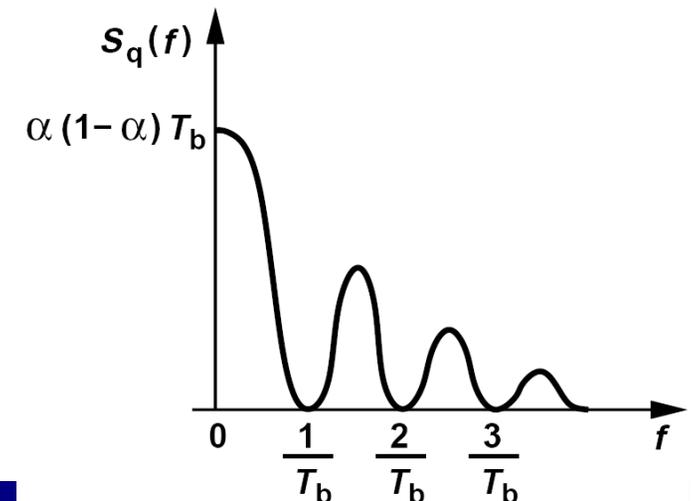
We first determine the spectrum of $b(t)$, $S_b(f)$. As shown in Appendix I, $S_b(f)$ is given by:

$$S_b(f) = \frac{\alpha(1 - \alpha)}{T_b} \left(\frac{\sin \pi T_b f}{\pi f} \right)^2 + \alpha^2 \delta(f).$$

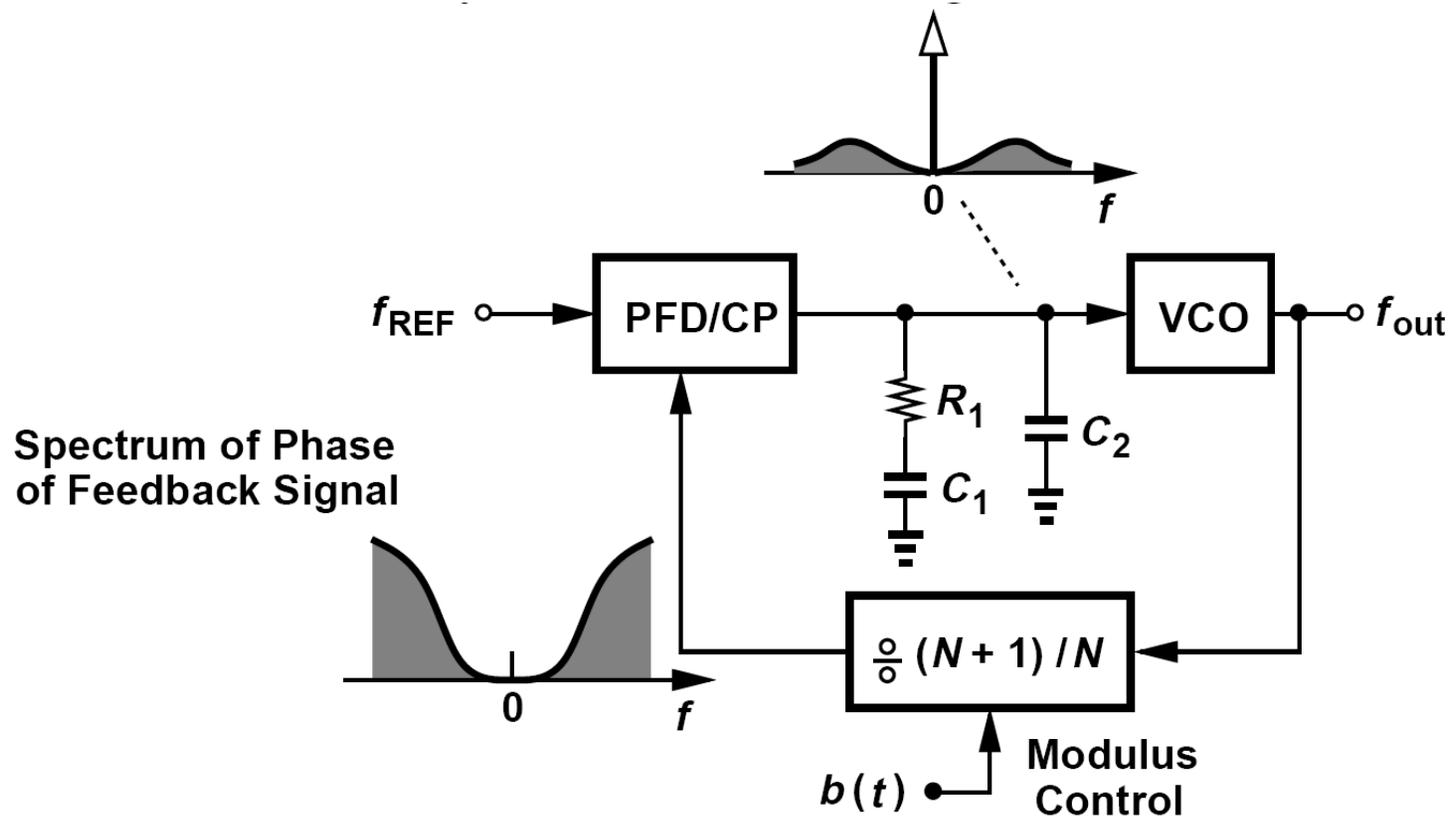
where the second term signifies the dc content. Thus,

$$S_q(f) = \frac{\alpha(1 - \alpha)}{T_b} \left(\frac{\sin \pi T_b f}{\pi f} \right)^2$$

revealing a main “lobe” between $f = 0$ and $f = 1/T_b$

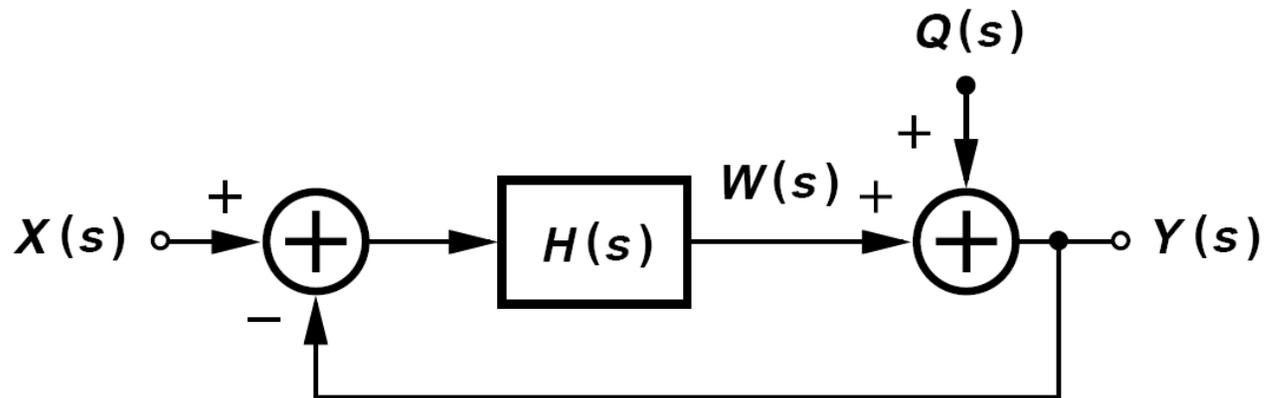


Basic Noise Shaping: Randomization Resulting in High-Pass Phase Noise Spectrum



- We wish to generate a random binary sequence, $b(t)$, that switches the divider modulus between N and $N+1$ such that (1) the average value of the sequence is α , and (2) the noise of the sequence exhibits a high-pass spectrum.

Negative Feedback System as a High-Pass System



$$\frac{Y(s)}{Q(s)} = \frac{1}{1 + H(s)}$$

$$\frac{Y(s)}{Q(s)} = \frac{s}{s + 1}$$

If $H(s)$ is an ideal integrator

- A negative feedback loop containing an integrator acts as a high-pass system on the noise injected “near” the output. If Q varies slowly with time, then the loop gain is large, making W a close replica of Q and hence Y small.

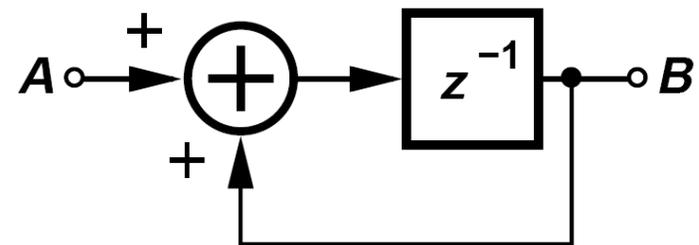
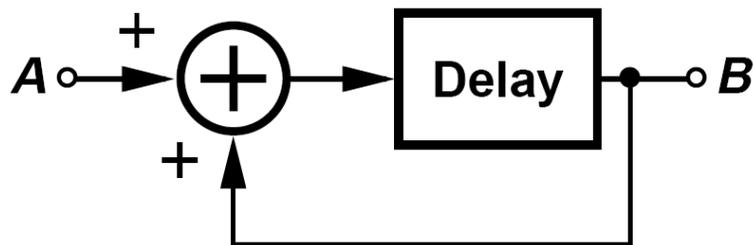
Example of a Discrete-Time Version of Previous System (I)

Construct a discrete-time version of the system shown in the previous slide if H must operate as an integrator

Solution:

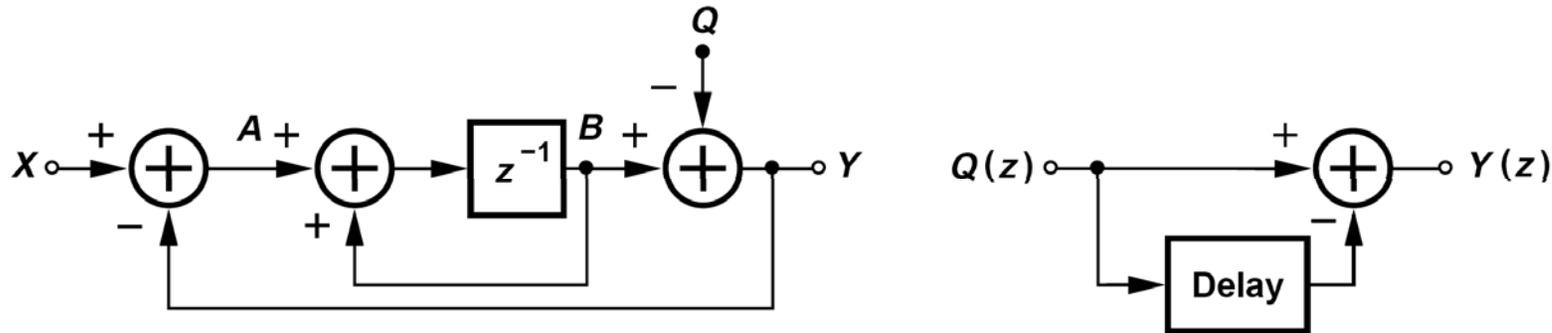
Discrete-time integration can be realized by *delaying* the signal and adding the result to itself. We observe that if, for example, $A = 1$, then the output continues to rise in unity increments in each clock cycle. Since the z -transform of a single-clock delay is equal to z^{-1} , we draw the integrator as shown below and express the integrator transfer function as

$$\frac{B}{A}(z) = \frac{z^{-1}}{1 - z^{-1}}$$



Example of a Discrete-Time Version of Previous System (II)

Construct a discrete-time version of the system shown in the previous slide if H must operate as an integrator



Thus, the discrete-time version of the system appears as shown above. Here, if $Q = 0$, then

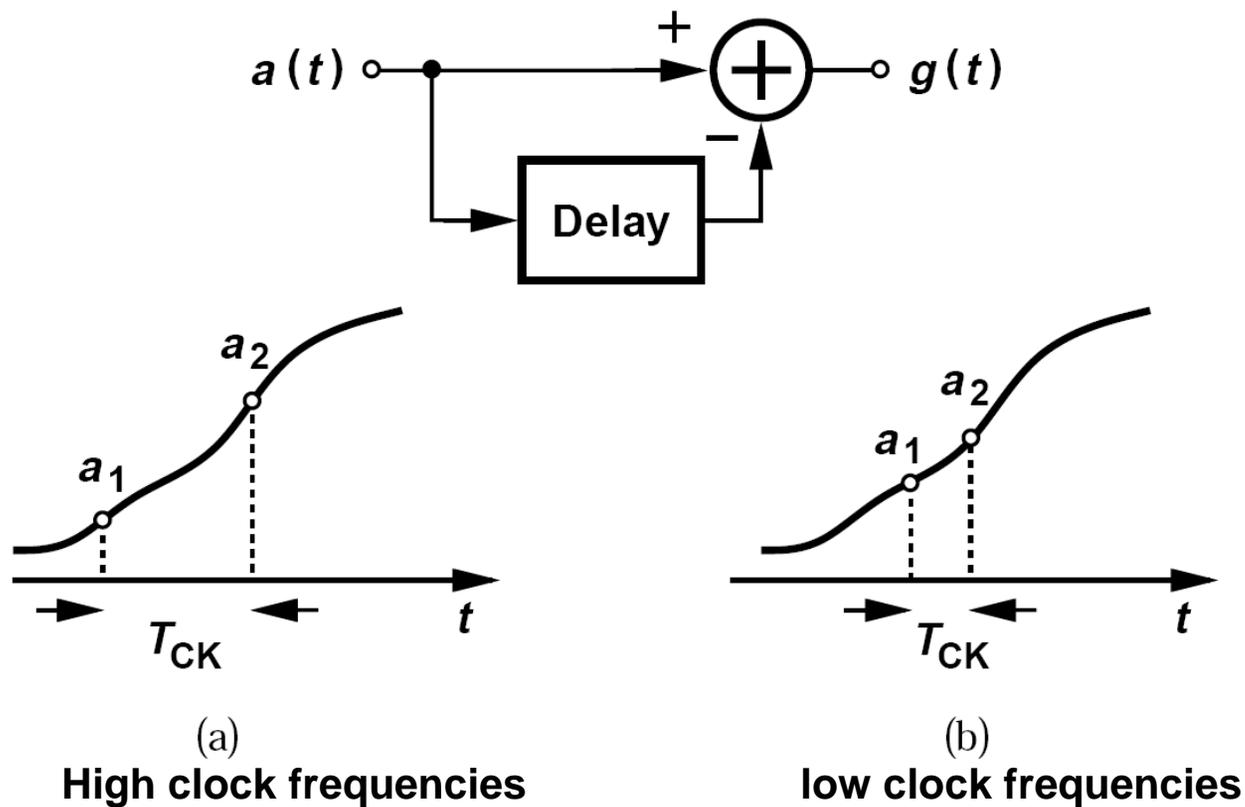
$$\frac{Y}{X}(z) = z^{-1}$$

i.e., the output simply tracks the input with a delay. Also, if $X = 0$, then

$$\frac{Y}{Q}(z) = 1 - z^{-1}$$

This is a high-pass response (that of a differentiator) because subtracting the delayed version of a signal from the signal yields a small output if the signal does not change significantly during the delay.

Addition of a Signal and Its Delayed Version for High and Low Clock Frequencies

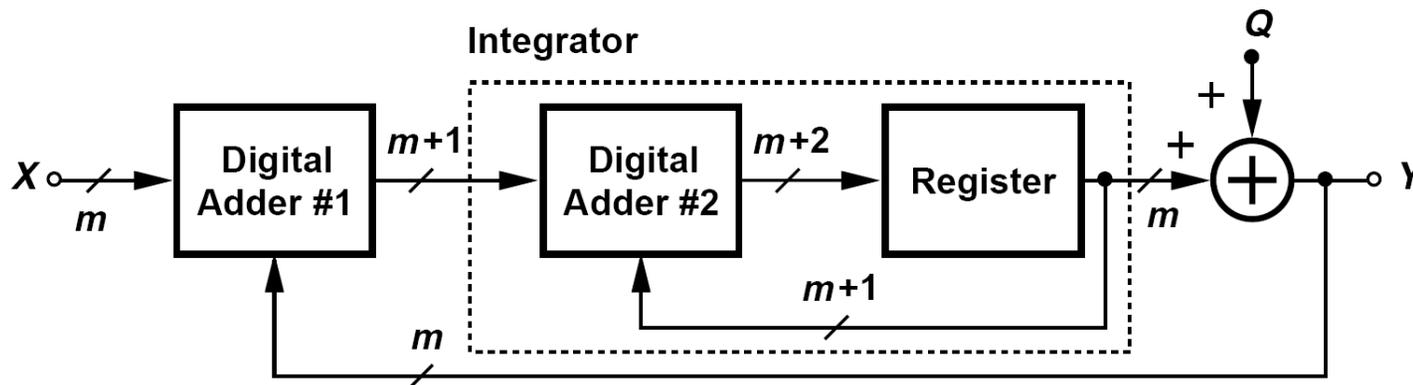


- If the clock frequency increases, $a(t)$ finds less time to change, and a_1 and a_2 exhibit a small difference.

Example of Feedback System with an m -bit Input

Construct the system in the previous example in the digital domain with a precision (word length) of m bits.

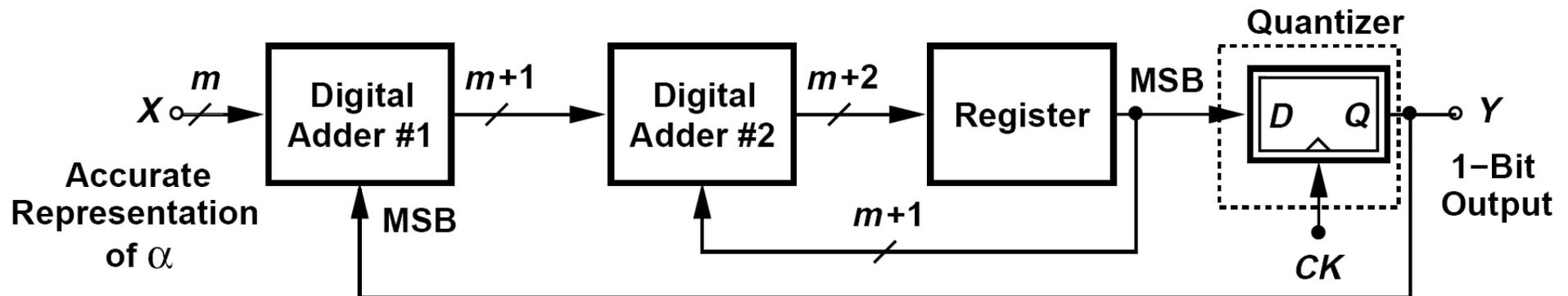
Shown here, the system incorporates an input adder (#1) (in fact a subtractor) and



an integrator (“accumulator”) consisting of a digital adder (#2) and a register (delay element). The first adder receives two m -bit inputs, producing an $(m + 1)$ -bit output. Similarly, the integrator produces an $(m + 2)$ -bit output. Since the feedback path from Y drops the two least significant bits of the integrator output, we say it introduces quantization noise, which is modeled by an additive term, Q .

In analogy with the continuous-time version, we note that the high integrator gain forces Y to be equal to X at low frequencies, i.e., the average of Y is equal to the average of X .

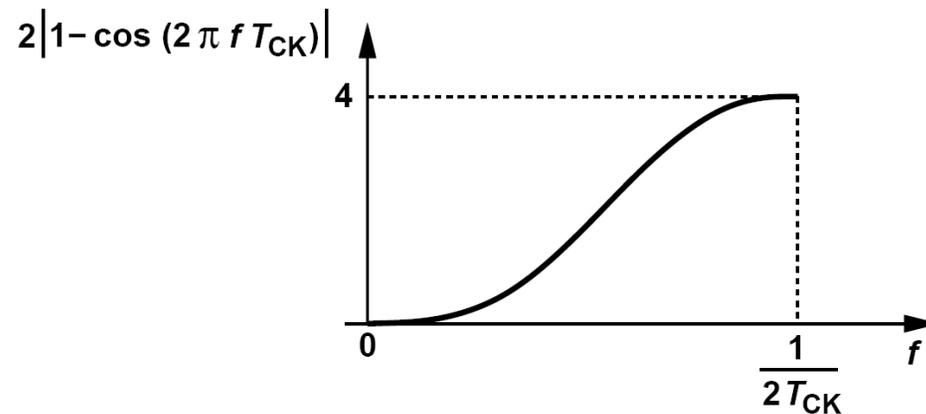
Σ - Δ Modulator



- The quantization from $m+2$ bits to 1 bit introduces significant noise, but the feedback loop shapes this noise in proportion to $1-z^{-1}$. The higher integrator gain ensures that the average of the output is equal to X .
- The choice of m is given by the accuracy with which the synthesizer output frequency must be defined.

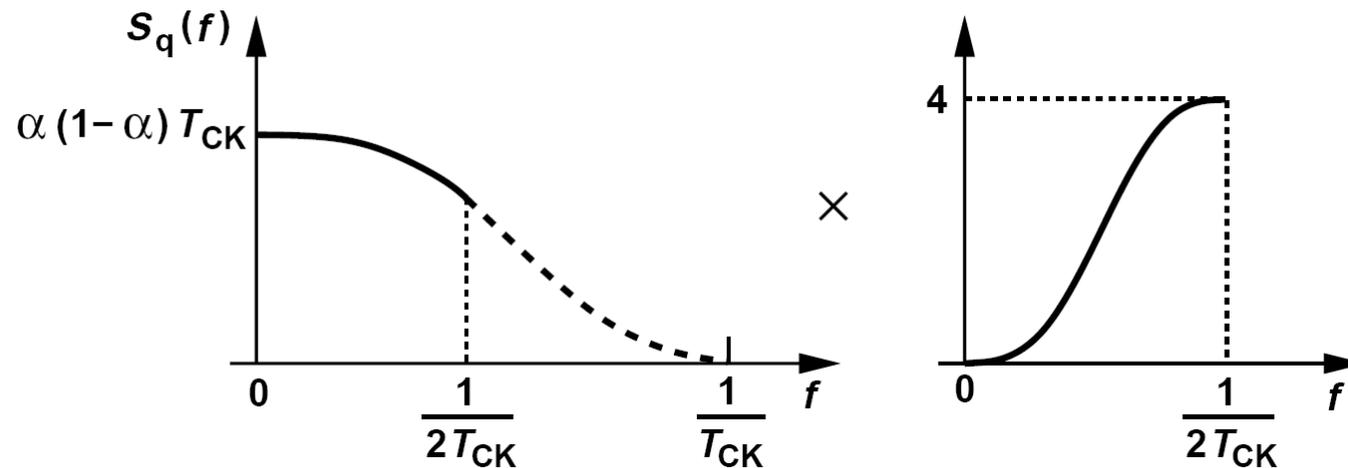
Noise Shaping of Modulator

$$\begin{aligned}\frac{Y}{Q}(z) &= 1 - z^{-1} && \Rightarrow S_y(f) = S_q(f) |2 \sin(\pi f T_{CK})|^2 \\ &= e^{-j\pi f T_{CK}} (e^{j\pi f T_{CK}} - e^{-j\pi f T_{CK}}) && = 2S_q(f) |1 - \cos(2\pi f T_{CK})|. \\ &= 2j e^{-j\pi f T_{CK}} \sin(\pi f T_{CK}).\end{aligned}$$



- The noise shaping function begins from zero at $f = 0$ and climbs to 4 at $f = (2T_{CK})^{-1}$ (half the clock frequency).
- A higher clock rate expands the function horizontally, thus reducing the noise density at low frequencies.

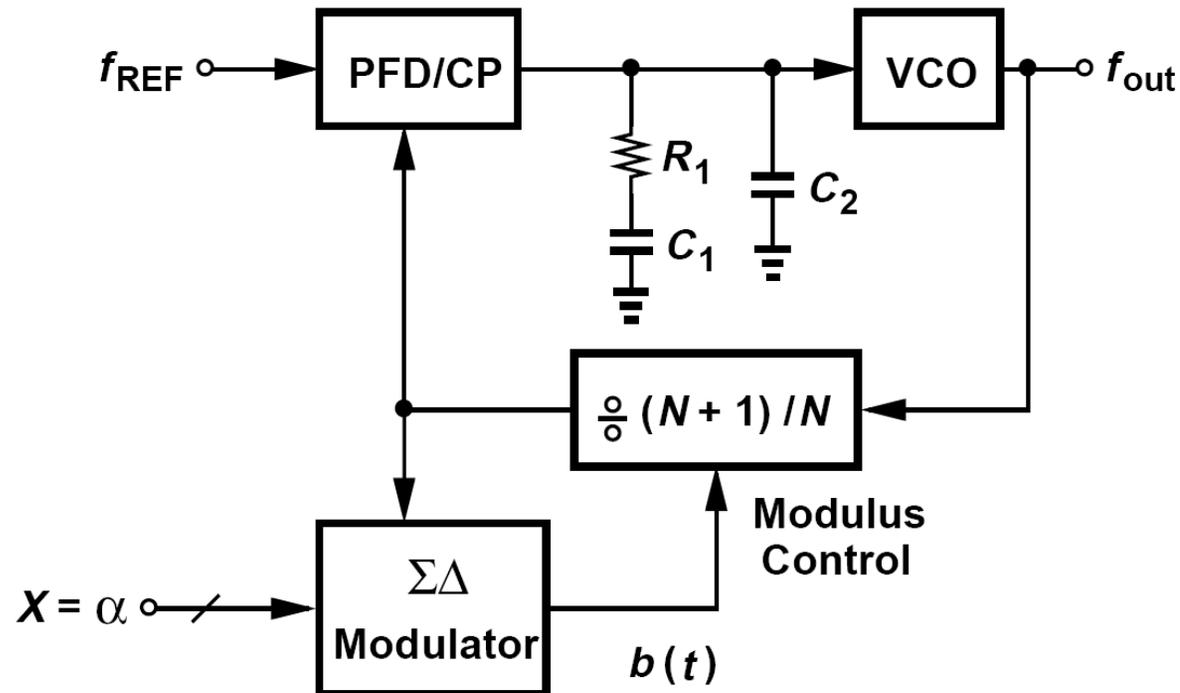
Shape of $S_y(f)$



$$S_y(f) = 2 \frac{\alpha(1-\alpha)}{T_{CK}} \left(\frac{\sin \pi T_{CK} f}{\pi f} \right)^2 |1 - \cos(2\pi f T_{CK})|$$

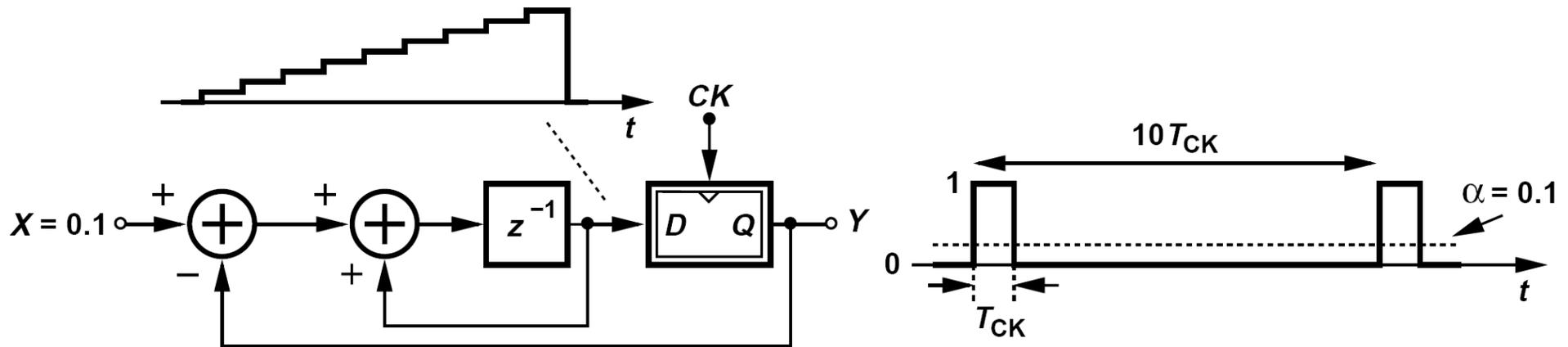
- Since the PLL bandwidth is much smaller than f_{REF} , we can consider $S_q(f)$ relatively flat for the frequency range of interest. We hereafter assume that the shape of $S_y(f)$ is approximately the same as that of the noise-shaping function.

Summary: Fractional-N Synthesizer Developed Thus Far



- Shown above is a basic fractional- N loop using a $\Sigma\Delta$ modulator to randomize the divide ratio.
- Clocked by the feedback signal, the $\Sigma\Delta$ modulator toggles the divide ratio between N and $N+1$ so that the average is equal to $N+\alpha$

Problem of Tones



- The output spectrum of Σ - Δ modulators contains the shaped noise, but also discrete tones. If lying at low frequencies, such tones are not removed by the PLL, thereby corrupting the synthesizer output.
- To suppress these tones, the periodicity of the system must be broken. If the LSB of X randomly toggles between 0 and 1, then the pulses in the output waveform occur randomly, yielding a spectrum with relatively small tones.

Seeking a System with a Higher-Order Noise Shaping

The noise shaping function shown above does not adequately suppress the in-band noise. This can be seen by noting that, for $f \ll (\pi T_{CK})^{-1}$,

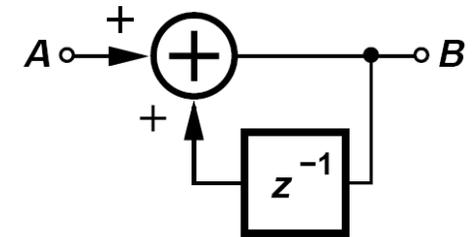
$$S_y(f) = S_q(f) |2\pi f T_{CK}|^2$$

We therefore seek a system that exhibits a sharper roll-off.

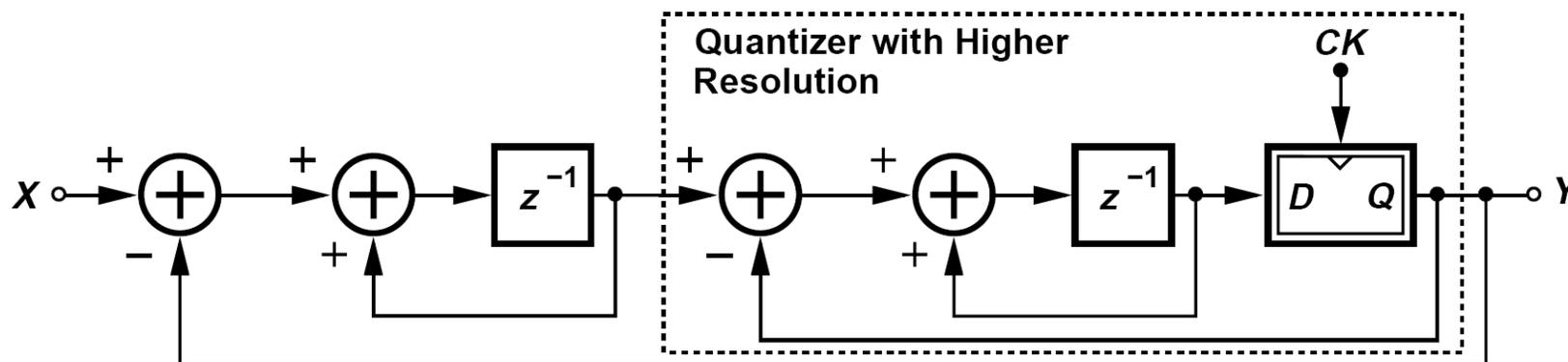
The following development will call for a “non-delaying integrator”.

The transfer function is given by

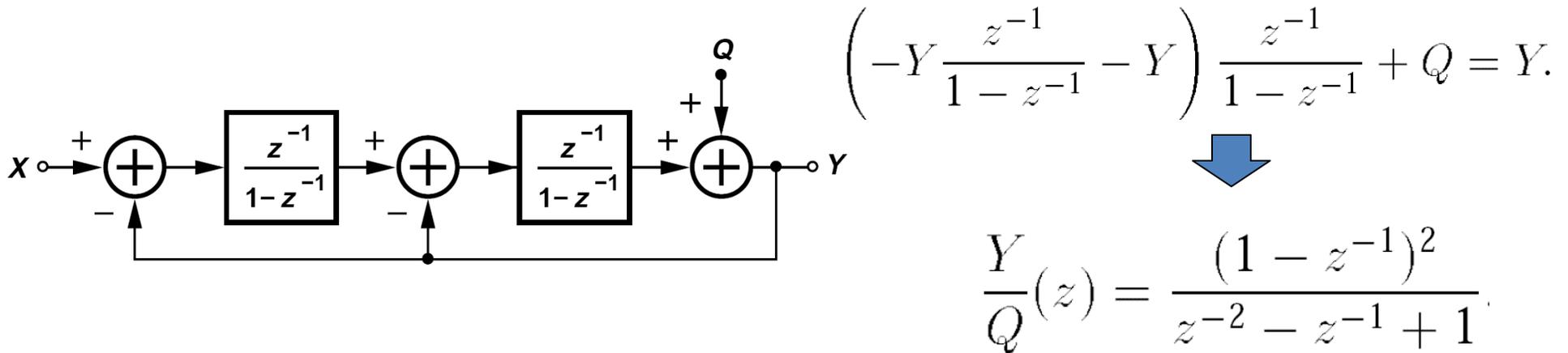
$$\frac{B}{A}(z) = \frac{1}{1 - z^{-1}}$$



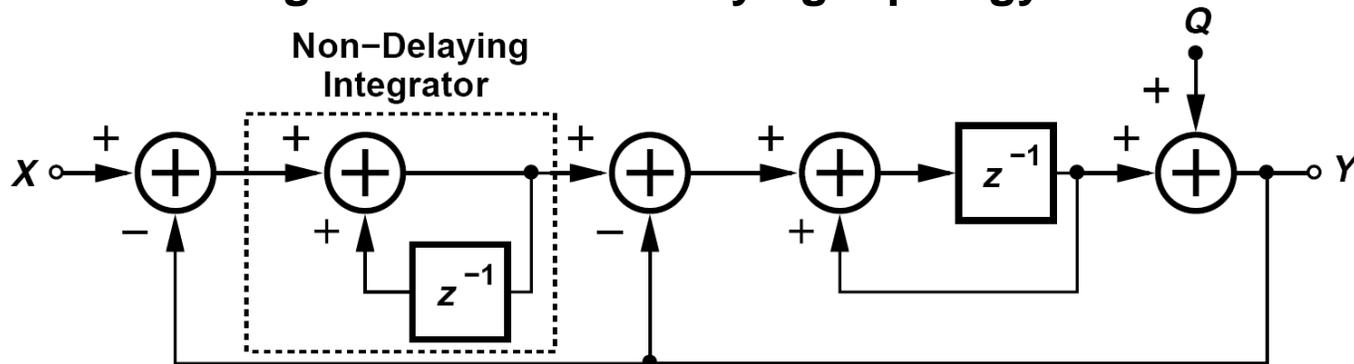
Replace the 1-bit quantizer with a Σ - Δ modulator



To Determine the Noise Shaping Function



Modifying the first integrator to a non-delaying topology:

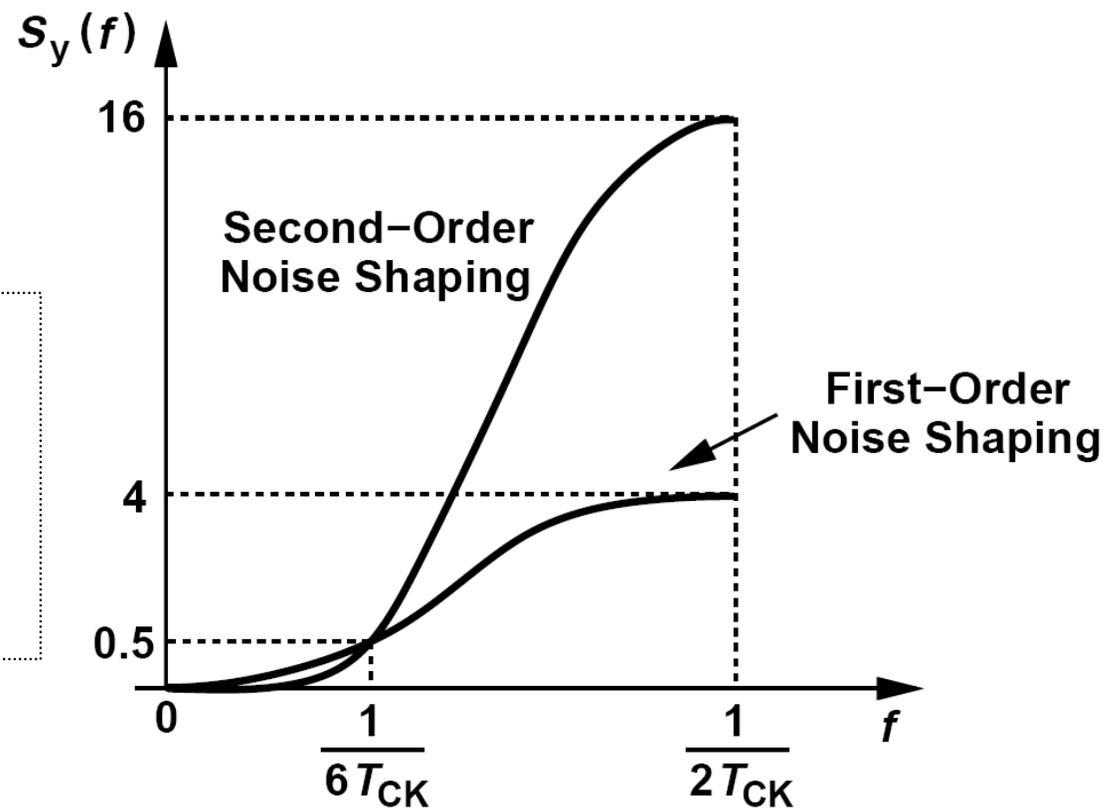


$$\left(-Y \frac{z^{-1}}{1-z^{-1}} - Y\right) \frac{z^{-1}}{1-z^{-1}} + Q = Y. \Rightarrow \frac{Y}{Q}(z) = (1-z^{-1})^2.$$

Comparison: Noise Shaping in First- and Second-Order Modulators

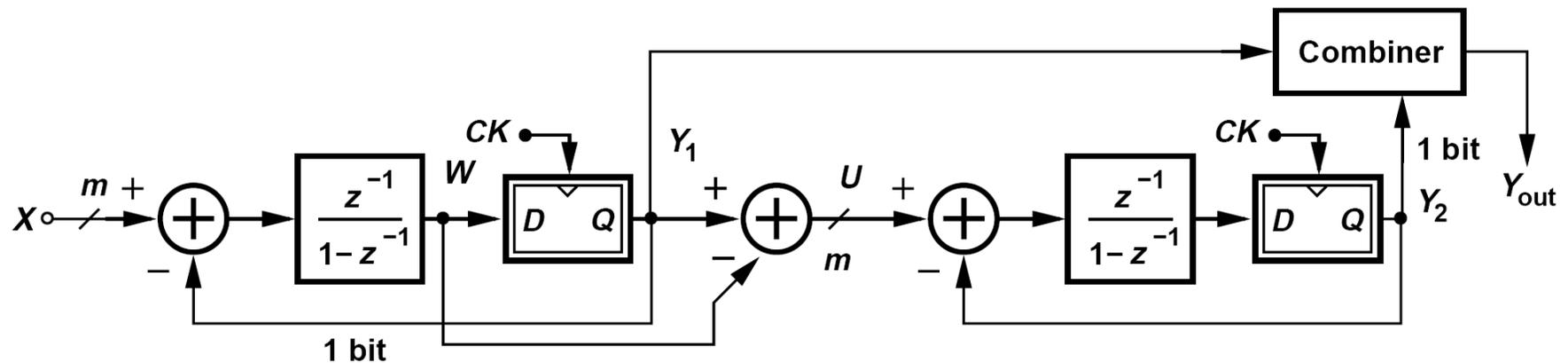
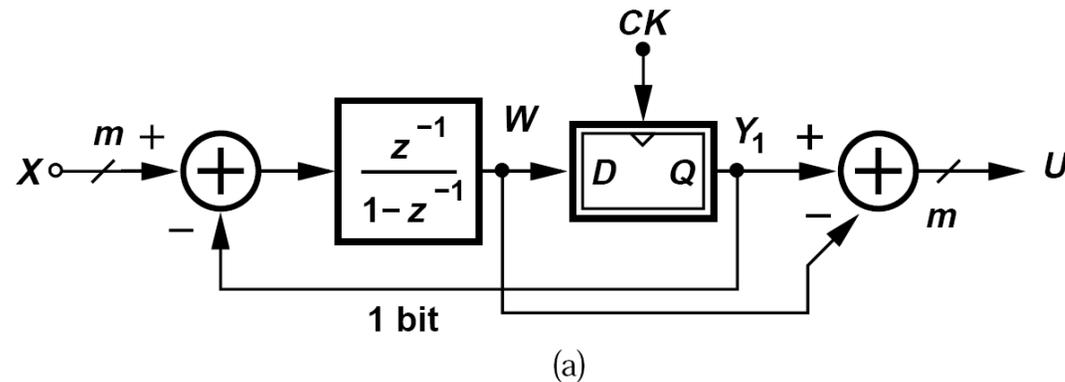
We have

$$S_y(f) = S_q(f) |2 \sin(\pi f T_{CK})|^4,$$



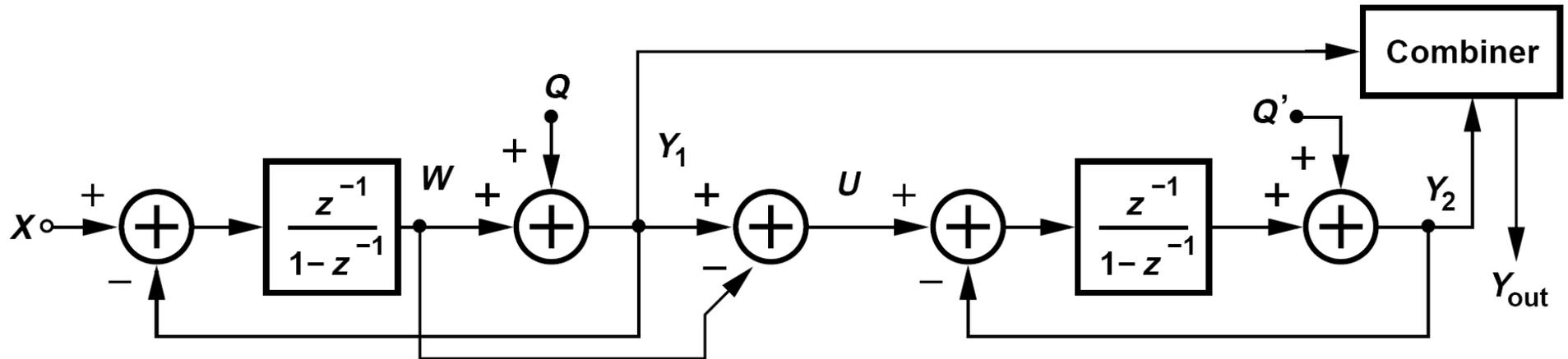
- The noise shaping in second-order modulator remains lower than that of the first-order modulator for frequencies up to $(6T_{CK})^{-1}$

Cascaded Modulators



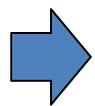
- Y_2 is a relatively accurate replica of U . Y_2 is combined with Y_1 , yielding Y_{out} as a more accurate representation of X . The system is called a “1-1 cascade”.

Residual Quantization Noise



we have $Y_1(z) = z^{-1}X(z) + (1 - z^{-1})Q(z),$

and $Y_2(z) = z^{-1}U(z) + (1 - z^{-1})Q'(z)$
 $= z^{-1}Q(z) + (1 - z^{-1})Q'(z).$



$$Y_{out}(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$$

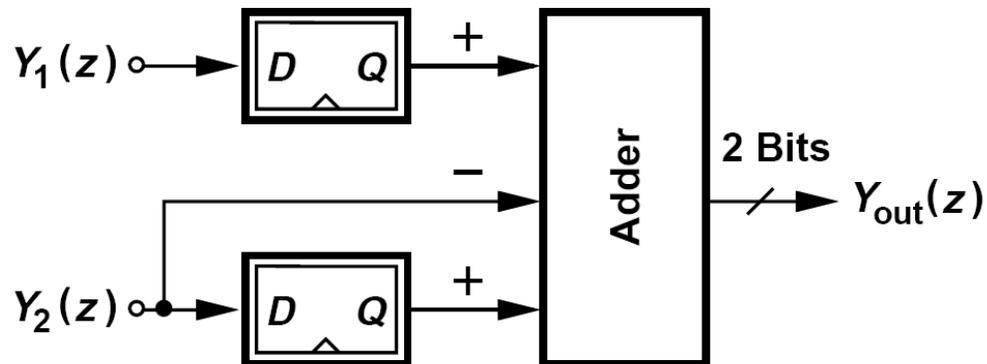
$$= z^{-2}X(z) - (1 - z^{-1})^2Q'(z).$$

Example of Signal Combining Operation

Construct a circuit that performs the combining operation shown previously.

Solution:

For 1-bit streams, multiplication by z^{-1} is realized by a flipflop. The circuit thus appears as shown below:



Problem of Out-of-Band Noise

The transfer function from the quantization noise to the frequency noise

$$Y(z) = (1 - z^{-1})^2 Q(z).$$

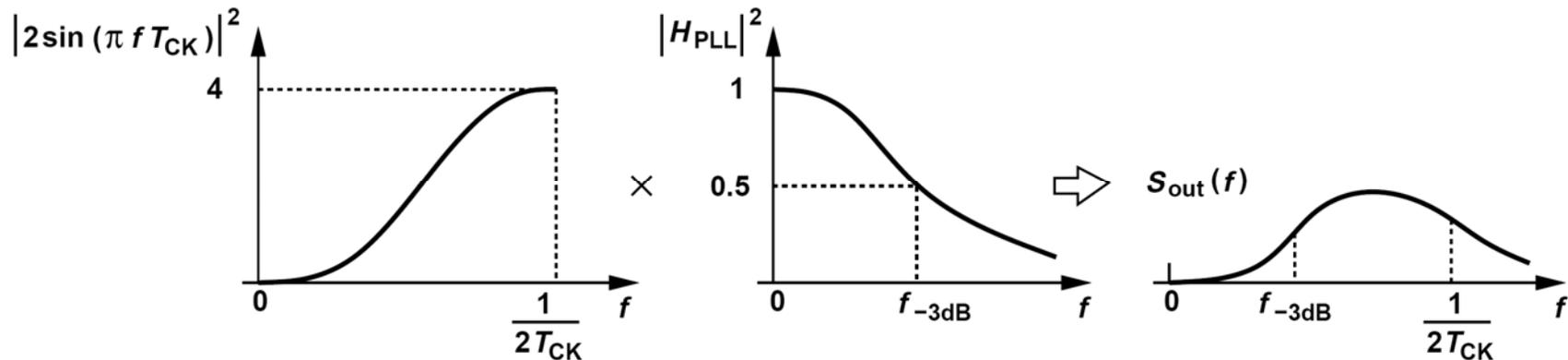
the phase noise $\Phi(z) = (1 - z^{-1})Q(z).$

The spectrum of the phase noise is thus obtained as

$$\begin{aligned} S_{\Phi}(f) &= |1 - z^{-1}|^2 S_q(f) \\ &= |2 \sin(\pi f T_{CK})|^2 S_q(f). \end{aligned}$$

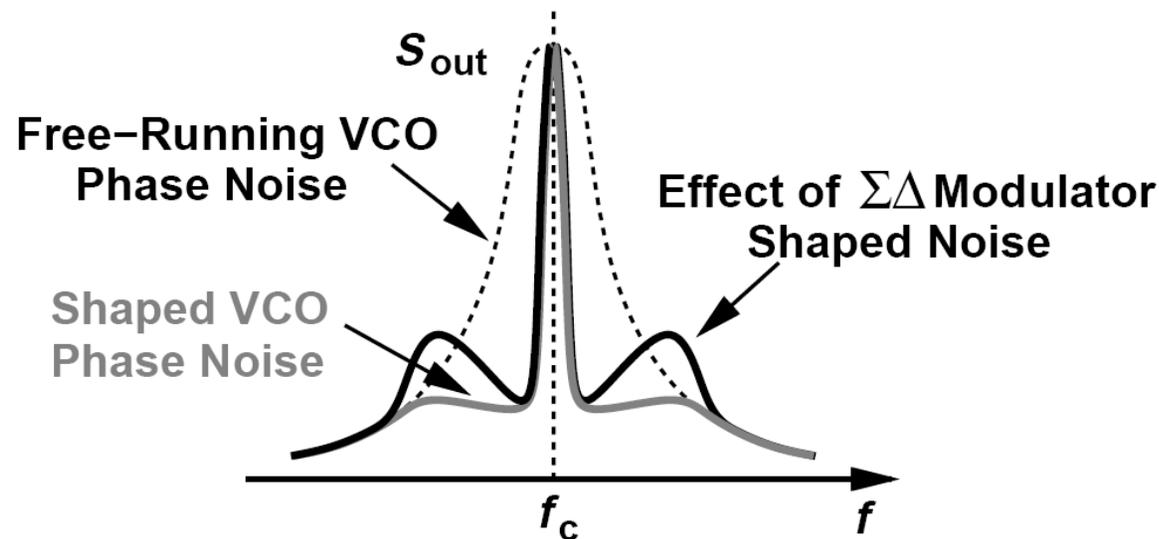
Experiencing the low-pass transfer function

$$S_{out}(f) = |2 \sin(\pi f T_{CK})|^2 S_q(f) N^2 \frac{4\zeta^2 \omega_n^2 \omega^2 + \omega_n^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2 \omega_n^2 \omega^2},$$

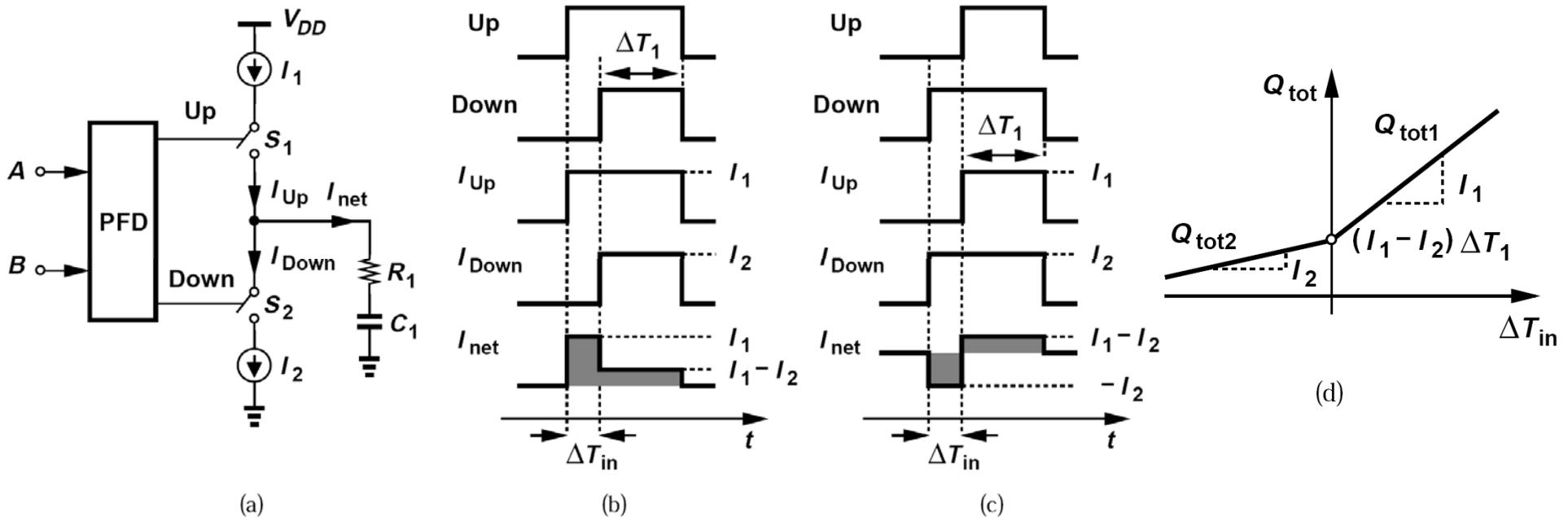


Summary: Effects of Phase Noise at the Output of a Fractional-N Loop

- For small value of f , the product, $S_{out}(f)$, begins from zero and rises to some extent.
- For larger values of f , the f^2 behavior of the noise shaping function cancels the roll-off of the PLL, leading to a relatively constant plateau.
- At values of f approaching $1/(2T_{CK}) = f_{REF}/2$, the product is dominated by the PLL roll-off. If comparable with the shaped VCO phase noise, this peaking proves troublesome.



Effect of Charge Pump Mismatch



the total charge delivered to the loop filter is equal to

$$Q_{tot1} = I_1 \cdot \Delta T_{in} + (I_1 - I_2) \cdot \Delta T_1.$$

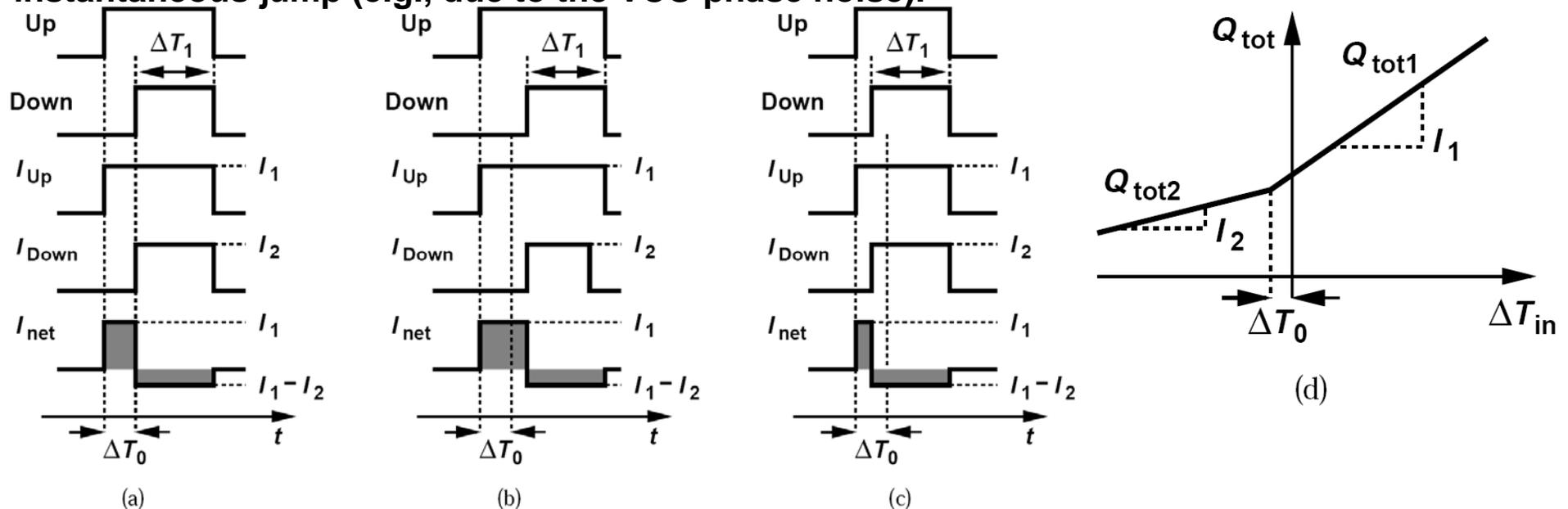
Now, let us reverse the polarity of the input phase difference.

$$Q_{tot2} = I_2 \cdot \Delta T_{in} + (I_1 - I_2) \Delta T_1.$$

Example of Charge Pump Mismatch in Integer-N Synthesizers

Does the above nonlinearity manifest itself in integer- N synthesizers?

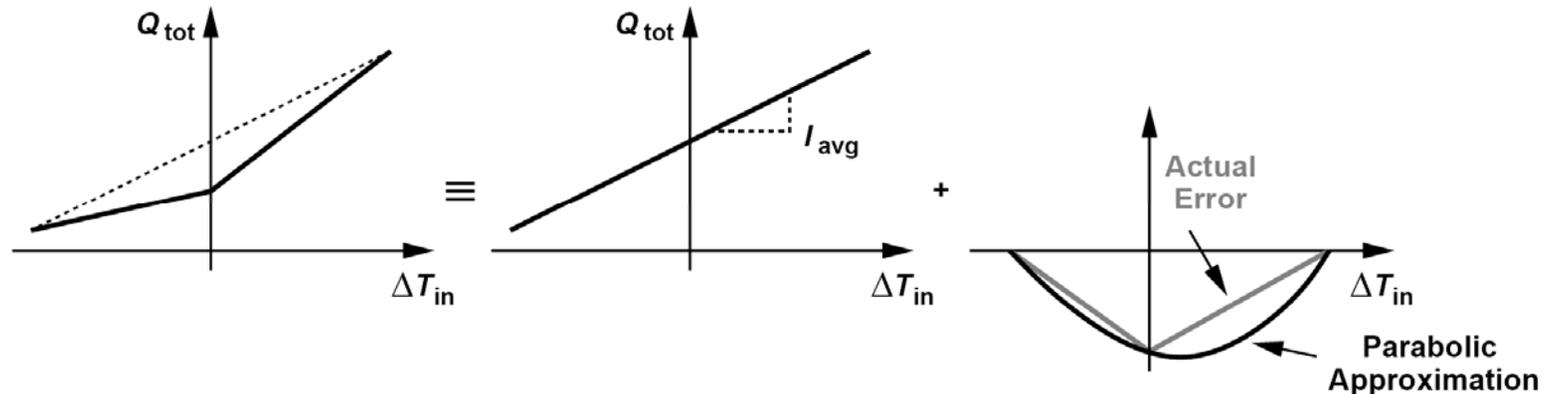
No, it does not. Recall from Chapter 9 that, in the presence of a mismatch between I_1 and I_2 , an integer- N PLL locks with a static phase offset, ΔT_0 , such that the net charge injected into the loop filter is zero. Now suppose the divider output phase experiences a small positive instantaneous jump (e.g., due to the VCO phase noise).



The net charge therefore becomes proportionally positive. Similarly, for a small negative instantaneous phase jump, the net charge becomes proportionally negative. The key point is that, in both cases, the charge is proportional to I_1 , leading to the characteristic shown in (d).

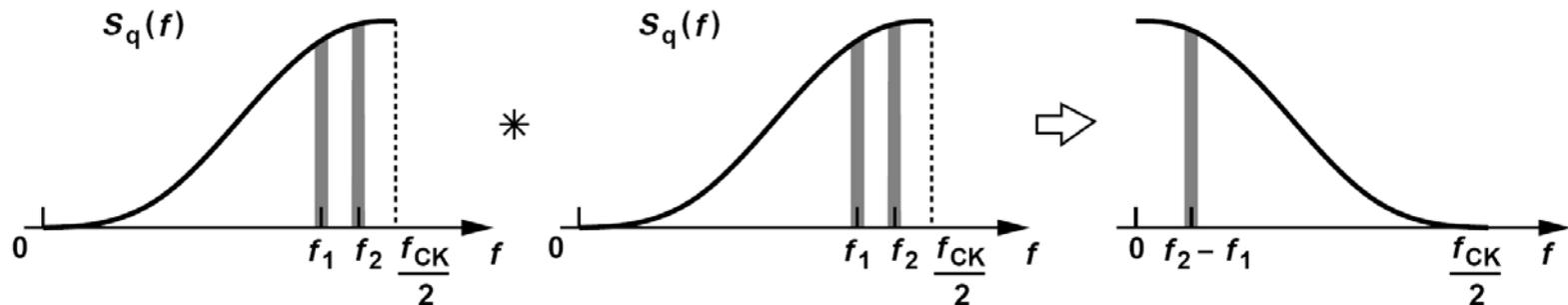
What is the Effect of the Above Nonlinearity on a $\Sigma\Delta$ Fractional-N Synthesizer?

Decompose the characteristic shown in previous example into two components:



We roughly approximate the error by a parabola, $\alpha\Delta T_{in}^2 - b$, and write $Q_{tot} \approx I_{avg}\Delta T_{in} + \alpha\Delta T_{in}^2 - b$

- The multiplication of ΔT_{in} by itself is a mixing effect and translates to the convolution.



- Charge pump nonlinearity translates the $\Sigma\Delta$ modulator's high-frequency quantization noise to in-band noise, thus modulating VCO.

Approach to Alleviating the Charge Pump Mismatch

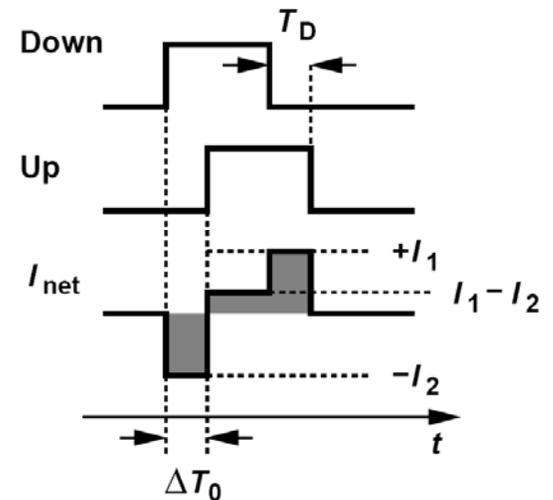
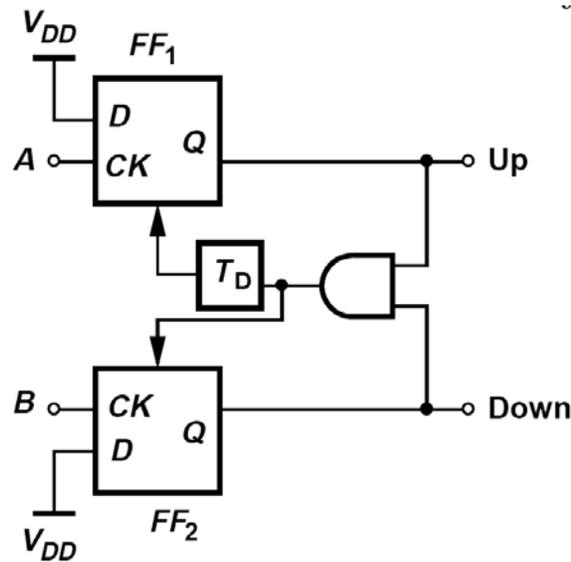
- Split the PFD reset pulse to create a static phase error and avoid slope change.

The PLL must lock with a zero net charge

$$\Delta T_0 \cdot I_2 \approx T_D \cdot I_1$$

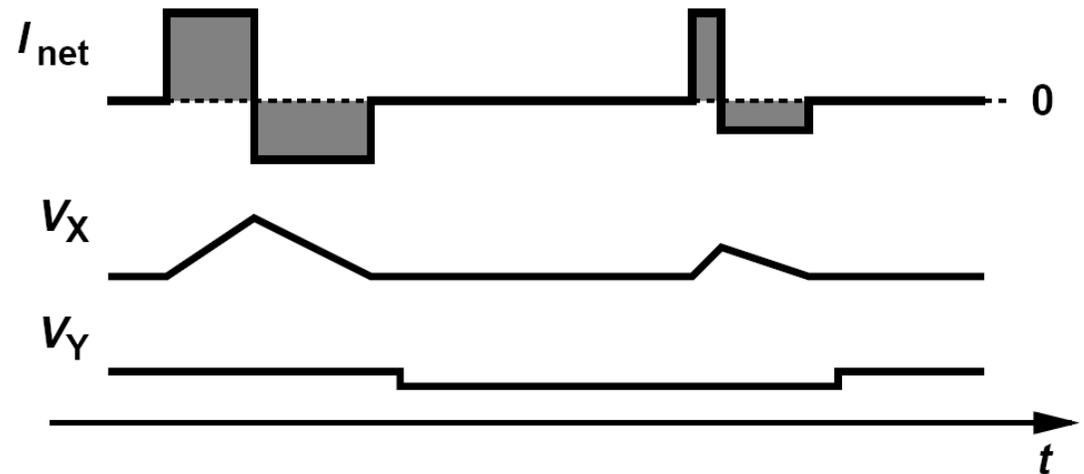
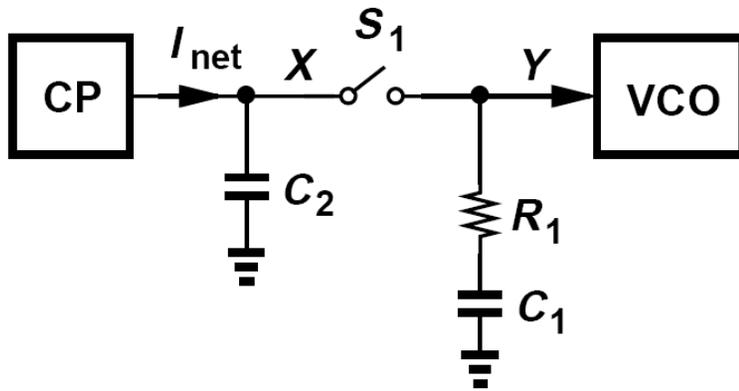
The static phase offset is

$$\Delta T_0 \approx T_D$$



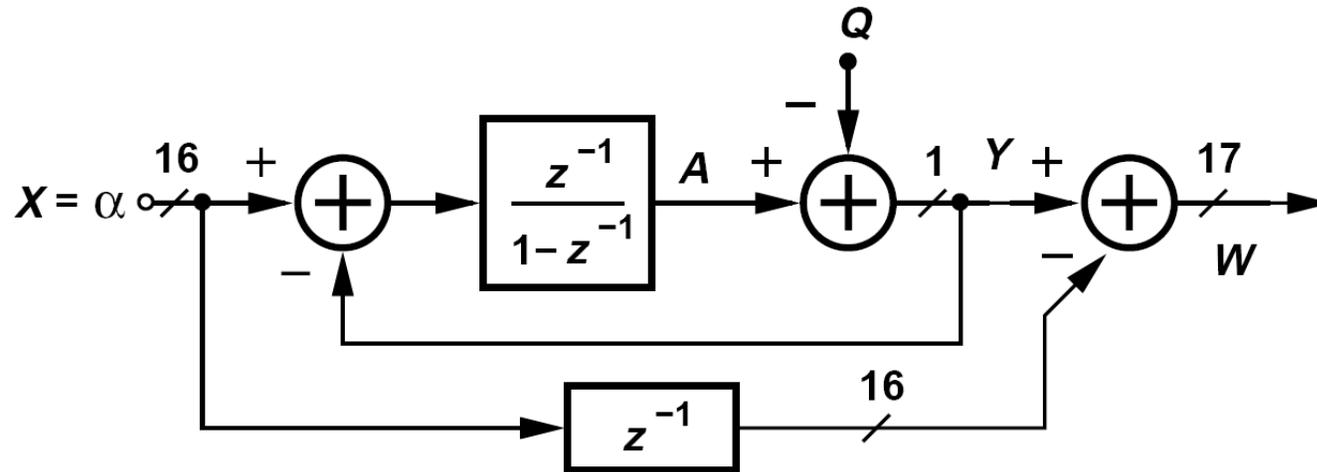
- For a sufficiently large T_D and hence ΔT₀, phase fluctuations simply modulate the width of the negative current pulse in I_{net}, leading to a characteristic with a slope of I₂. Unfortunately, this technique also introduces significant ripple on the control voltage.

Another Approach Using Sampling Circuit



- A sampling circuit interposed between the charge pump and the loop filter can “mask” the ripple, ensuring that the oscillator control line sees only the settled voltage produced by the CP.
- In other words, a deliberate current offset or Up/Down misalignment along with a sampling circuit removes the nonlinearity resulting from the charge pump and yields a small ripple

Quantization Noise Reduction Techniques: DAC Feedforward



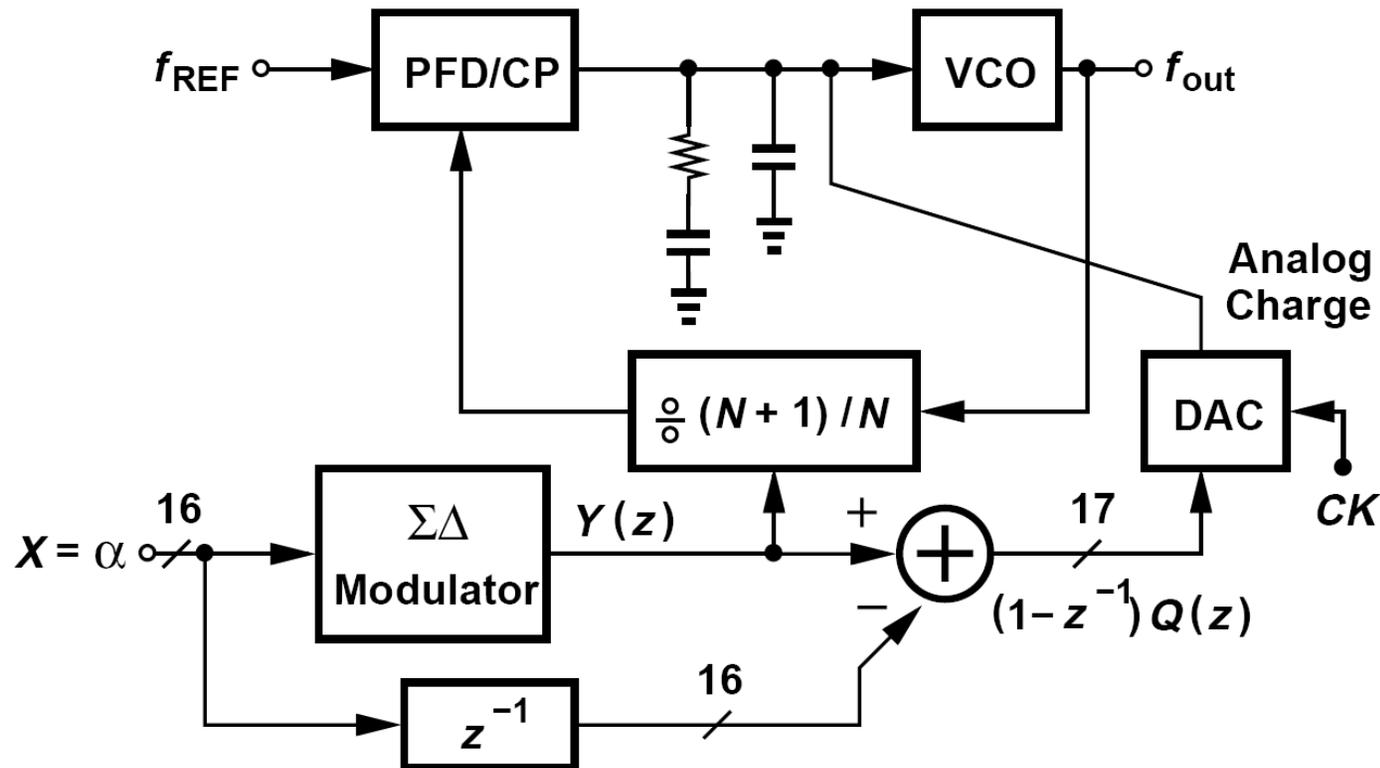
$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z).$$

quantization error:

$$\begin{aligned} W(z) &= Y(z) - z^{-1}X(z) \\ &= (1 - z^{-1})Q(z). \end{aligned}$$

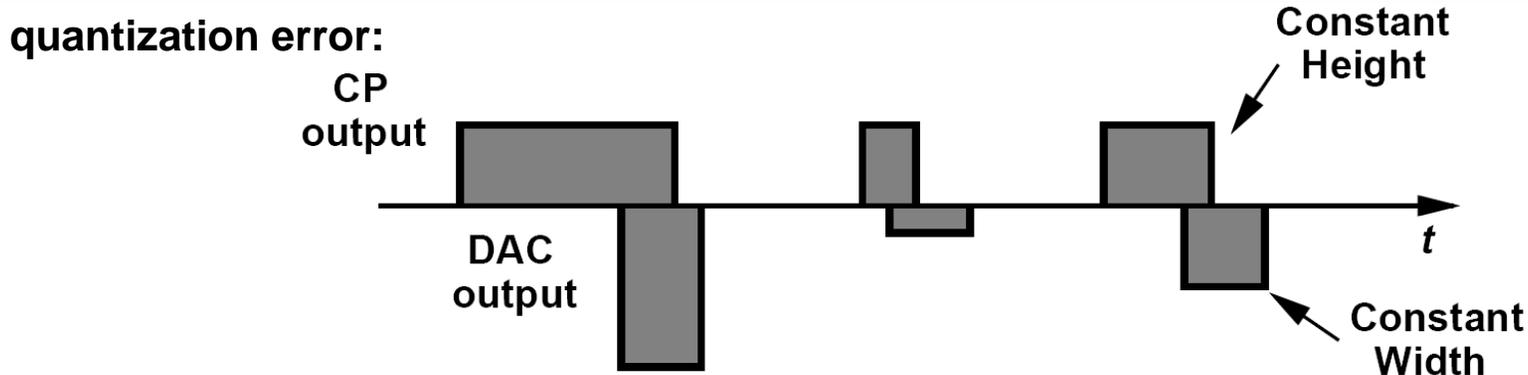
➤ Here, W is the shaped noise whereas in cascaded modulators, we compute $Q = Y - A$, which is unshaped.

Basic DAC Feedforward Cancellation



- In the absence of analog and timing mismatches, each $\Sigma\Delta$ modulator output pulse traveling through the divider, the PFD, and the charge pump is met by another pulse produced by the DAC, facing perfect cancellation.

Issues in Previous System and Modifications(II)

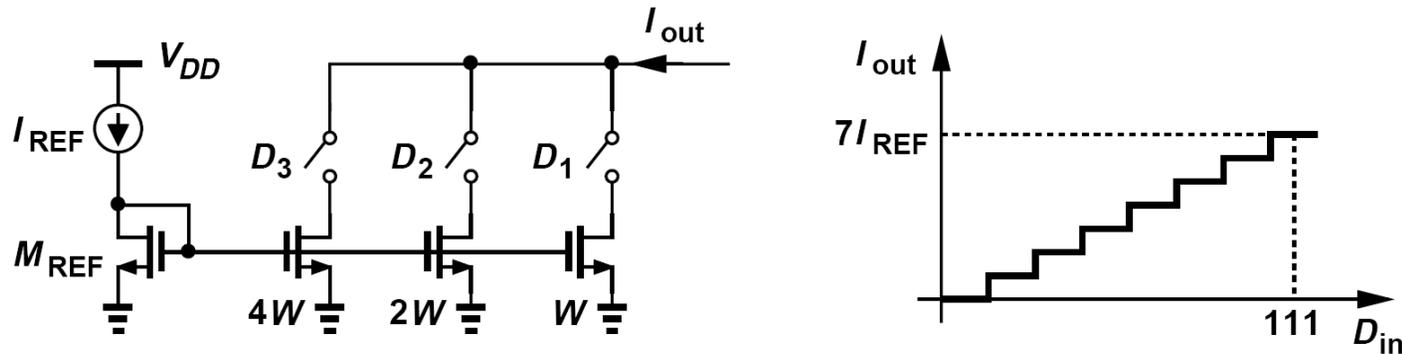


- The Up and Down pulses activate the CP for only a fraction of the reference period, producing a current pulse of constant height each time. The DAC, on the other hand, generates current pulses of constant width.
- The sampling loop filter is typically used to mask the ripple.

What is the effect of the mismatch between the charge pump current and the DAC current in system above?

The unequal areas of the current pulses generated by the CP and the DAC lead to incomplete cancellation of the quantization noise. For example, a 5% mismatch limits the noise reduction to roughly 26 dB.

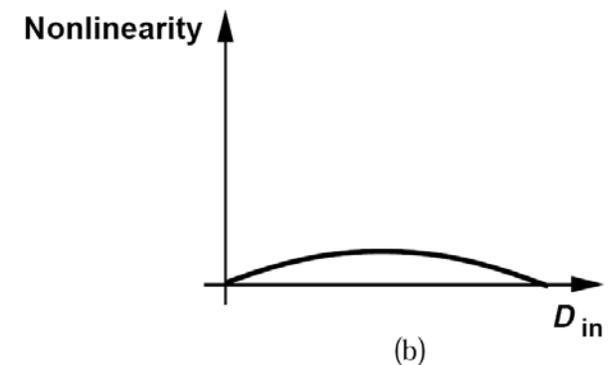
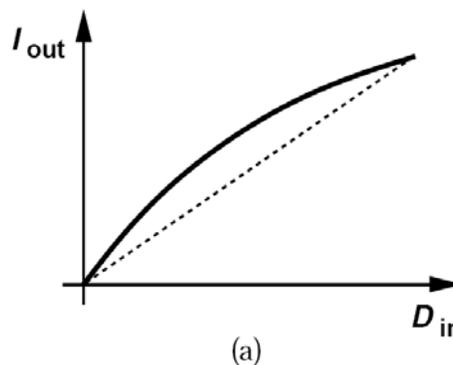
DAC Gain Error



$$I_{out} = I_{REF}(4D_3 + 2D_2 + D_1)$$

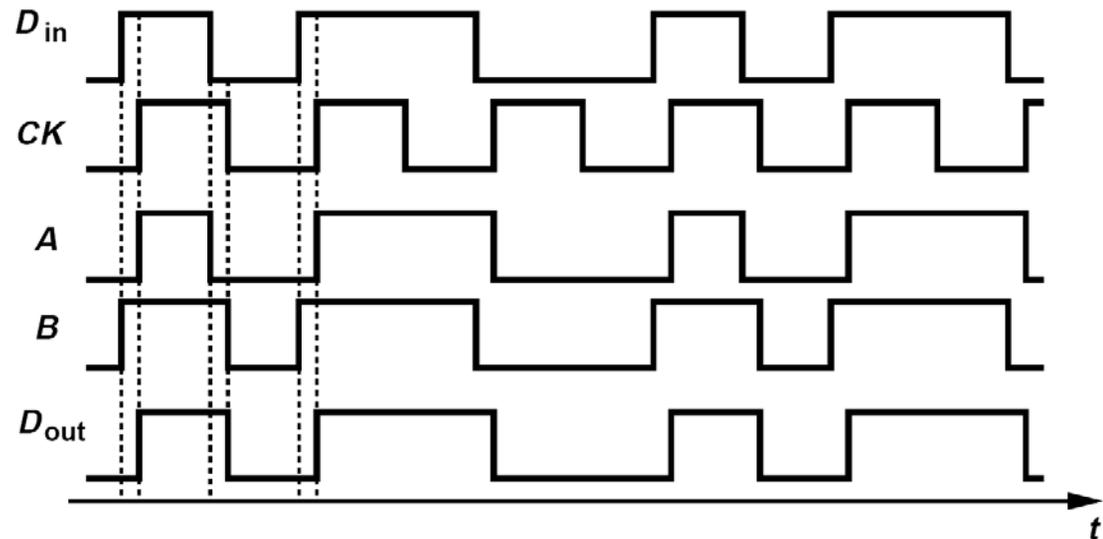
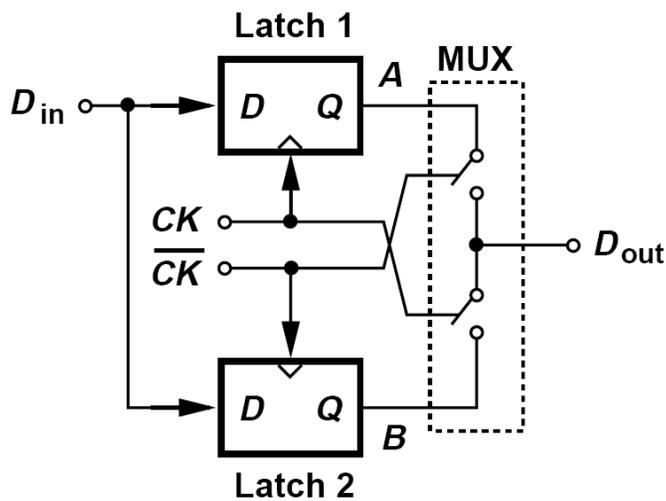
➤ Since both the charge pump current and the DAC current are defined by means of current mirrors, mismatches between these mirrors lead to incomplete cancellation of the quantization noise.

➤ The quantization noise applied to the DAC are convolved and folded to low frequencies, raising the in-band phase noise.



Fractional Divider

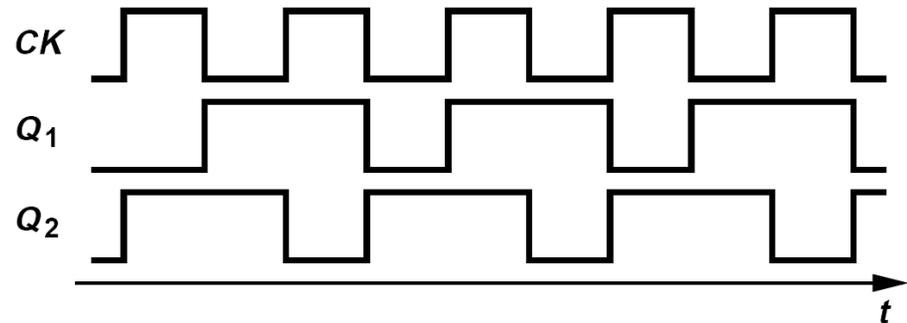
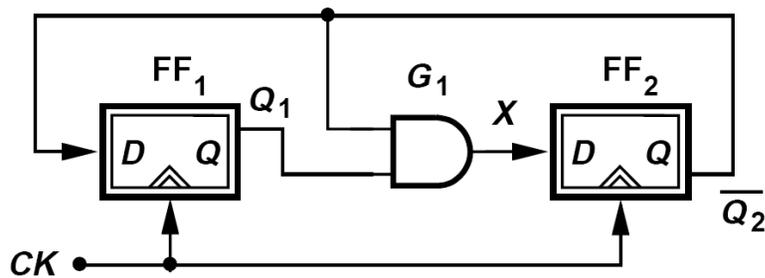
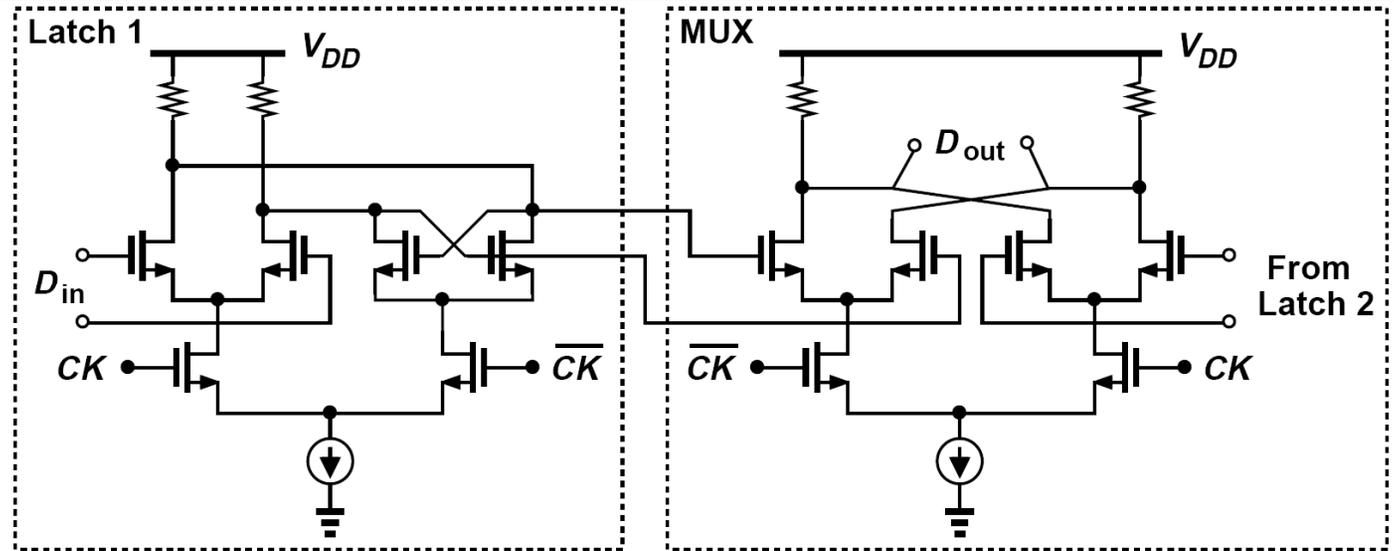
- Another approach to reducing the $\Sigma\Delta$ modulator quantization noise employs “fractional” dividers, i.e., circuits that can divide the input frequency by noninteger values such as 1.5 or 2.5



- Even with a half-rate clock, D_{out} track D_{in} . In other words, for a given clock rate, the input data to a DET flipflop can be twice as fast as that applied to a single-edge-triggered counterpart.

CML Implementation and Use in Divide-by-1.5 Circuit

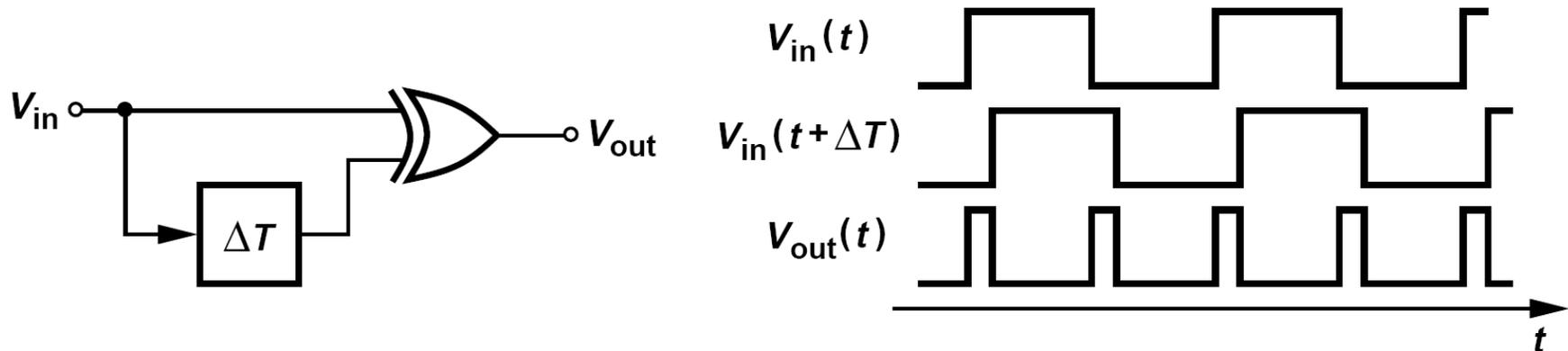
CML implementation



- Replacing the flipflops of $\div 3$ circuit with the DET circuit. The circuit produces one output period for every 1.5 input periods.

Reference Doubling

- If the reference frequency can be doubled by means of an on-chip circuit preceding the PLL, then the phase noise due to the $\Sigma\Delta$ modulator quantization can be reduced by 6 dB.



The input is delayed and XORed with itself, producing an output pulse each time $V_{in}(t)$ and $V_{in}(t - \Delta T)$ are unequal.

Example of Fourier Series of Doubler Output

If we consider $V_{out}(t)$ as the sum of the two half-rate waveforms, determine the Fourier series of $V_{out}(t)$.

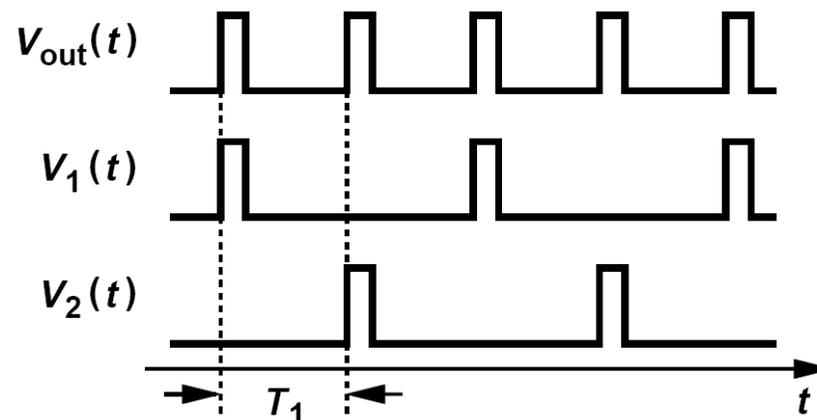
The Fourier series of $V_1(t)$ can be written as

$$V_1(t) = a_1 \cos(\omega_0 t + \phi_1) + a_2 \cos(2\omega_0 t + \phi_2) + a_3 \cos(3\omega_0 t + \phi_3) + \dots,$$

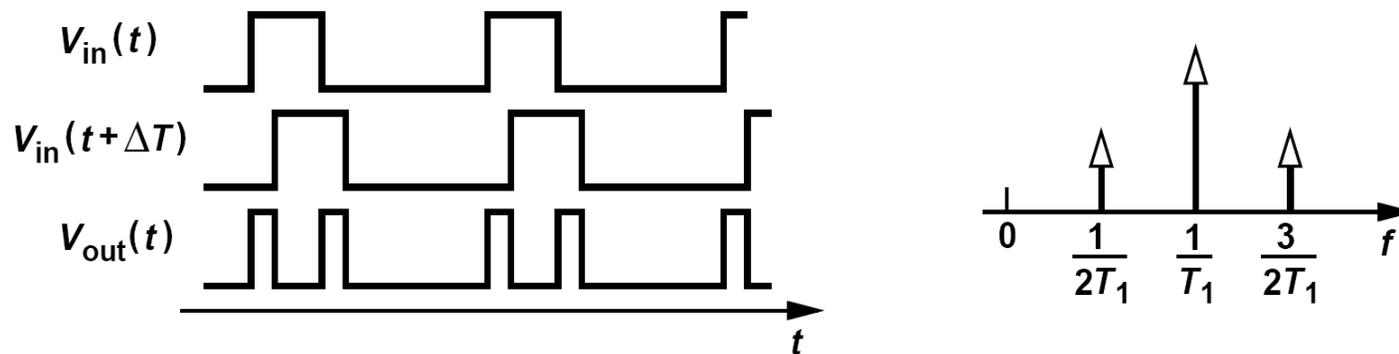
where $\omega_0 = 2\pi/(2T_1)$. The second waveform, $V_2(t)$, is obtained by shifting V_1 by T_1 . Thus, the first harmonic is shifted by $\omega_0 T_1 = \pi$, the second by $2\omega_0 T_1 = 2\pi$, etc. It follows that

$$V_2(t) = -a_1 \cos(\omega_0 t + \phi_1) + a_2 \cos(2\omega_0 t + \phi_2) - a_3 \cos(3\omega_0 t + \phi_3) + \dots$$

Adding $V_1(t)$ and $V_2(t)$, we note that all odd harmonics of ω_0 vanish, yielding a waveform with a fundamental frequency of $2\omega_0$

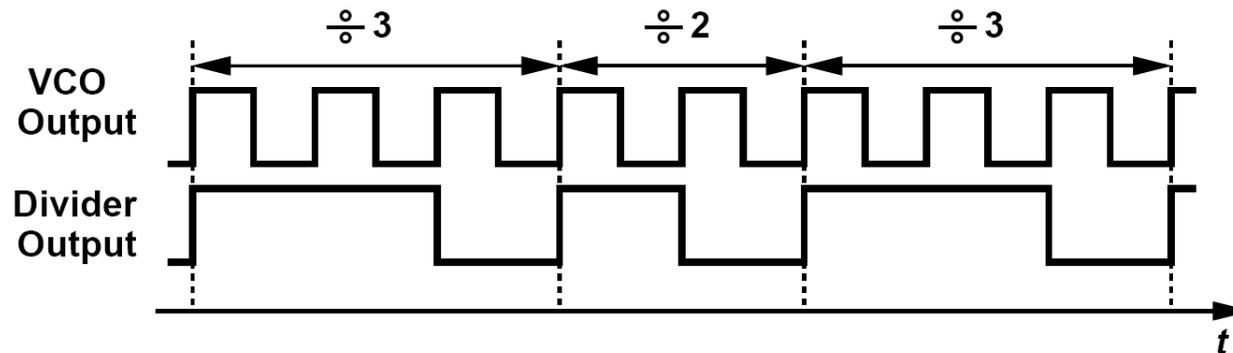


Doubler Output with Input Duty Cycle Distortion



- If the input duty cycle deviates from 50%, the odd harmonics are not completely canceled, appearing as sidebands around the main component at $1/T_1$. Since the PLL bandwidth is chosen about one-tenth $1/T_1$, the sidebands are attenuated to some extent.

Multi-Phase Frequency Division: an Overview



It is possible to create a fractional divide ratio by means of a multi-phase VCO and a multiplexer. Suppose a VCO generates M output phases with a minimum spacing of $2\pi/M$, and the MUX selects one phase each time, producing an output given by

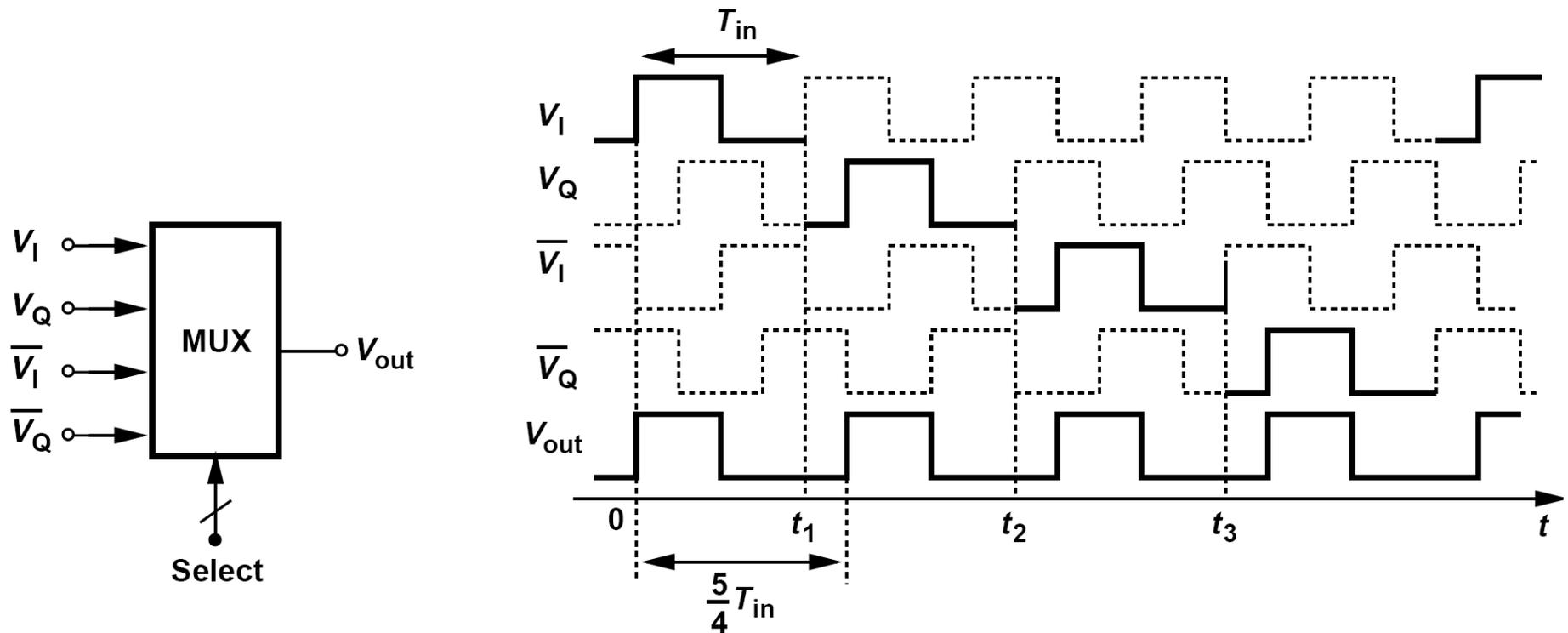
$$V_{MUX}(t) = V_0 \cos \left(\omega_c t - k \frac{2\pi}{M} \right)$$

where k is an integer. Now, let us assume that k varies linearly with time, sequencing through $0, 1, \dots, M-1, M, M+1, \dots$. Thus, $k = \beta t$, where β denotes the rate of change of k , and hence

$$V_{MUX}(t) = V_0 \cos \left[\left(\omega_c - \beta \frac{2\pi}{M} \right) t \right]$$

The divide ratio is therefore equal to $1 - (\beta/\omega_c)(2\pi/M)$

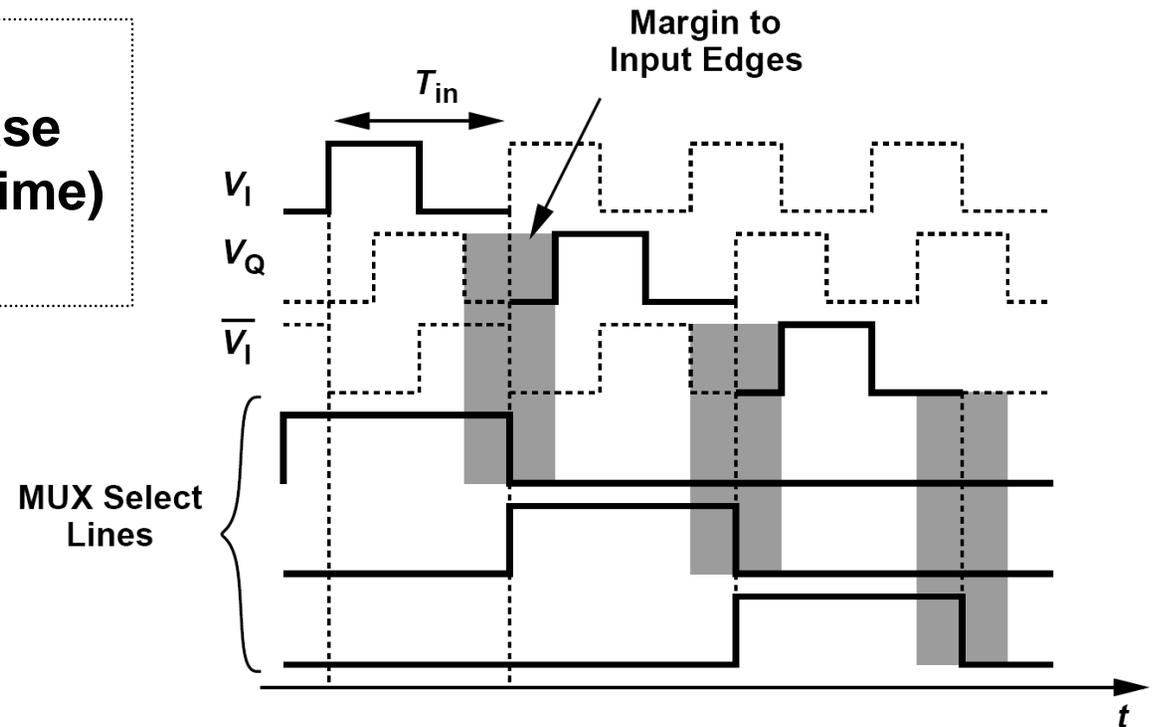
An Example of Multi-Phase Frequency Division



- This technique affords a frequency divider having a modulus of 1 and modulus of 1.25. Since the divide ratio can be adjusted in a step of 0.25, the quantization noise falls by $20 \log 4 = 12$ dB

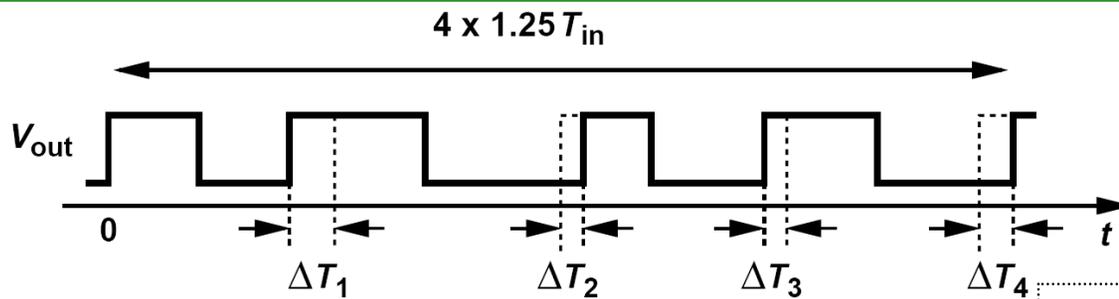
Issues in Multi-Phase Fractional Division: Problem of Phase Selection Timing Margin

- The MUX select command (which determines the phase added to the carrier each time) is difficult to generate.

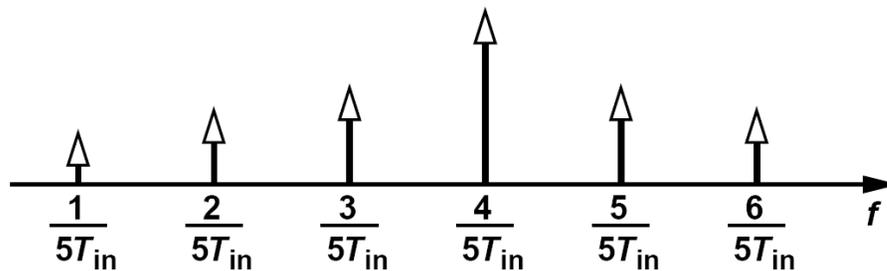


- The edges of the select waveforms have a small margin with respect to the input edges. Moreover, if the divide ratio must switch from 1.25 to 1, a different set of select waveforms must be applied, complicating the generation and routing of the select logic.

Issues in Multi-Phase Fractional Division: Phase Mismatches

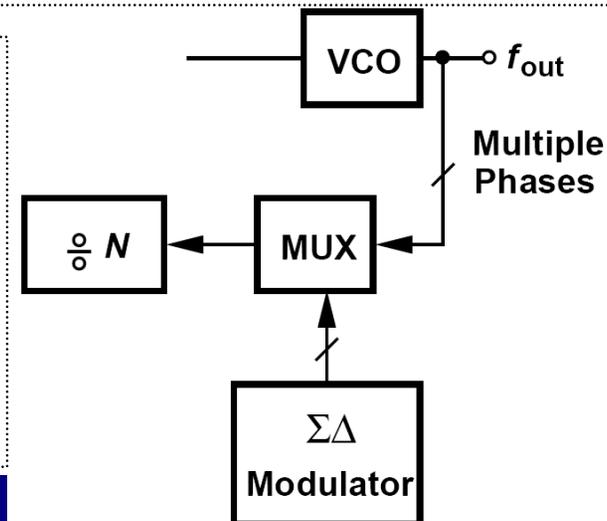


(a)



➤ The quadrature LO phases and the paths within the MUX suffer from mismatches, thereby displacing the output transitions from their ideal points in time.

- The spectrum contains a large component at $4/(5T_{in})$ and “sidebands” at other integer multiples of $1/(5T_{in})$
- It is possible to randomize the selection of the phases so as to convert the sidebands to noise.



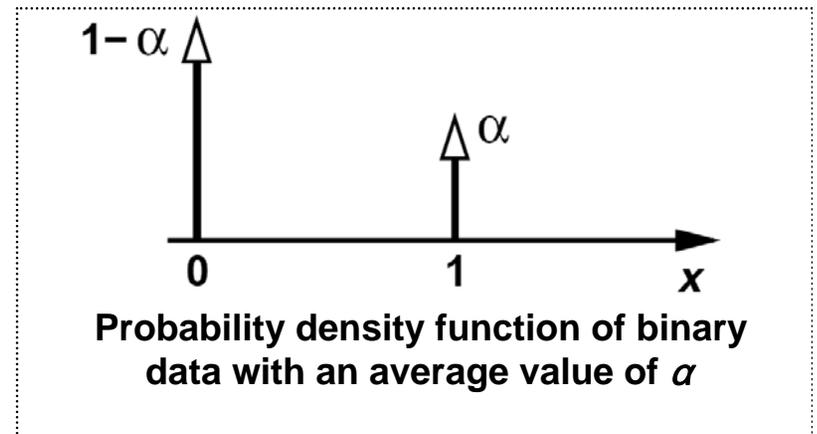
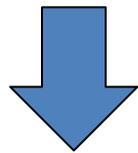
Appendix I: Spectrum of Quantization Noise

In general, if a pulse $p(t)$ is randomly repeated every T_b seconds, the resulting spectrum is given by

$$S(f) = \frac{\sigma^2}{T_b} |P(f)|^2 + \frac{m^2}{T_b^2} \sum_{k=-\infty}^{+\infty} \left| P\left(\frac{k}{T_b}\right) \right|^2 \delta\left(f - \frac{k}{T_b}\right),$$

The variance of a random variable x is obtained as

$$\sigma_x^2 = \int_{-\infty}^{+\infty} (x - m)^2 g(x) dx$$



$$\begin{aligned} \sigma^2 &= \int_{-\infty}^{+\infty} \left[(0 - \alpha)^2 (1 - \alpha) \delta(0) + (1 - \alpha)^2 \alpha \delta(x - 1) \right] dx \\ &= \alpha(1 - \alpha). \end{aligned}$$

Fourier transform of $p(t)$ is equal to

$$P(f) = \frac{\sin \pi f T_b}{\pi f},$$

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