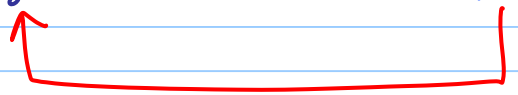
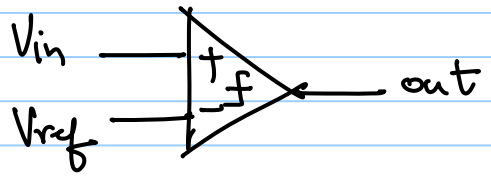
ECE 517 - Lecture 7

Note Title 2/7/2017

Quantizers → Comparators, Sample-and-hold



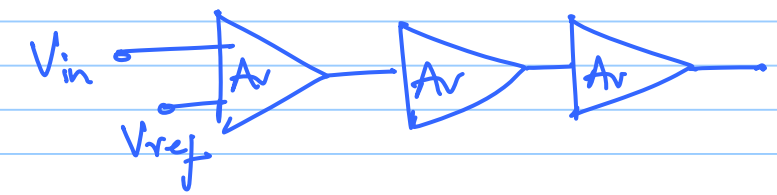
Comparators:



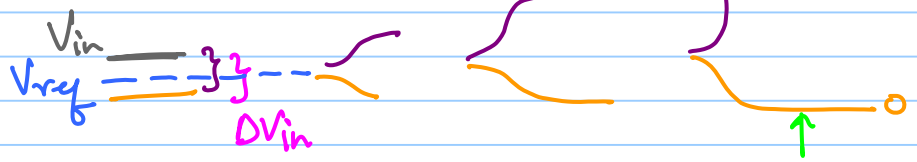
$$\text{out} = \begin{cases} \text{"1"}, & V_{in} > V_{ref} \\ \text{"0"}, & V_{in} \leq V_{ref} \end{cases}$$

"1" ⇒ V_{DD} supply voltage

Ideal :



Cascade of several amplifiers to get a large gain



→ Large Layout area

n- stages

⇒ gain ⇒ A^n, $A>1$

resolvable input = $\frac{V_{DD}}{A^n} \Leftarrow \Delta V_{in}$

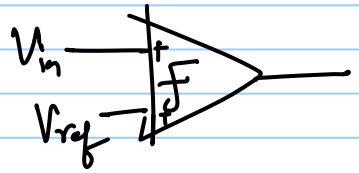
n-stage $\quad A \Rightarrow A^n$

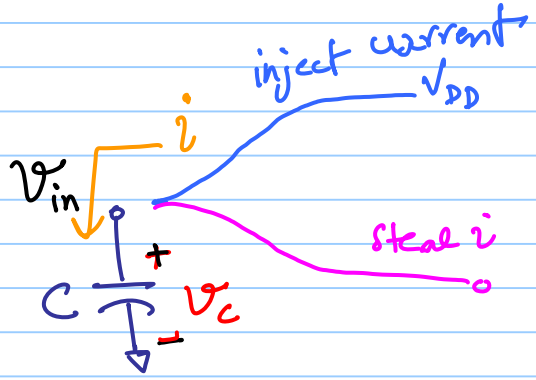
BW of single stage

$$f_{3dB,n} = f_0\sqrt{2^{1/n}-1}$$

Idea 2: Positive feedback

Compare V_{in} with $V_{ref} \triangleq 0$





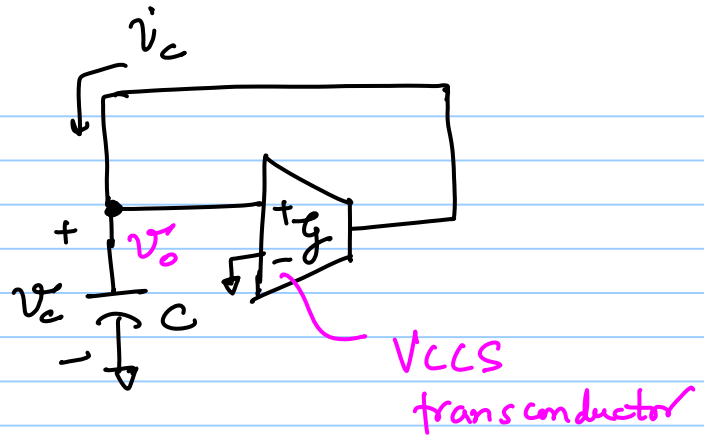
Sampled signal V_{in} is applied to the capacitor C

V_{ref}

* Add more charge to the capacitor if $V_{in} > 0$
↳ inject current into C
⇒ V_c will increase and reach ∞ (V_{DD})

V_{ref}

* Remove charge from the Capacitor if $V_{in} < 0$
↳ steal current from the C
⇒ V_c will decrease and reach $-\infty$ (0V)

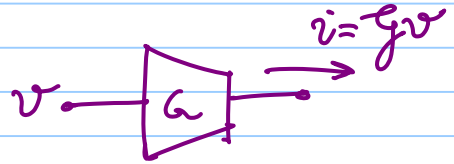


VCCS

"Voltage controlled current source"

↳ transconductor, G

$i = Gv$



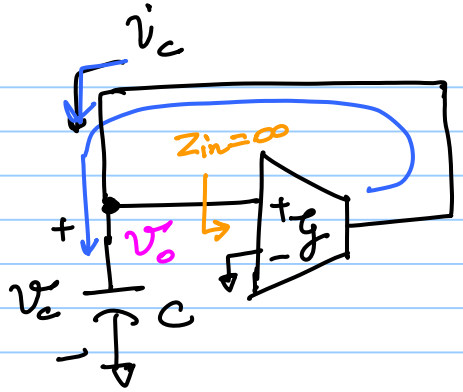
Initial conditions:

@ $t=0$, $v_c = v_o$

final condition

$t \to \infty$, $v_c \to \infty$ if $v_o > 0$

$v_c \to -\infty$ if $v_o < 0$



Regenerative comparator

$$i_c = C\frac{dv_c}{dt} = g v_c \longrightarrow (1)$$

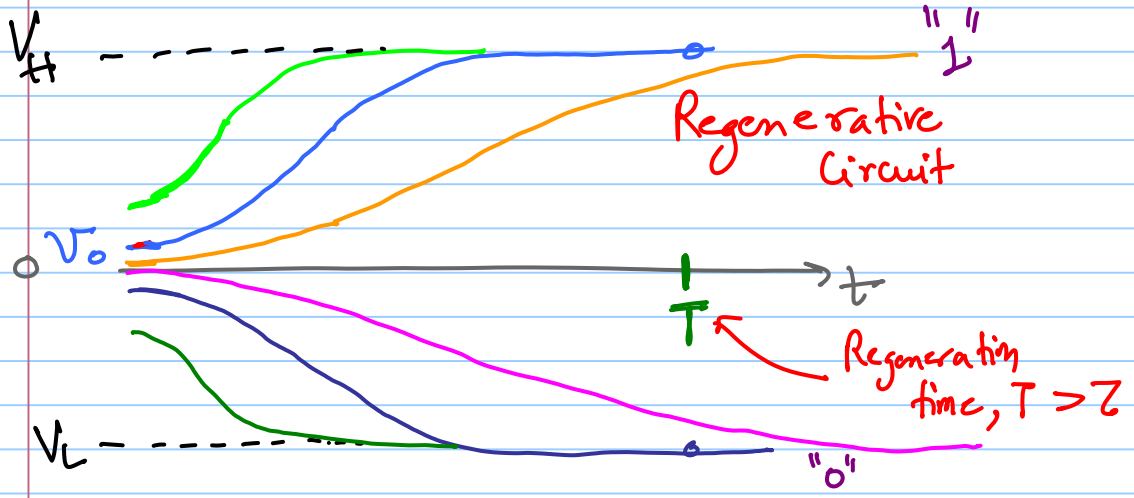
$$C\frac{dv_c}{dt} = g v_c$$

$$\frac{dv_c}{dt} = \left(\frac{g}{C}\right) v_c$$

$$\boxed{v_c = v_o e^{+g/C\,t}}$$

Exponential

g/C is in the right half plane (RHP)
↳ system is not stable



Regeneration time depends upon

↳ V_o

↳ $\tau_c = \frac{C}{G}$ } regenerative time constant

↳ $\frac{C}{G} \sim RC \sim$ dimension of time

gain ⇒ function of time

$\frac{dV_c}{dt} \sim V_c = V_c(t)$

↳ if we wait long enough, the gain will get higher

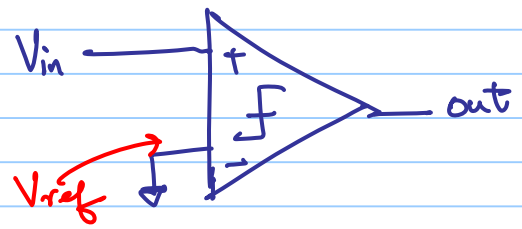
↳ hardware efficient method compared to the amplifier solution

↳ +ve feedback is used here

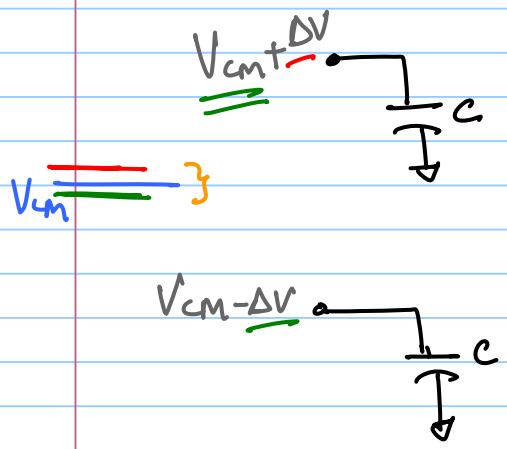
↳ standard circuit for resolving voltage differences.

Minimum resolvable voltage $\Rightarrow \Delta V_{in} \propto \frac{V_{DD}}{e^{\frac{T}{T_{GLC}}}}$

'T' $\Rightarrow$ regeneration time

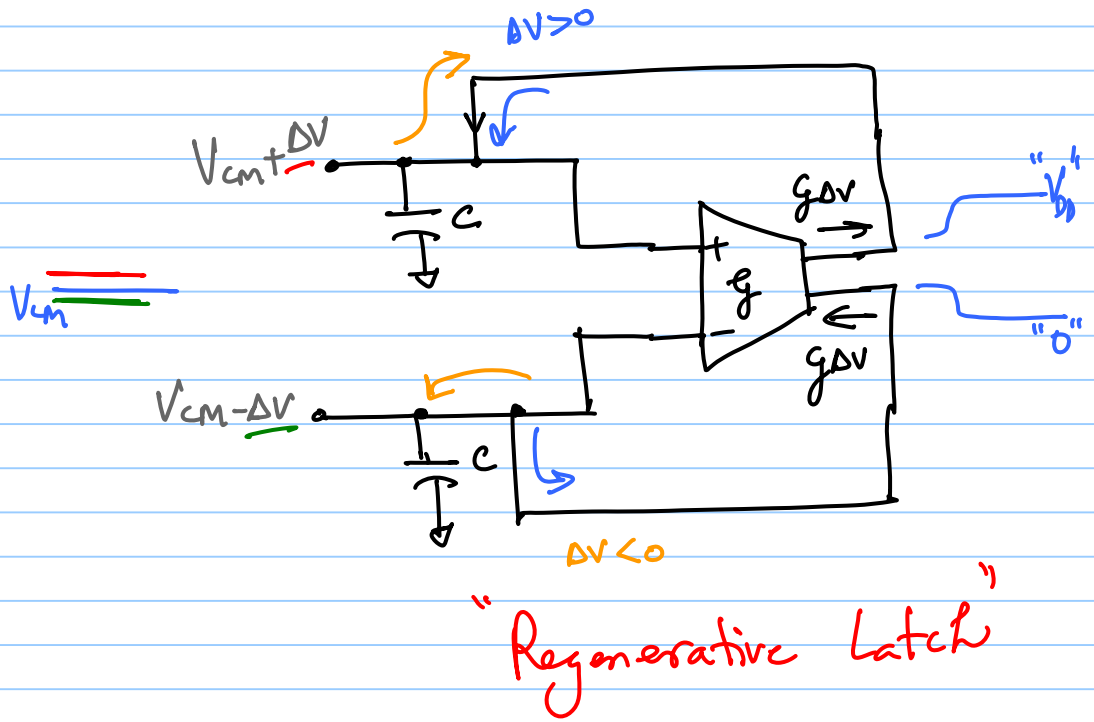


Differential Signals.



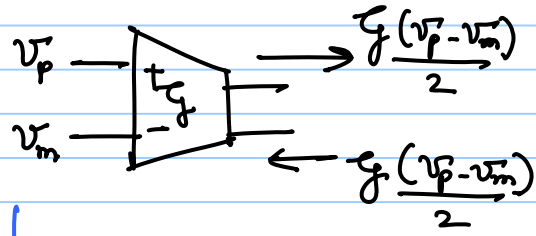
Compare the two inputs and find out if the difference is +ve or -ve.

V_{cm} ⇒ Common-mode voltage
↳ common to both the input lines.



"Regenerative Latch"

Differential Transconductor

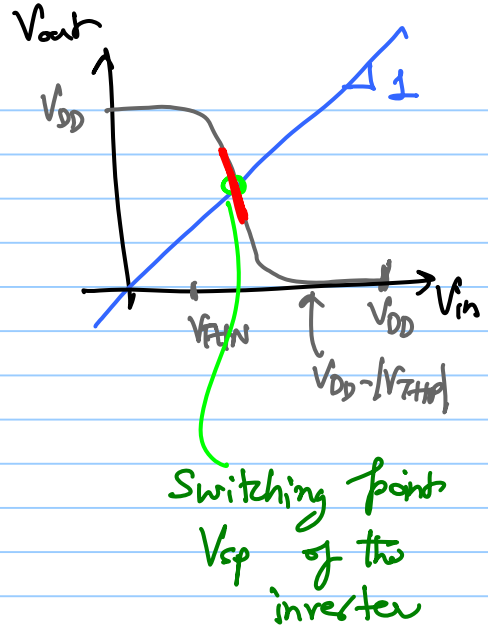


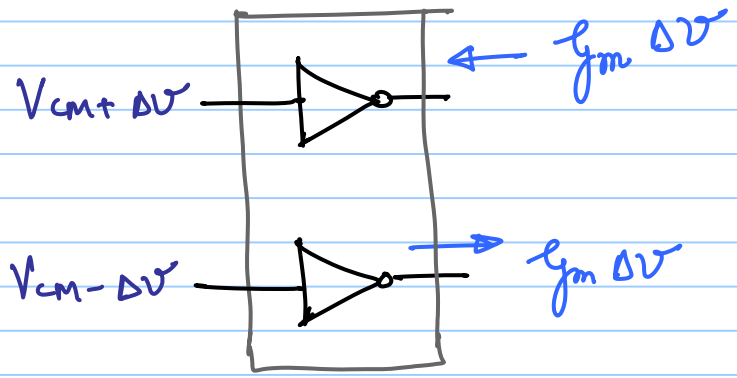
↳ Can be designed using several possible circuit topologies.

CMOS Inverter:

⇒ high gain around the switching point of the inverter

↳ bias the inverter at the switching-point
↳ trip point

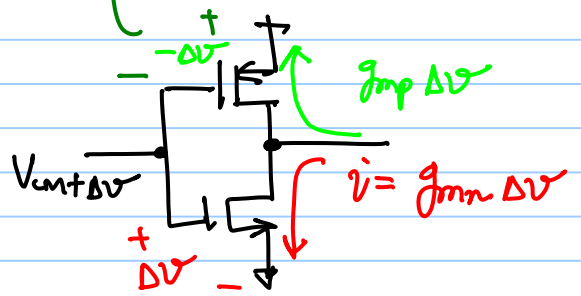




Differential G_m Circuit

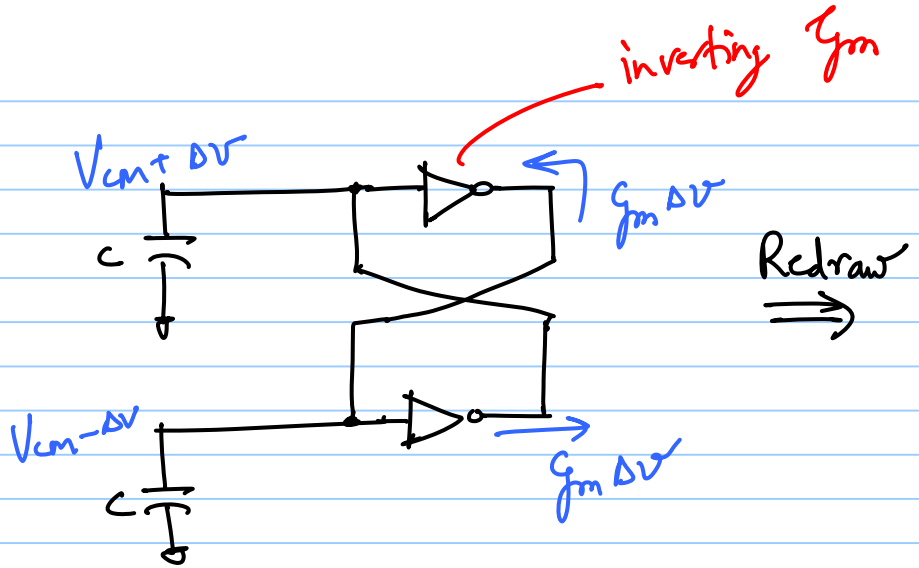
$V_{cm} \in V_{sp}$

$V_{SG} = V_{DD} - V_{cm} - \Delta V$

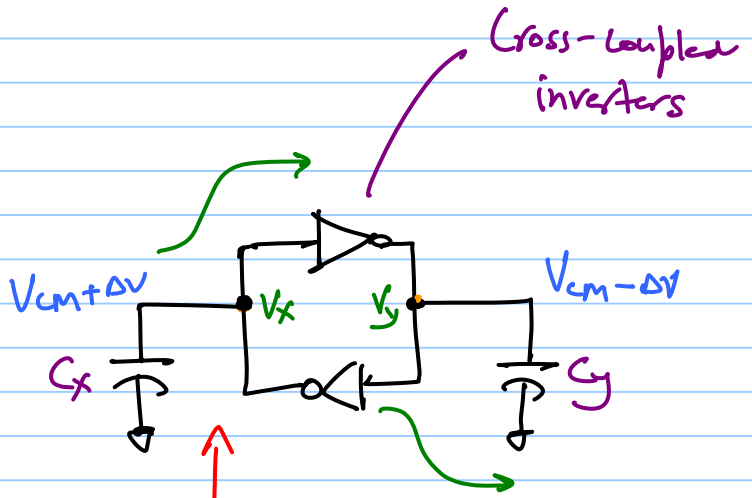


$G_m = g_{mn} + g_{mp}$

g_{mn}: NMos, g_{mp}: PMos



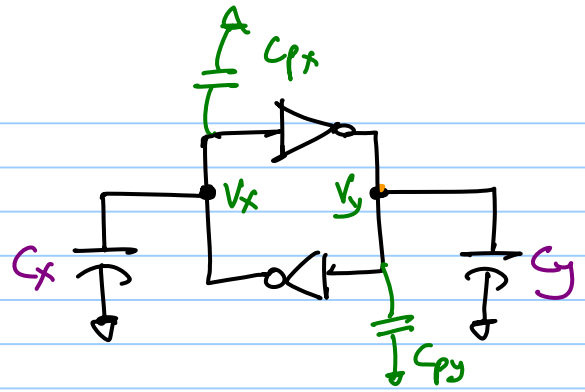
Redraw ⟹



Basic skeleton of CMOS Latch

C_x & C_y are the parasitic or loading caps on nodes x+y

$$\tau = \frac{C}{G}$$



How to speed up regeneration operation $\left(\tau_c = \frac{C}{g}\right)$

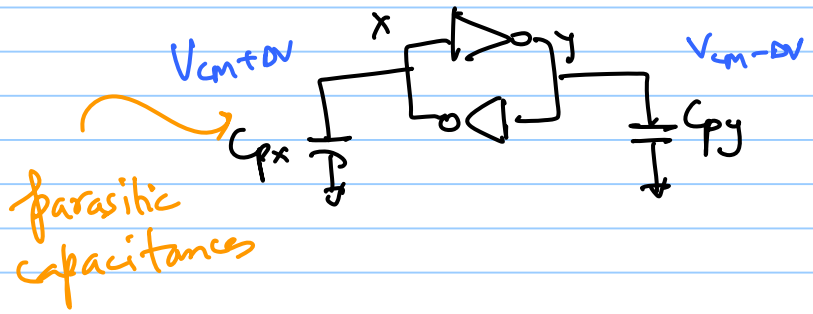
↳ increase g ↑ ⇒ also increases C_{px} & C_{py}

$$\tau_c = \frac{C + C_{px} + C_{py}}{G}$$

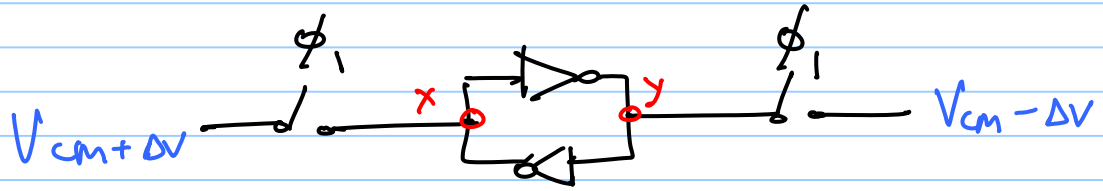
reduce C for higher speed

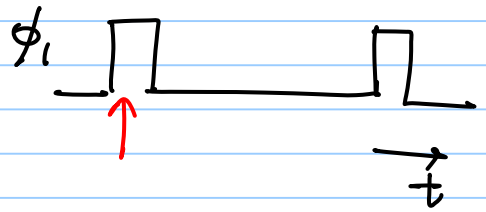
↳ remove C altogether

Cross coupled Latch

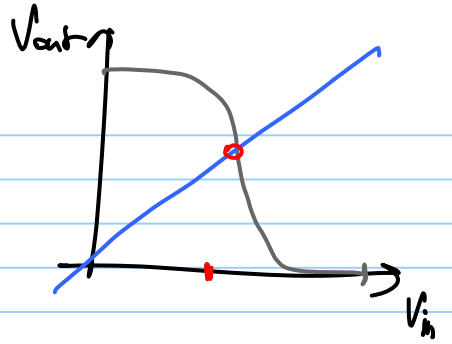


provides the best possible speed.





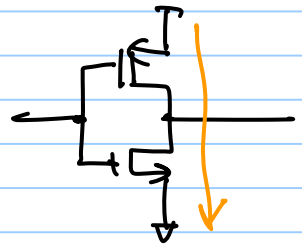
Issue :

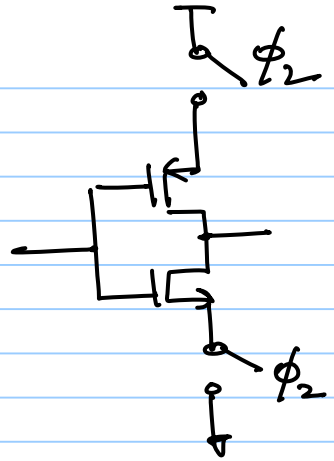


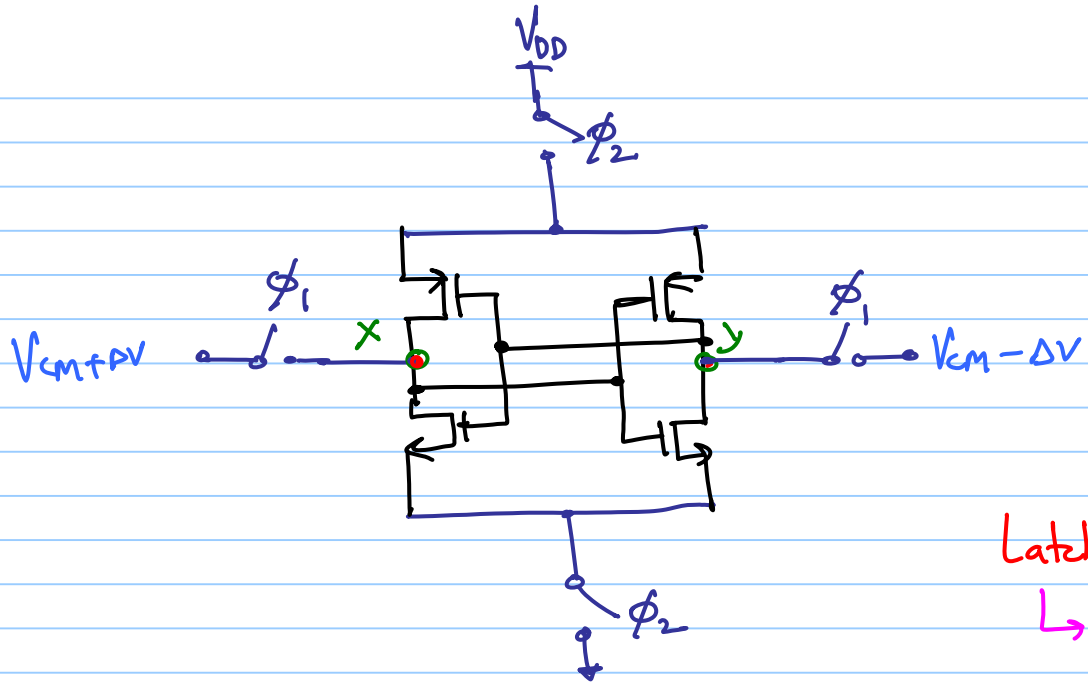
"Static power dissipation"

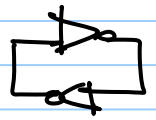
Solution : Tristate the inverter when it is not regenerating

↳ during phase ϕ_1




ϕ_2
ϕ_2

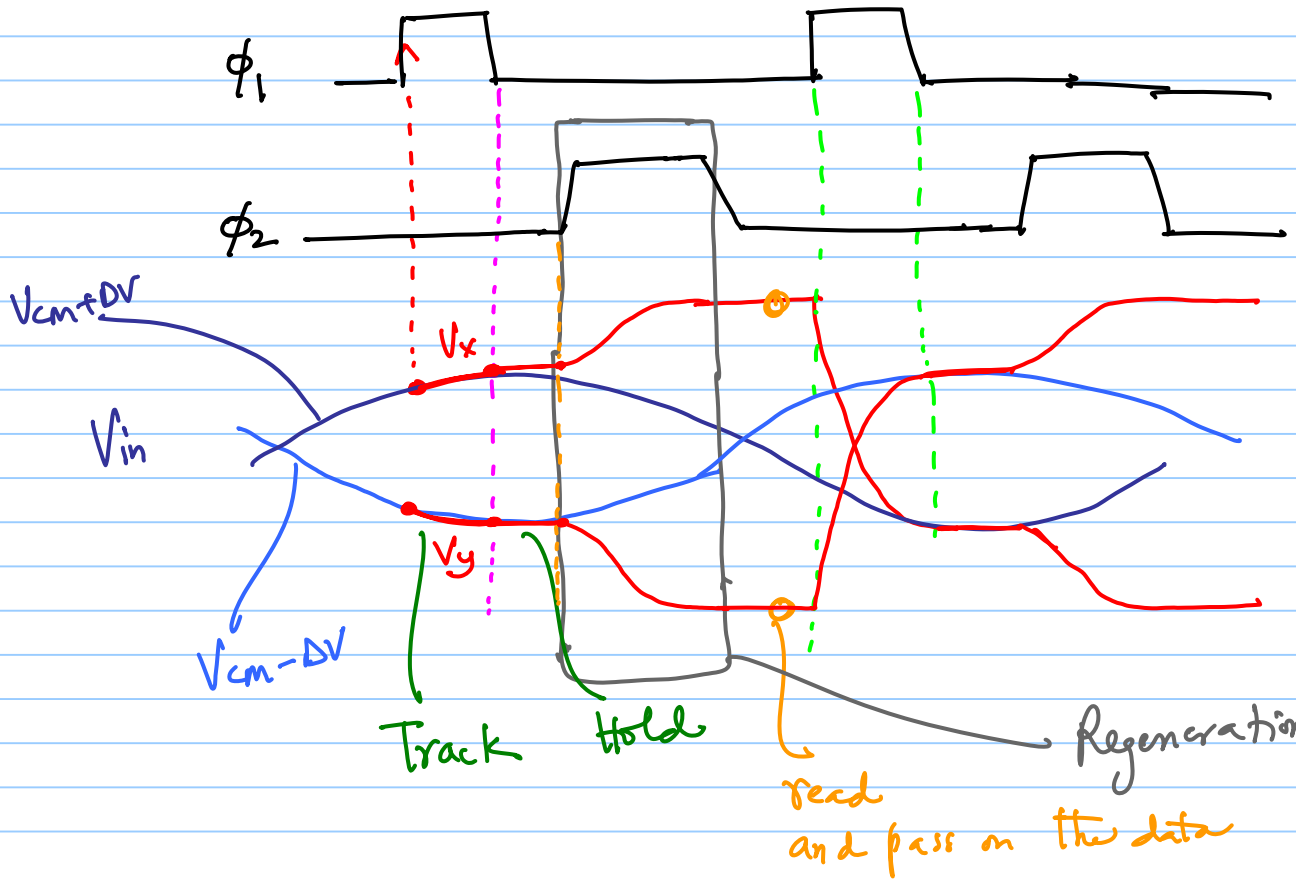




Latch is disabled when $\phi_2=0$

↳ doesn't pull any current from the V_{DD} or the inputs

Regeneration occurs when ϕ_2="1"



ϕ_1 & ϕ_2 are non-overlapping

* Sampling instant
  ↳ falling edge of ϕ_1
* outputs are valid a little time after ϕ_2 goes high
  (regeneration to complete)
  ↳
* Hold onto the data for a full clock cycle