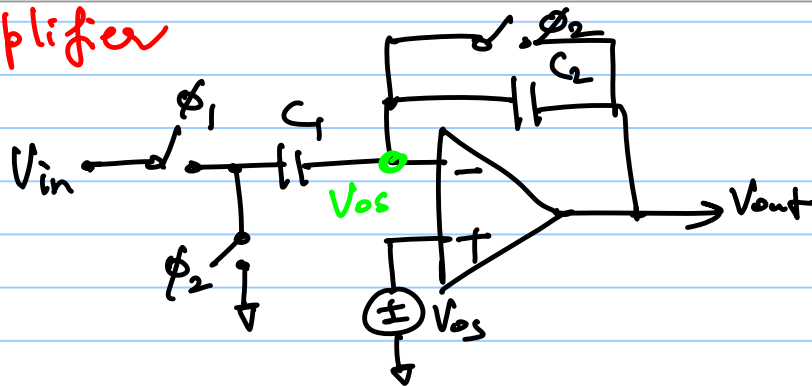


ECE 517 - Lecture 24

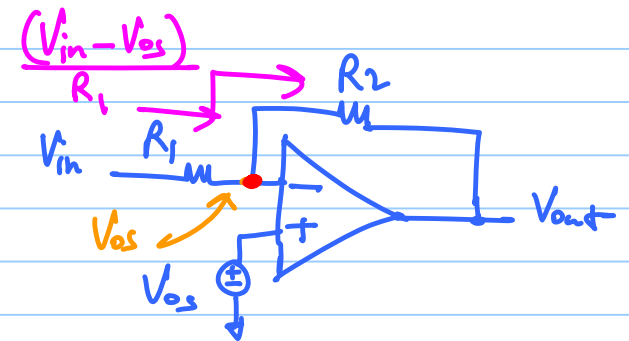
Note Title

CT Amplifier 4/13/2017

SC Amplifier

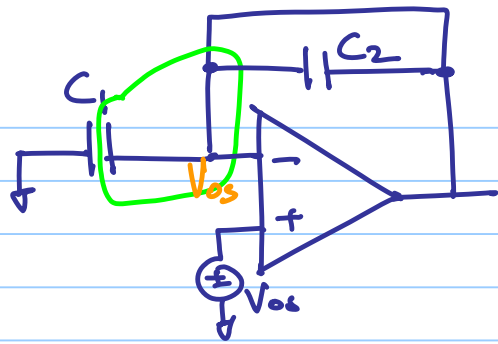


$$V_{out} = -\frac{C_1}{C_2} V_{in} + \underline{\underline{V_{os}}}$$



$$V_{out} = \underline{V_{os}} - \frac{R_2}{R_1} (V_{in} - \underline{V_{os}})$$

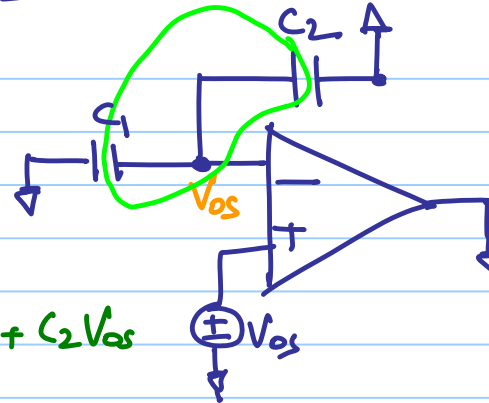
ϕ_2



$$Q = +C_1 V_{os}$$

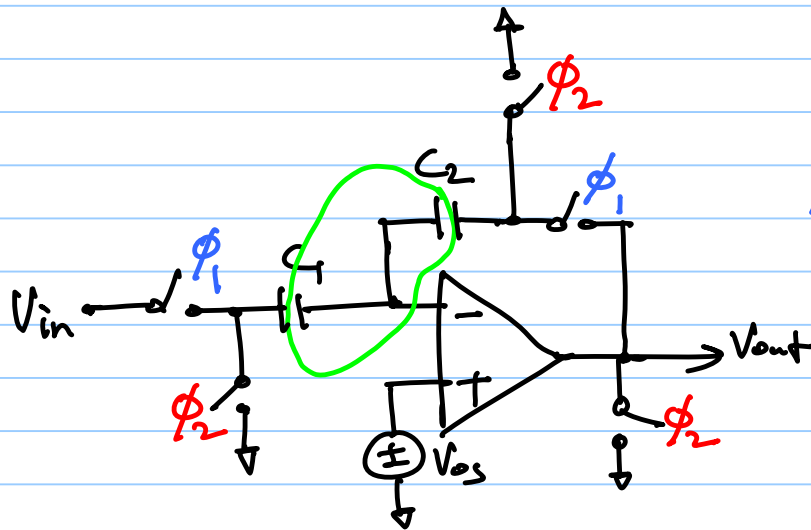
Modify $\rightarrow$

ϕ_2



$$Q = C_1 V_{os} + C_2 V_{os}$$

Different way of resetting



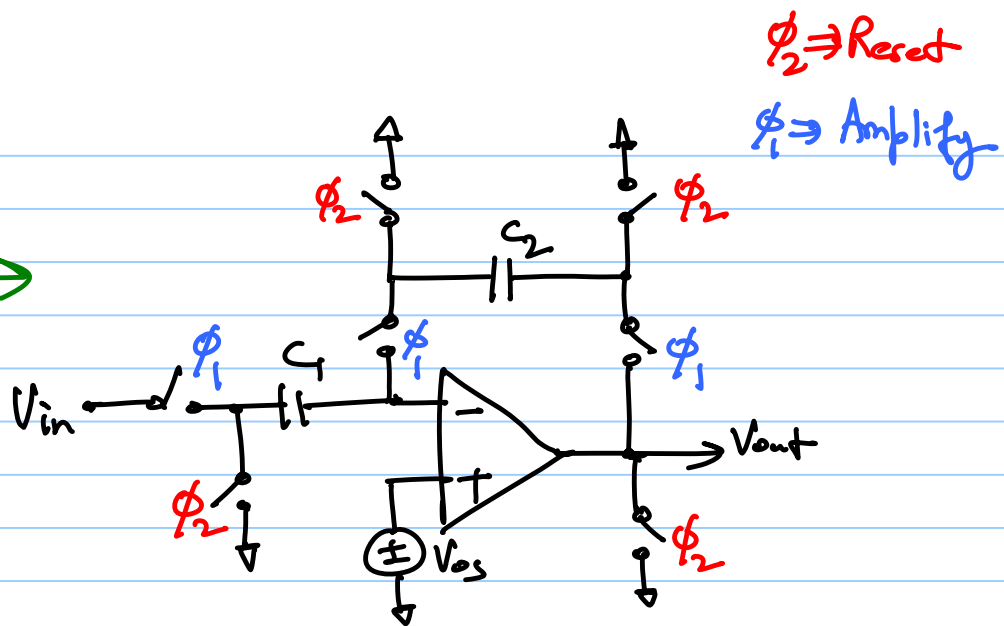
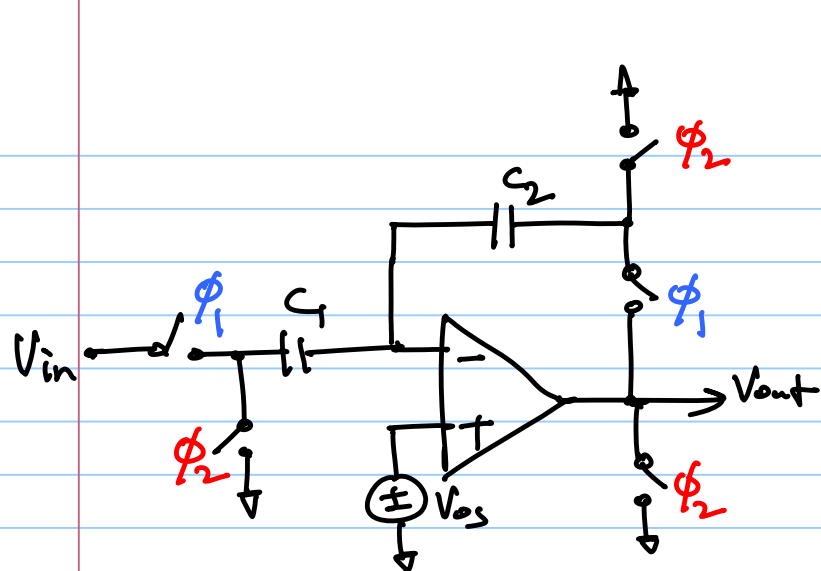
ϕ_2 :

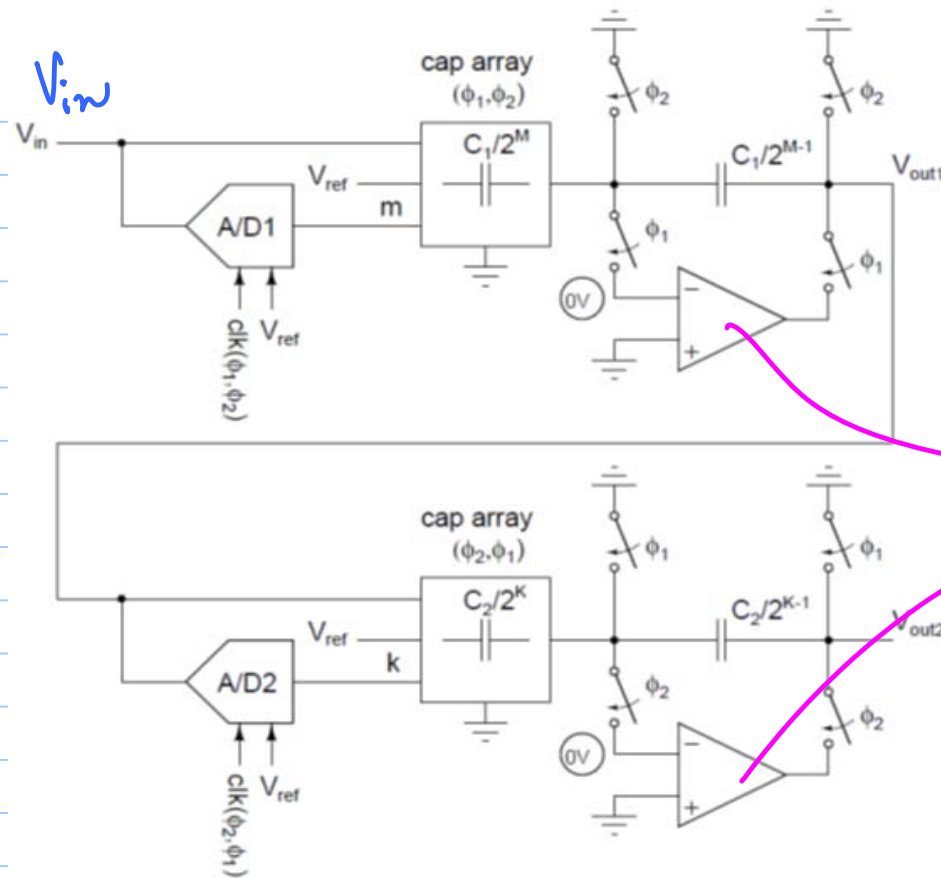
$$Q = C_1 V_{os} + C_2 V_{os}$$

$$\phi_1: -C_1(V_{in} - V_{os}) - C_2(V_{out} - V_{os})$$

$$C_1 V_{os} + C_2 V_{os} = -C_1 V_{in} + C_1 V_{os} - C_2 V_{out} + C_2 V_{os}$$

$$V_{out} = -\frac{C_1}{C_2} V_{in}$$





Stage 1

$\phi_1 \Rightarrow$ Amplify

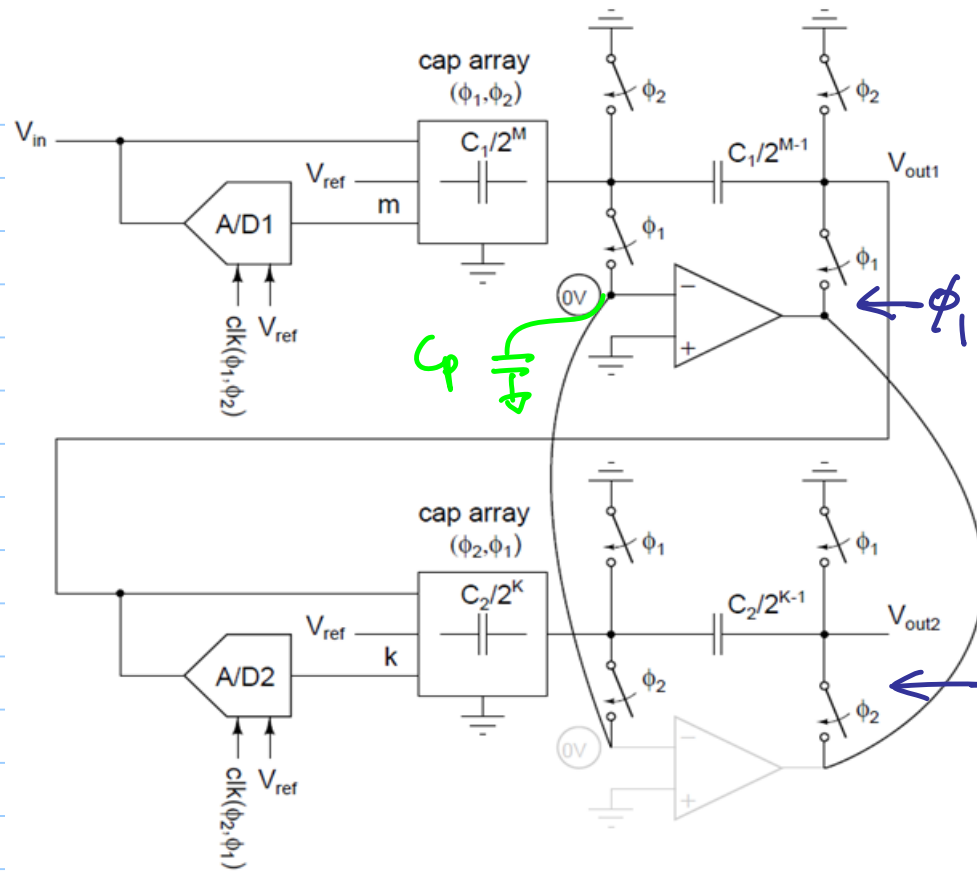
$\phi_2 \Rightarrow$ Reset

Idle during
Reset phase

Stage 2

$\phi_1 \Rightarrow$ Reset

$\phi_2 \Rightarrow$ Amplify



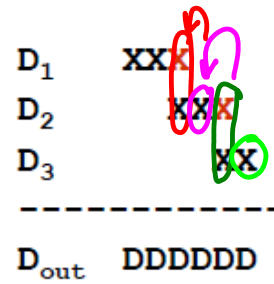
Opamp sharing

(+) Reduce Power Consumption

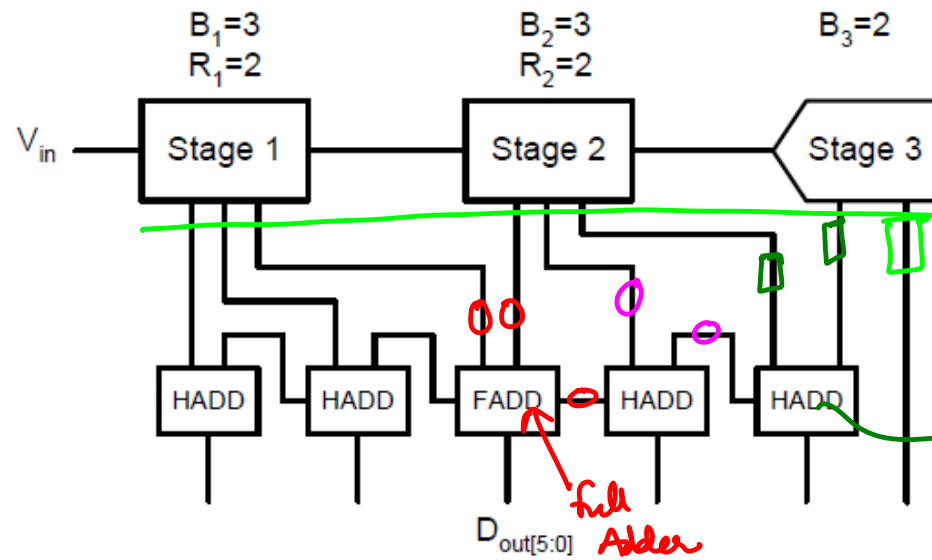
(-) Cannot correct for opamp offsets

(-) Memory effect due to charge storage at ϕ_2 -ve inputs of the opamp.

$$D_{out} = D_1 + \frac{1}{4}D_2 + \frac{1}{16}D_3$$



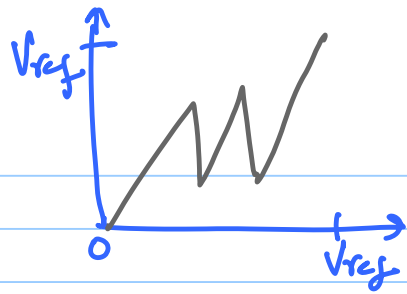
Overlap by 1-bit and add



Registers to create appropriate shifts

Half Adder

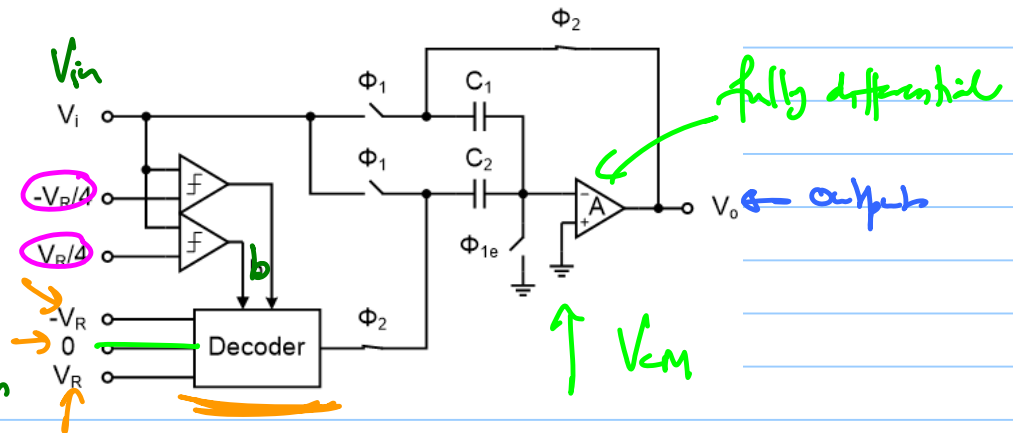
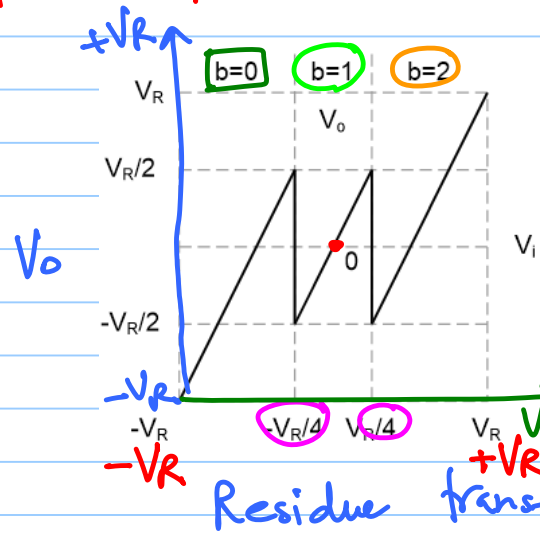
D_{out}[5:0] full Adder

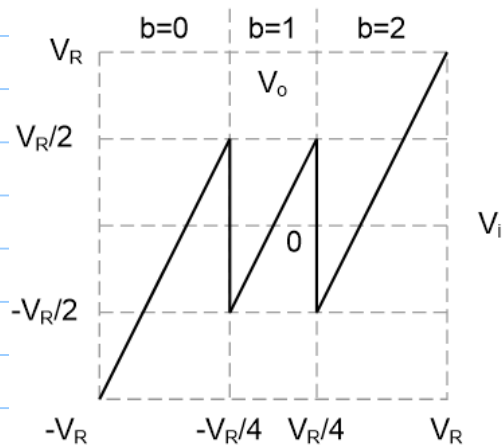
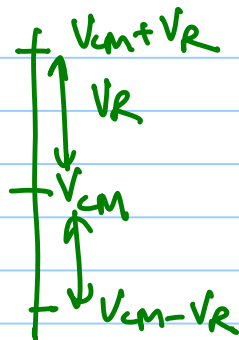
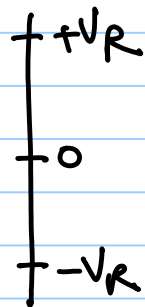


Single ended inputs

Differential inputs

* 1.5bit/stage design





Flash A/D output

	00	01	10
b	0	1	2
b-1	<u>-1</u>	<u>0</u>	<u>+1</u>
C_2	<u>$+V_R$</u>	0	<u>$-V_R$</u>

