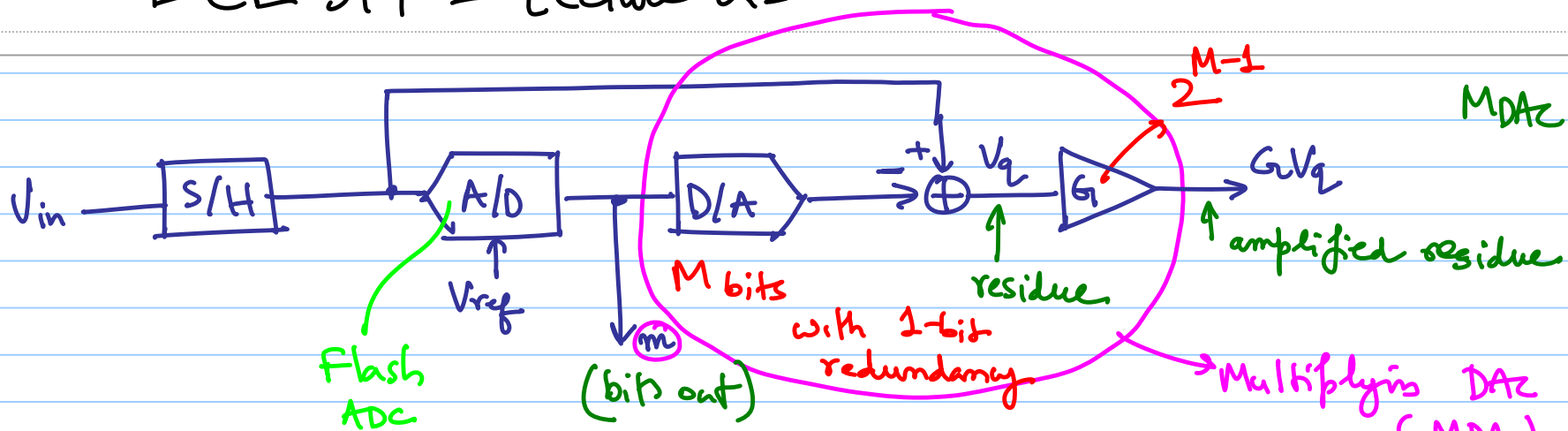
ECE 517 – Lecture 23

Note Title 4/11/2017

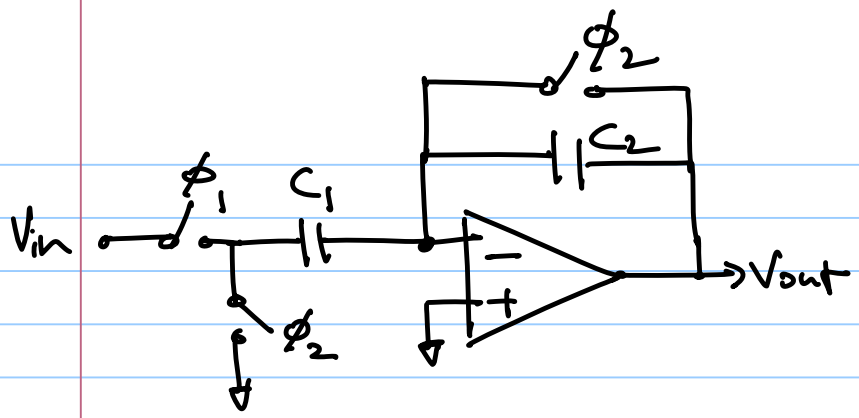


$m = \{0, 1, \ldots 2^M - 1\}$ ← code ← Integer

M ⇒ number of bits

$$m = \sum_{i=0}^{M-1} b_i 2^i$$

b_i ← binary



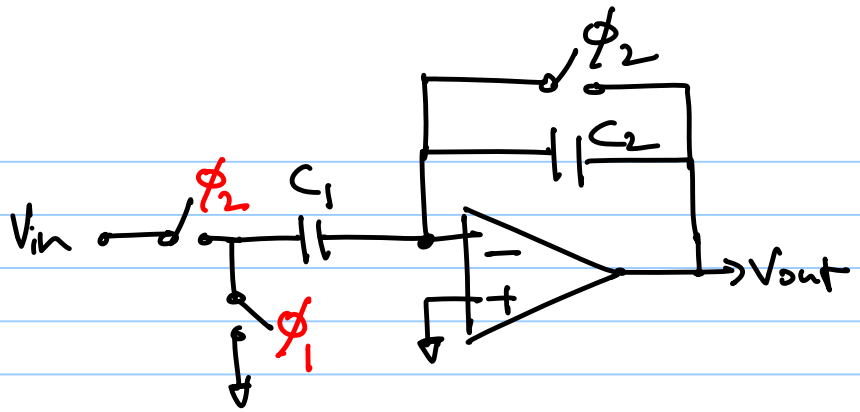
Input sampled during ϕ_1

$\phi_1 \Rightarrow$ Amplification

$\phi_2 \Rightarrow$ Reset

-ve gain

$V_{out} = -\frac{C_1}{C_2} V_{in}$



Input sampled during ϕ_2

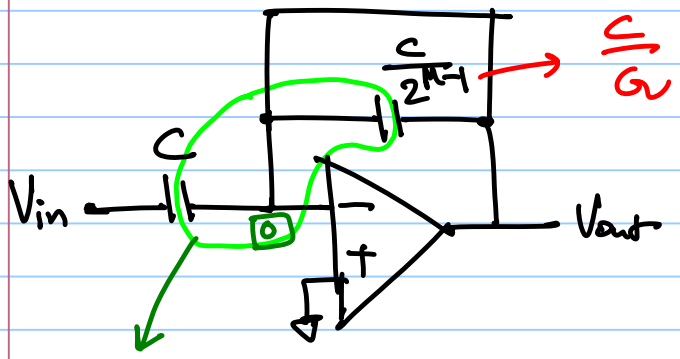
$\phi_1 \Rightarrow$ Amplification

$\phi_2 \Rightarrow$ reset

+ve gain

$V_{out} = +\frac{C_1}{C_2} V_{in}$

ϕ_2

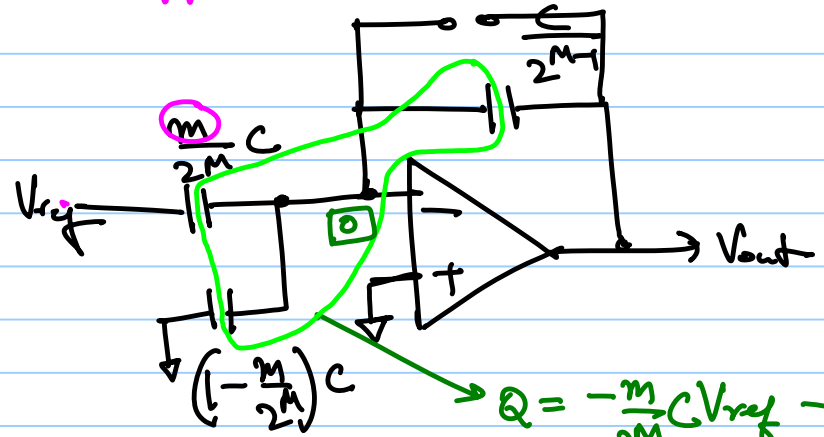


$= C_G$

$Q = -CV_{in}$

"m"

ϕ_1



$Q = -\frac{m}{2^M}CV_{ref} - \frac{C}{2^{M-1}}V_{out}$

$$-\frac{m}{2^M}CV_{ref} - \frac{C}{2^{M-1}}V_{out} = -CV_{in}$$

$$\Rightarrow \quad \frac{V_{out}}{2^{M-1}} = V_{in} - \frac{m}{2^M}V_{ref}$$

$$\Rightarrow \quad V_{out} = \underbrace{2^{M-1}}_{G}\left(V_{in} - \underbrace{m\,\frac{V_{ref}}{2^M}}_{\text{DAC output}}\right) \qquad \frac{V_{ref}}{2^M} \leftarrow V_{LSB}$$

G — gain; residue; m — digital code output from A/D$_1$

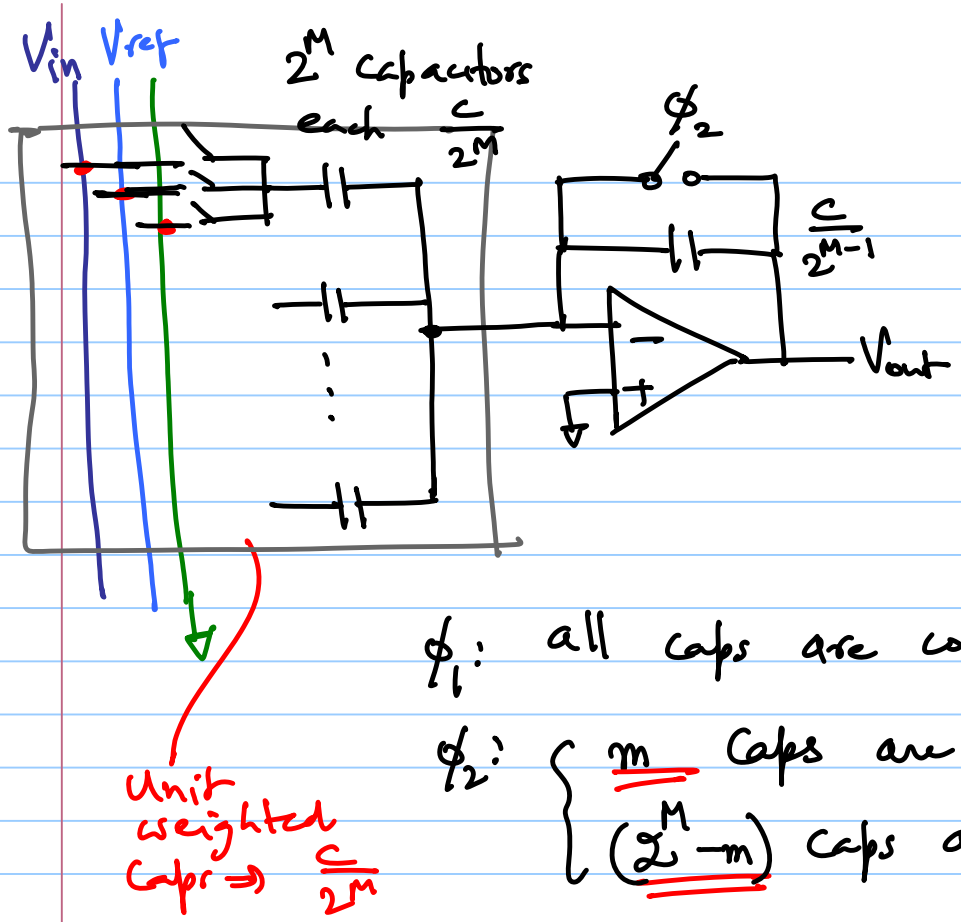
@ the end of ϕ_1:

$$V_{out} = G\left[V_{in} - m\,V_{LSB}\right]$$

← just a notation simplification

$$m = \left(\sum_{i=0}^{M-1} b_i 2^i\right) V_{LSB}$$

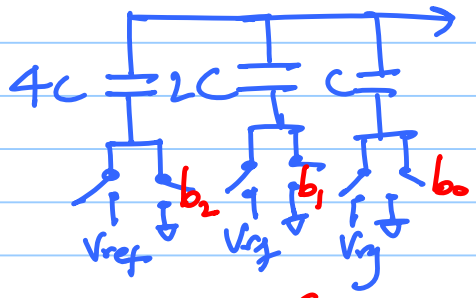
b_i ↑ bit from the flash A/D$_1$



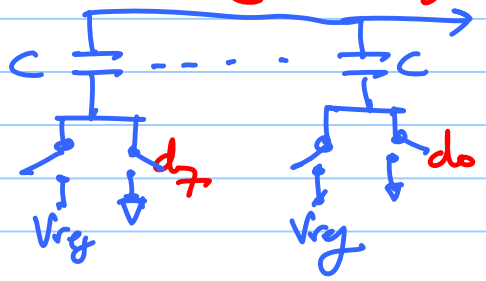
ϕ_1: all caps are connected to V_{in}

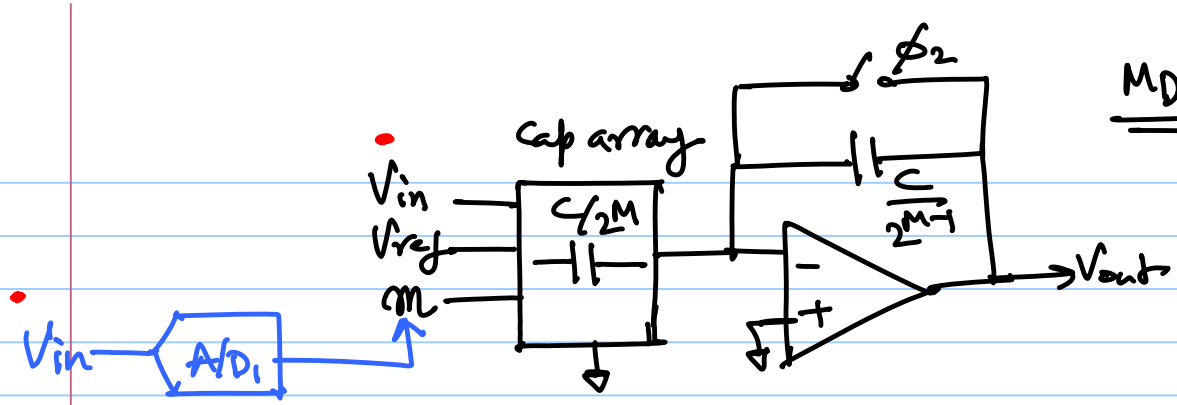
ϕ_2: $\begin{cases} m \text{ Caps are connected to } V_{ref} \\ (2^M - m) \text{ caps are connected to gnd} \end{cases}$

3 bits DAC (binary weighted)

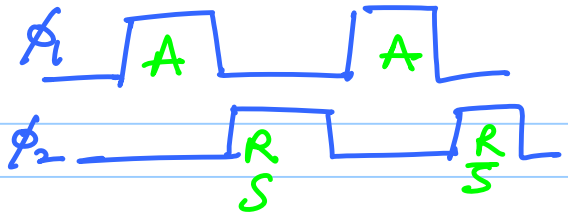


(Unit weighted)

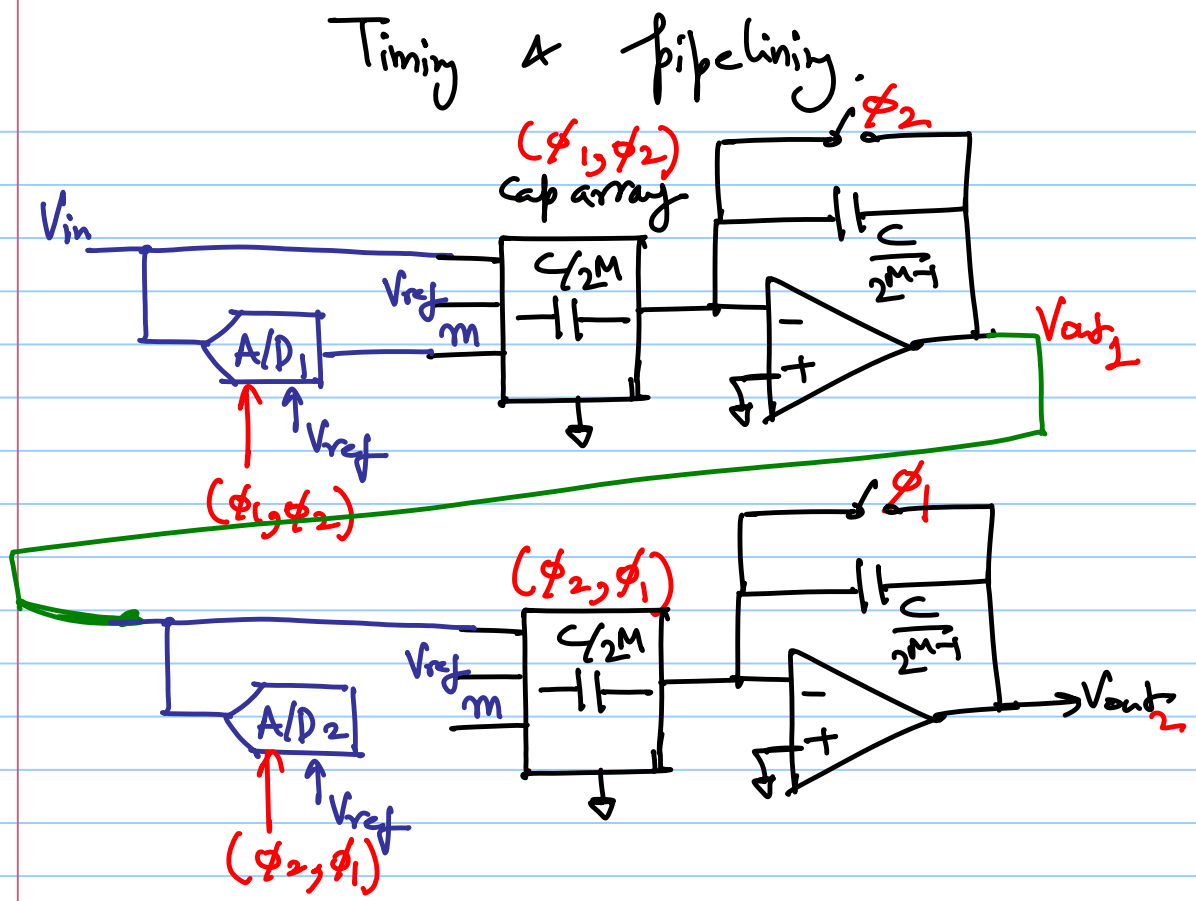




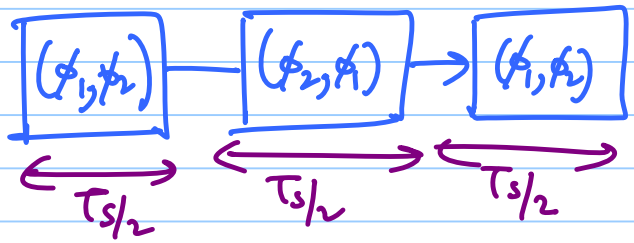
MDAC



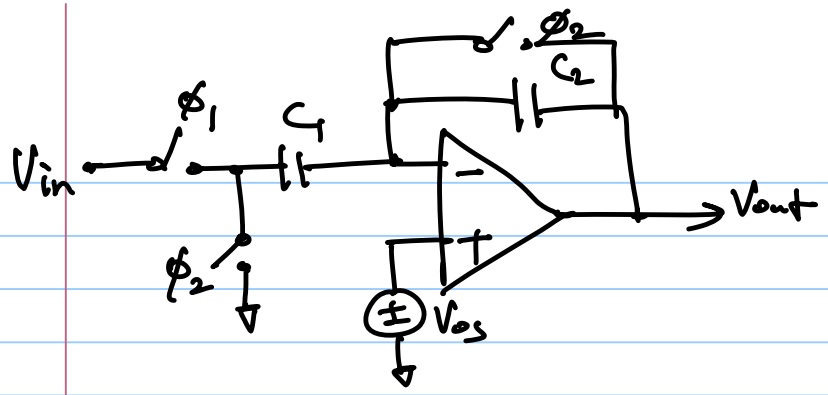
Timing & pipelining



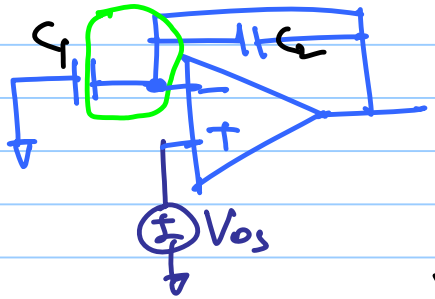
* Half clock period for each stage in the pipeline



Minimize the Latency



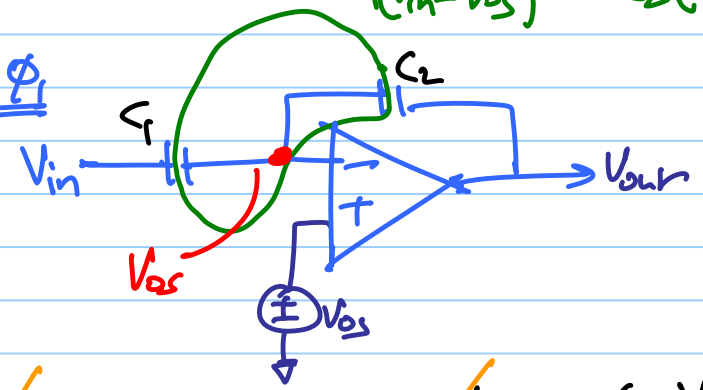
ϕ_2



$Q_2 + C_1 V_{os} =$)

$-C_1(V_{in} - V_{os}) - C_2(V_{out} - V_{os})$

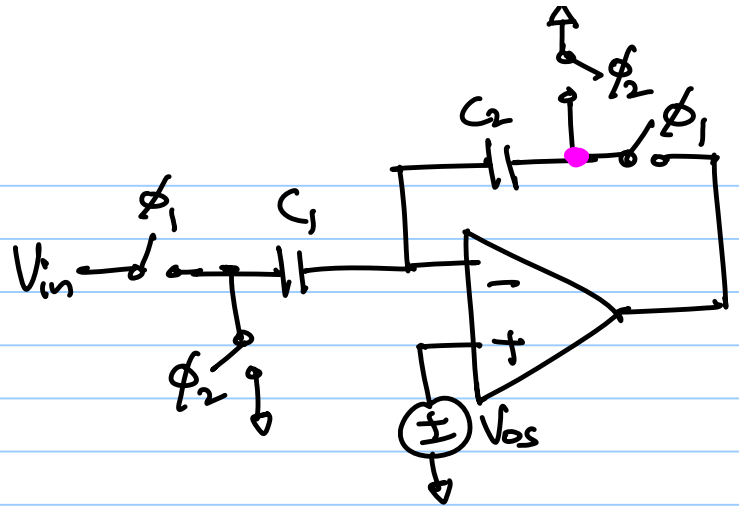
ϕ_1



Input offset is stored & cancelled

$C_1 V_{os} = -C_1 V_{in} + C_1 V_{os} - C_2 V_{out} + C_2 V_{os}$

$V_{out} = -\frac{C_1}{C_2} V_{in} + V_{os}$ ← output offset


ϕ_2
C_2
ϕ_1
ϕ_1
C_1
V_{in}
$-$
$+$
ϕ_2
$\pm$
V_{os}