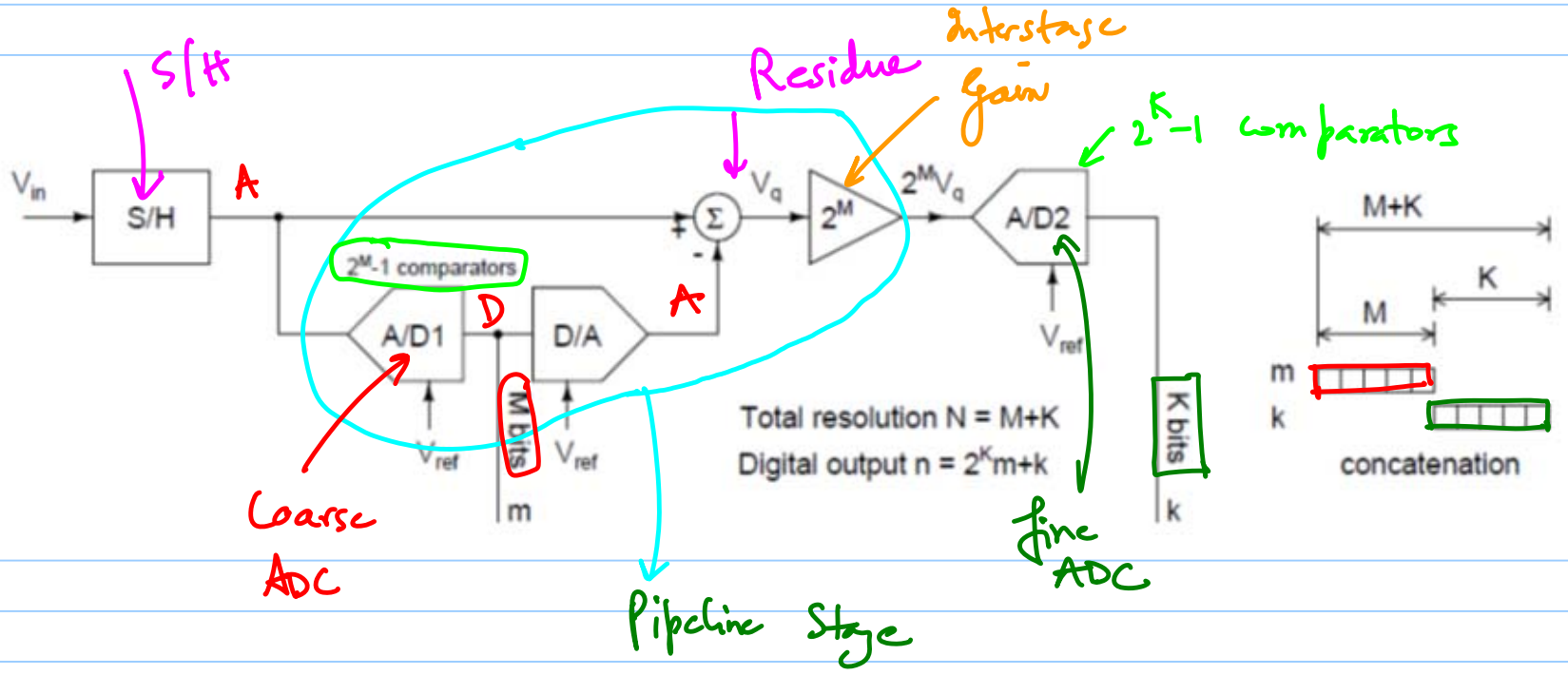
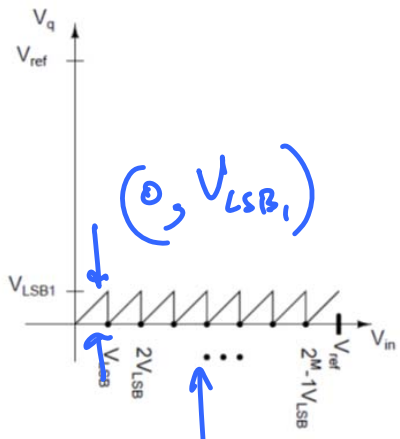
ECE 517 – Lecture 22

Note Title 4/6/2017

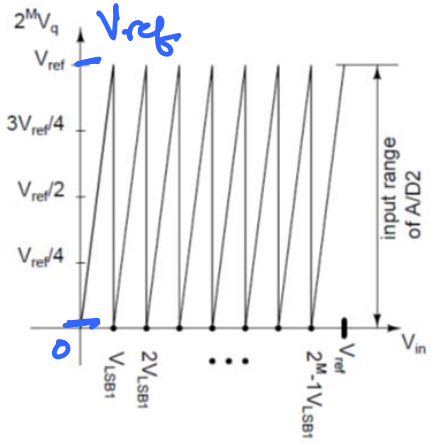


Ideal



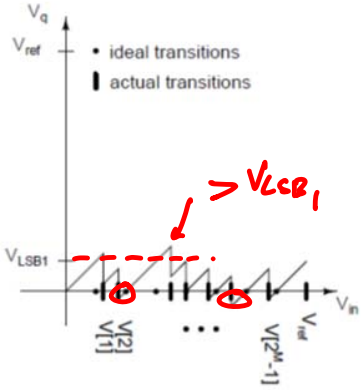
$(0, V_{LSB_1})$

residue

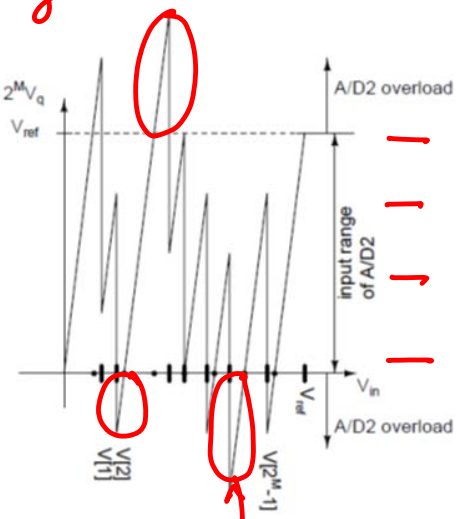


Vref

Reality



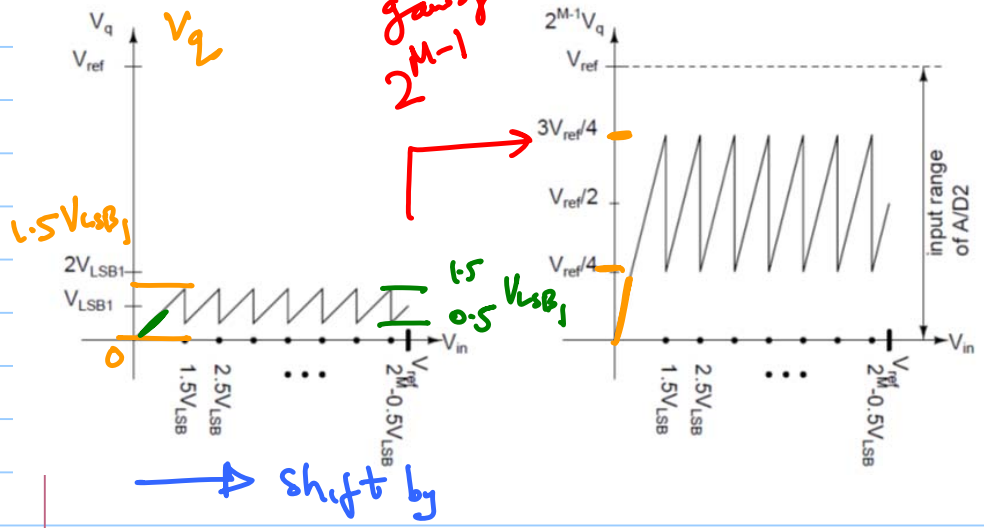
$> V_{LSB_1}$



↳ Drop the gain to 2^{M-1} from 2^M & make V_q look positive

missing transitions in the overall ADC response

Ideal



V_q

gain of 2^{M-1}

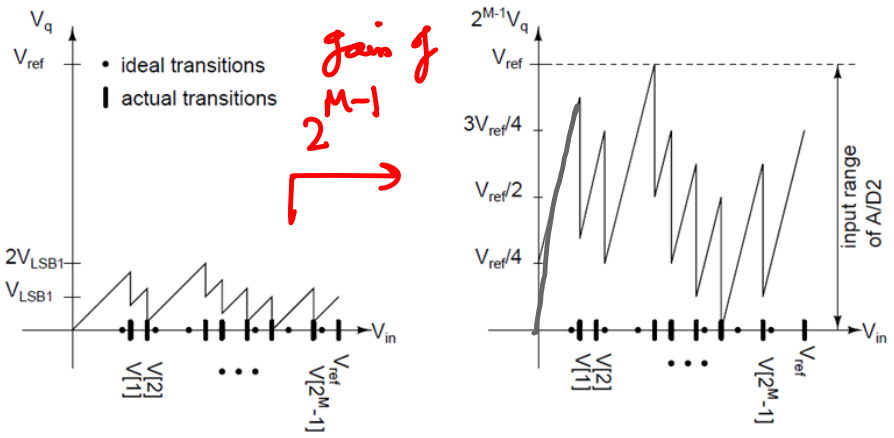
$1.5V_{LSB_1}$

1.5 0.5 V_{LSB_1}

shift by

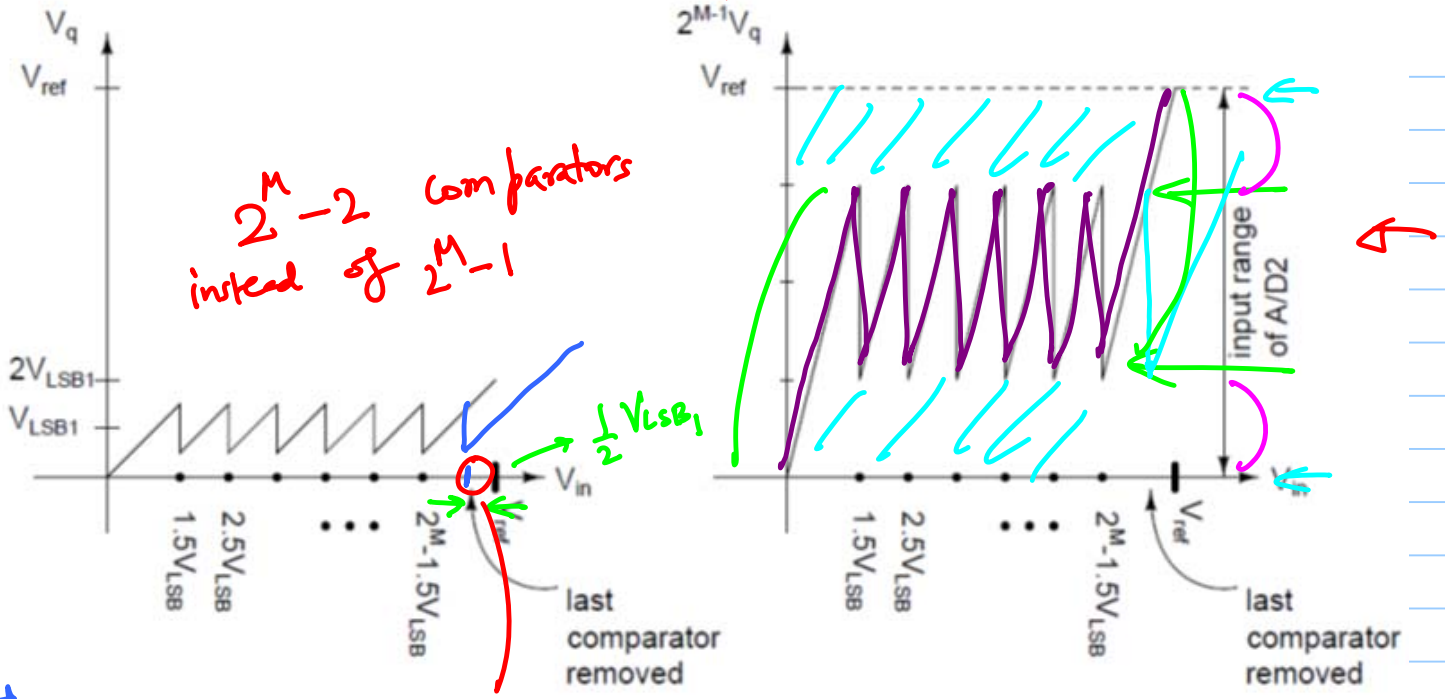
$0.5\ LSB_1$

With error upto 0.5 LSB in A/D_1



* We shifted the references (transitions) for A/D_1 by $\pm V_{LSB_1}$
  ↳ changes the reference generation

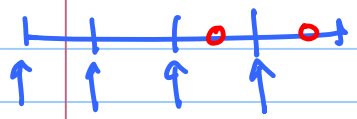
"Save 1 comparator"



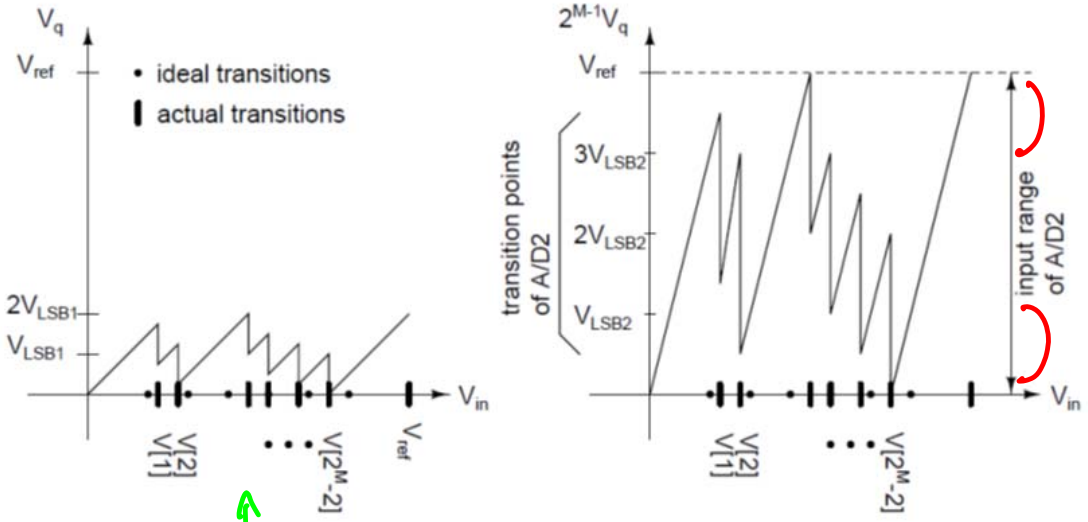
$2^M - 2$ comparators instead of $2^M - 1$

$\frac{1}{2} V_{LSB_1}$

removed the last comparator



LSB, V_{LSB}



errors $\leq \pm \frac{1}{2}$ LSB

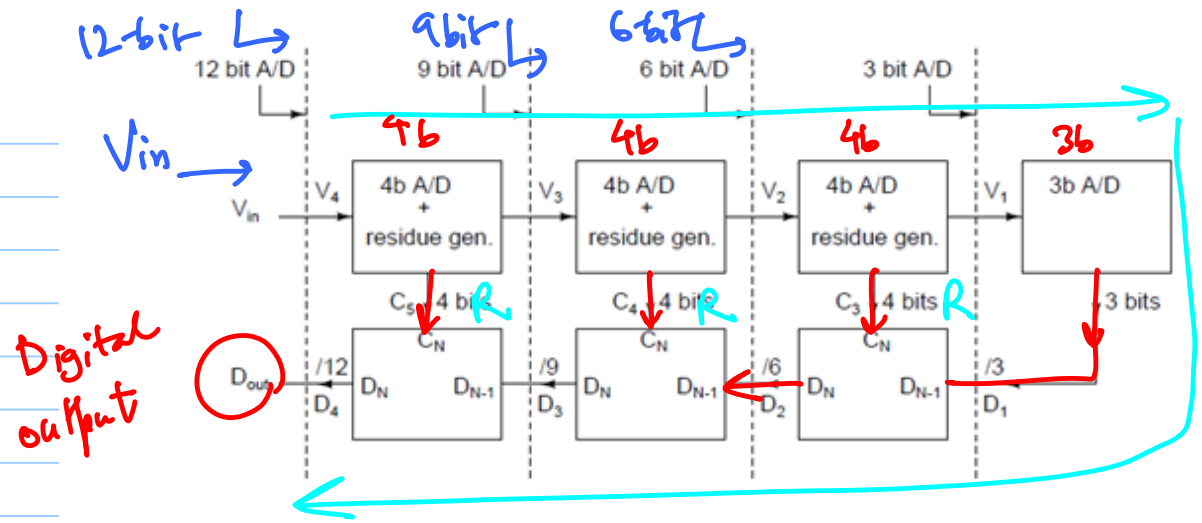
M bits → $2^M - 2$ comparators | 2 comparators ← 1.5 bit

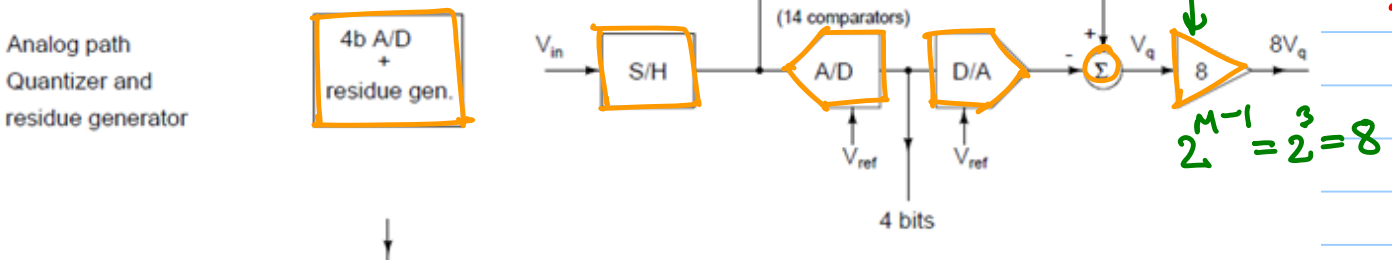
without redundancy (M-1) bits → $2^{M-1} - 1$ comparators | 1 comparator ← 1 bit

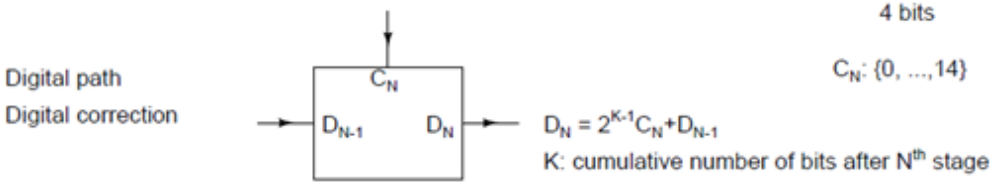
0.5 bit redundancy

Let M=2 :

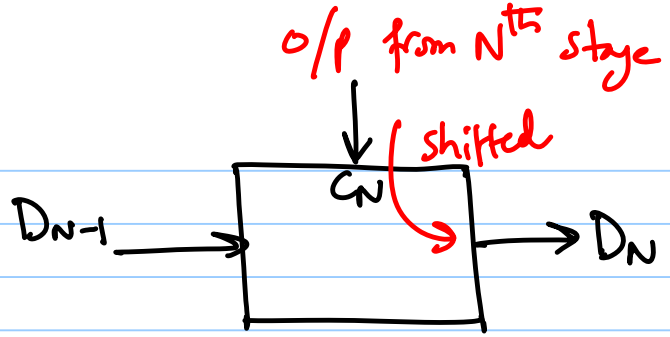
M	
2	1.5 bit stage
3	2.5 bit stage
4	3.5 bit stage







- Example:
  - * 12-bit Pipelined ADC Design
  - * 4-stages
    4-4-4-3
  - * effectively 3-bits per stage



bit shifting by k-1

$$D_N = 2^{k-1} C_N + D_{N-1}$$

k ⇒ cumulative number of bits after N^{th} stage

Q: Large # of stages or More bits per stage?!

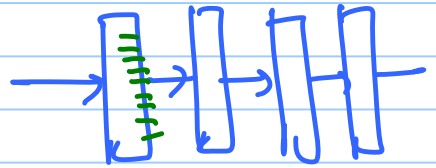
* Large # of stages ⇒ fewer bits per stage
  - ↳ fewer comparators → low accuracy (Large LSB size)
    - ↳ lower power
  - ↳ large number of amplifiers → more opamps → higher power consumption
  - ↳ Larger Latency

* fewer stages, more bits per stage

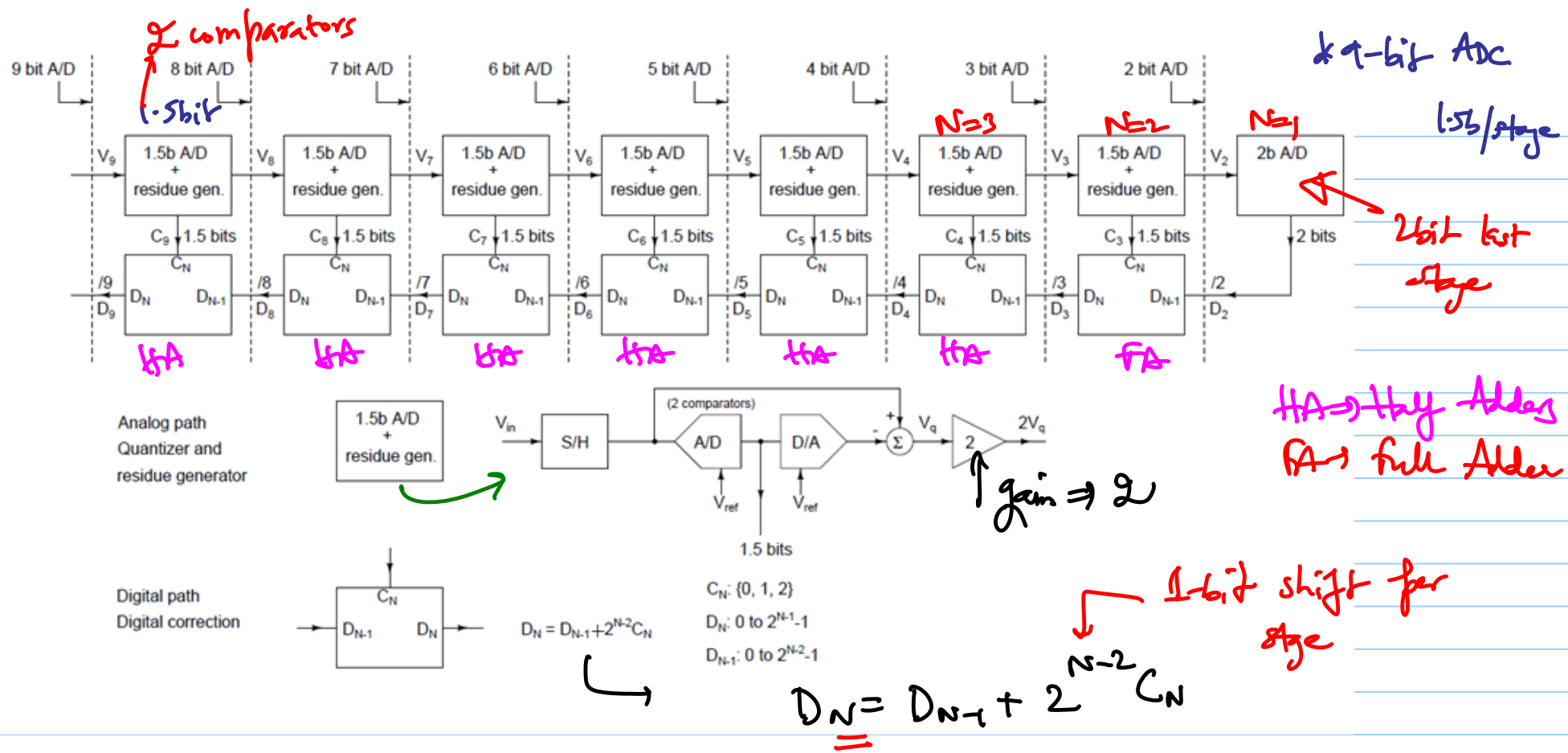
↳ More comparators, higher accuracy designs (lower offset)

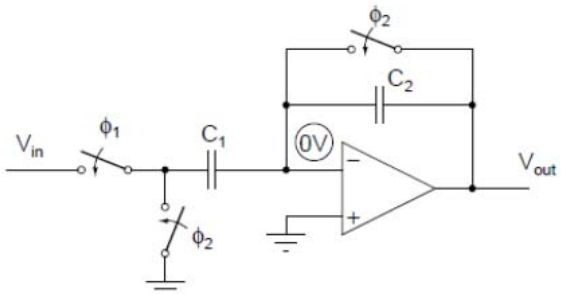
↳ Smaller # of amplifiers ⇒ less # of amps → lower power

↳ Smaller latency

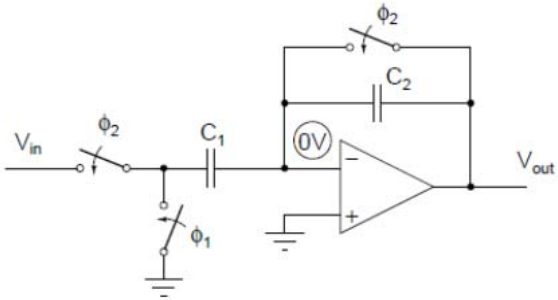


Typically ⇒ 3-4 bits per stage design is manageable

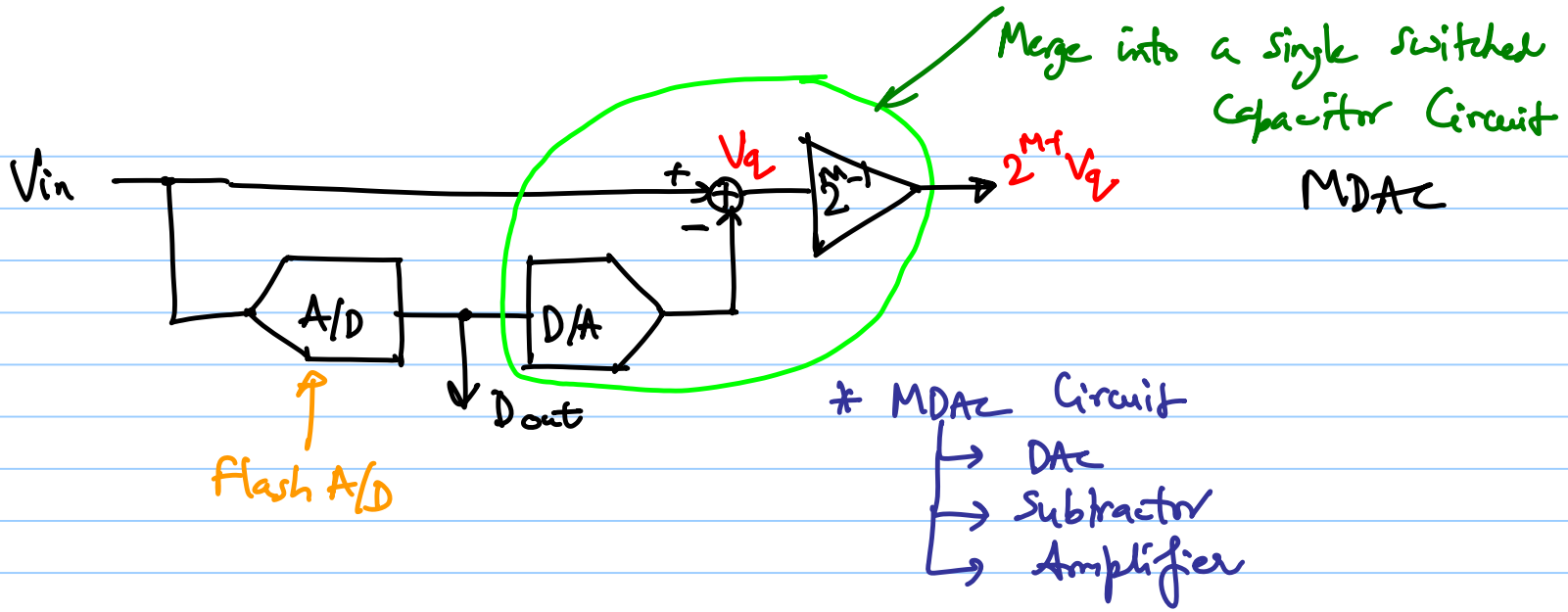

9 bit A/D
8 bit A/D
7 bit A/D
6 bit A/D
5 bit A/D
4 bit A/D
3 bit A/D
2 bit A/D
2 comparators
1.5bit
k-q-bit ADC
1.5b/stage
N=3
N=2
N=1
1.5b A/D + residue gen.
2b A/D
2bit last stage
1.5 bits
2 bits
HA
FA
Analog path
Quantizer and residue generator
S/H
A/D
D/A
(2 comparators)
gain ⇒ 2
1.5 bits
Digital path
Digital correction
HA=Half Adder
FA=Full Adder
1-bit shift per stage
$D_N = D_{N-1} + 2^{N-2} C_N$
C_N: {0, 1, 2}
D_N: 0 to $2^{N-1}-1$
D_{N-1}: 0 to $2^{N-2}-1$



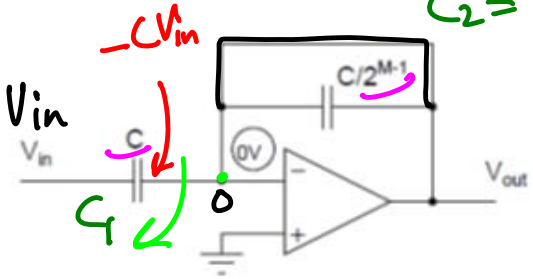
$V_{out} = -(C_1/C_2)V_{in}$



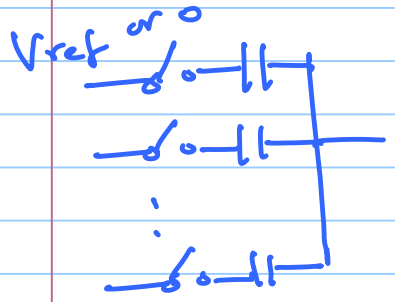
$V_{out} = +(C_1/C_2)V_{in}$

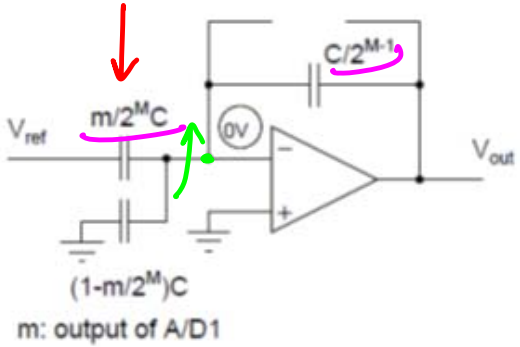


* MDAC Circuit
  - DAC
  - Subtractor
  - Amplifier



$C_2 = \frac{C_1}{2^{M-1}} \Rightarrow$ gain of 2^{M-1}





gain of 2^{M-1}

Gain — DAC

$$V_{out} = 2^{M-1}\left(V_{in} - m\cdot\frac{V_{ref}}{2^M}\right)$$

Sub