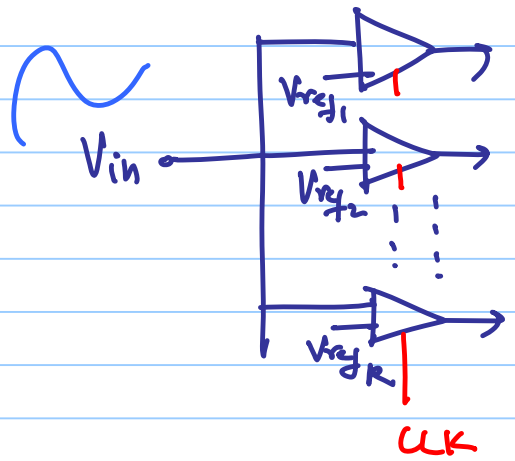
ECE 517 - Lecture 12

Note Title 2/23/2017

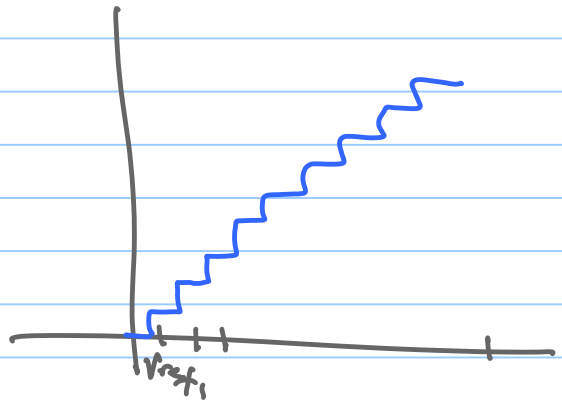


for N-bits → $2^N - 1$ comparators

3 → 7

4 → 15

5 → 31



↳ not very power & Area efficient

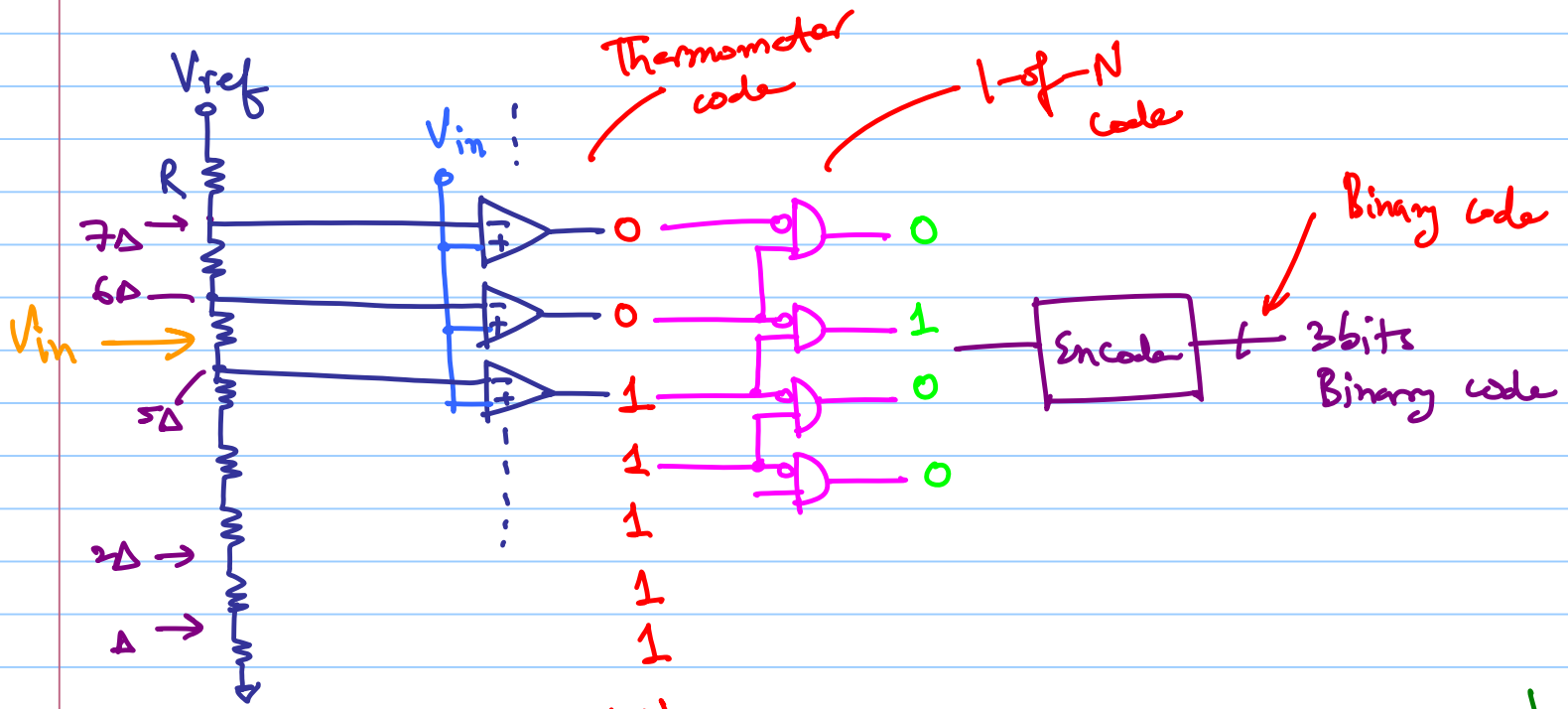
↳ used where we need low latency

$N \geq 4$

$V_{LSB} \rightarrow \sigma_{os,comp}$

3-bit flash ADC Example

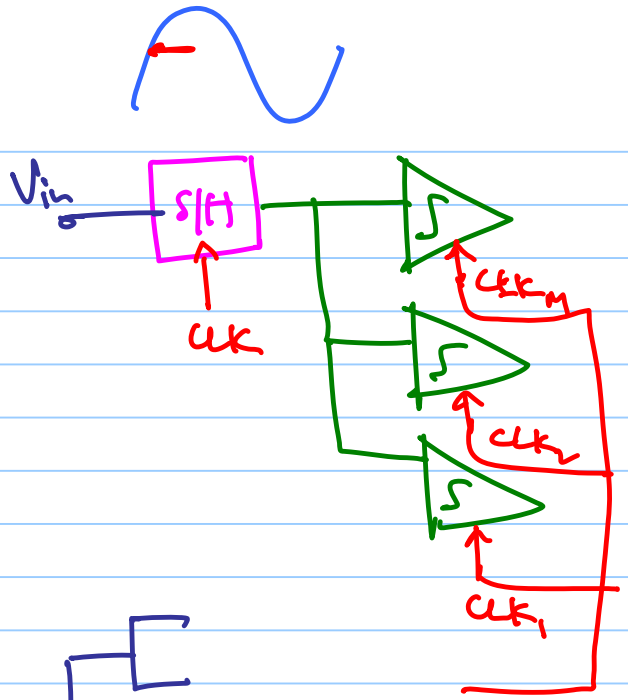
$2^N - 1$ comparators



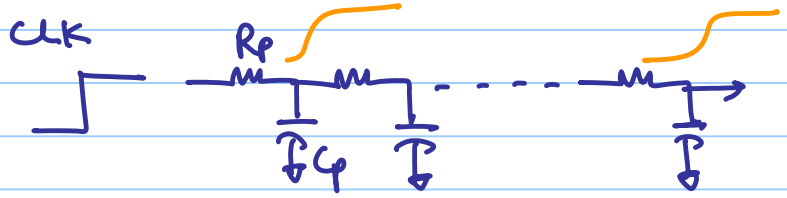
Δ → LSB size

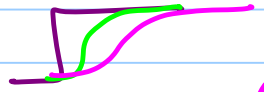
$(2^N - 1)$ bits

Digital backend → only one transition if everything works

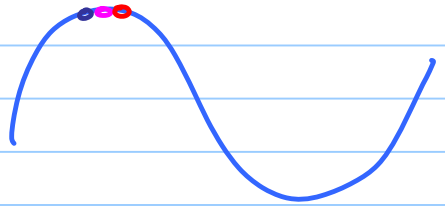


Clock Tree

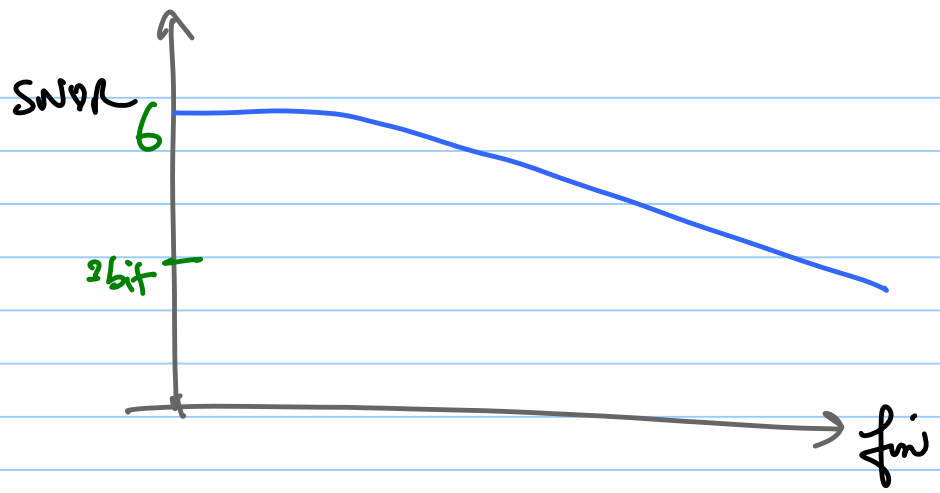


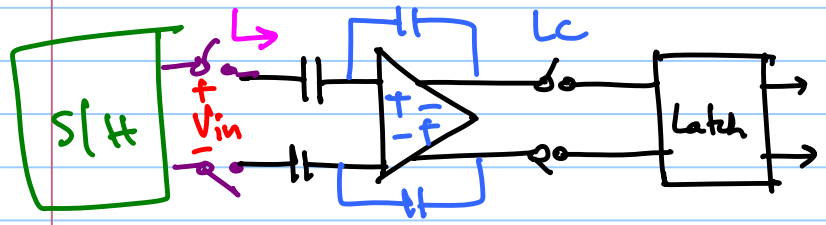


Clock skew



↳ clock skew is a serious problem at high frequencies

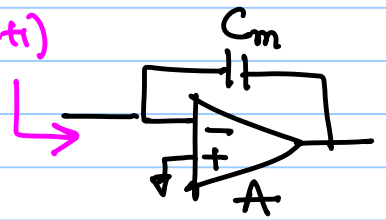

SNDR
6
2bit
fin



Buffering to drive the input Cap of the comparators

Miller Cap

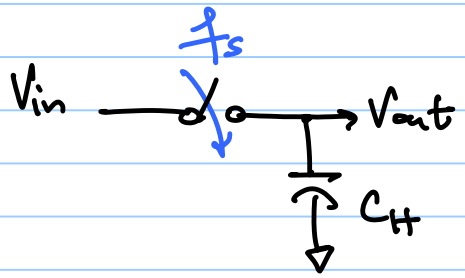
Cm(Adi)

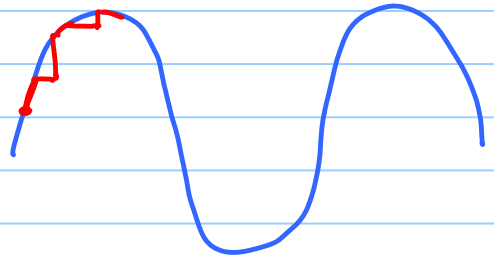


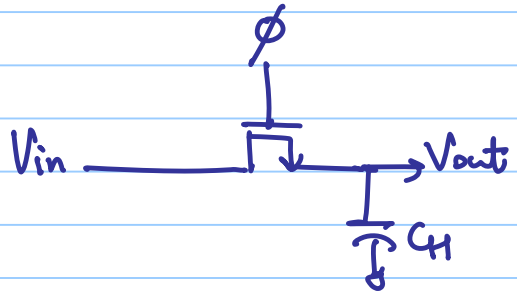
Input capacitance of the preamp is variable

Lin is not "clean"

Sample and Hold

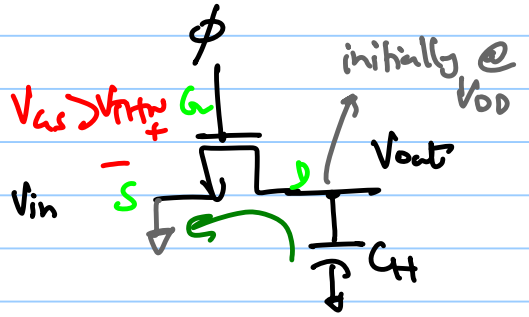


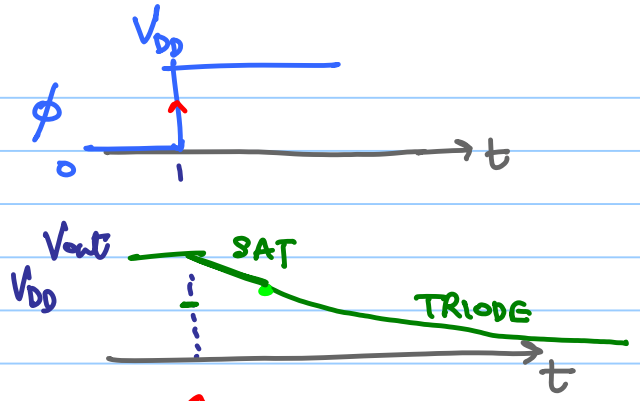




SAT

$V_{DS} > V_{GS} - V_{TH}$





$V_{GS} = V_{DD}$

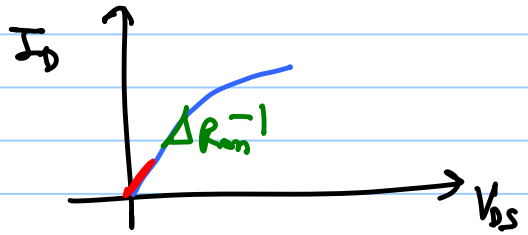
$V_{DS} = V_{DD}$

SAT: $I_D = \frac{K_n W}{2 L} (V_{GS} - V_{THN})^2$

TRIODE: $I_D = K_n \frac{W}{L} \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$

$$R_{ON} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{1}{K_n \frac{W}{L} (V_{DD} - V_{THN} - V_{DS})}$$

$V_{DD} - V_{THN} - V_{DS} = V_{GS}$

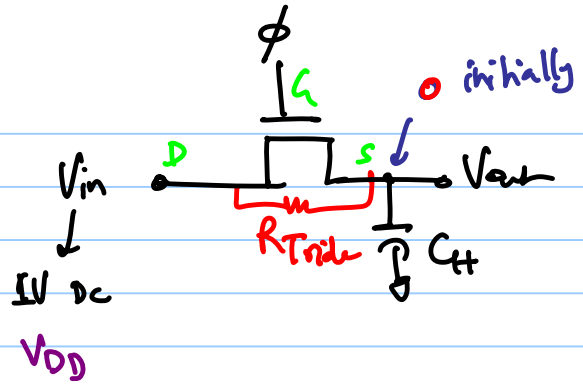


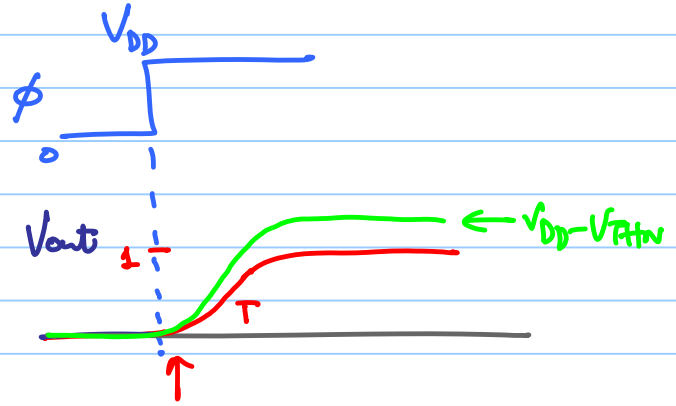
$$V_{DS} \ll \underbrace{V_{DD} - V_{TH}}_{V_{DS,sat}}$$

Deep Triode: $R_{on} \approx \dfrac{1}{k_n \frac{W}{L}(V_{GS} - V_{TH})}$

V_{DD}

$R_{off} =$ subthreshold behavior





$V_{THN} = 1V$

NMOS is not good at passing V_{DD}

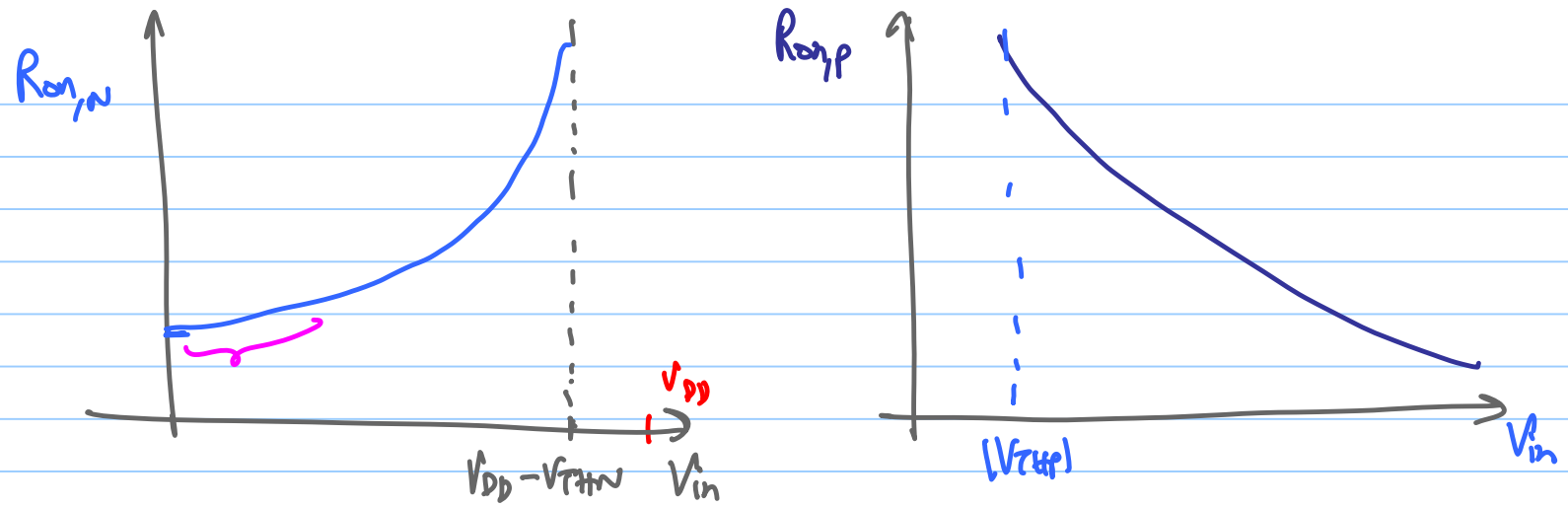
$V_{GS} = V_{DD} = 3V$

$V_{DS} = 1V$

NMOS switch doesn't pass full signal level till V_{DD}

$$R_{on} = \frac{1}{K_n \frac{W}{L} (V_{DD} - V_{in} - V_{THN})}$$

V_{GS}


$R_{on,N}$
V_{DD}
$V_{DD}-V_{TH,N}$
V_{in}
$R_{on,P}$
$|V_{TH,P}|$
V_{in}