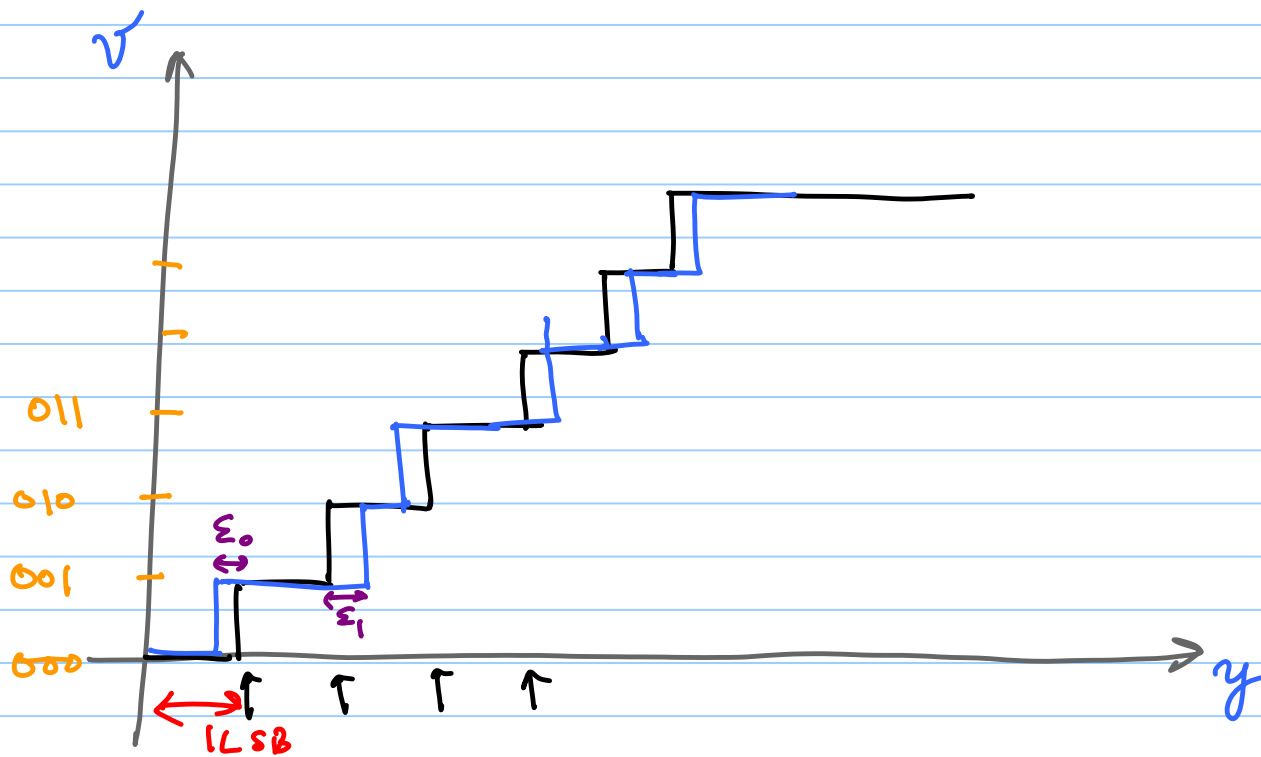


# ECE 517 - Lecture 11

Note Title

2/21/2017

HW 2 is posted



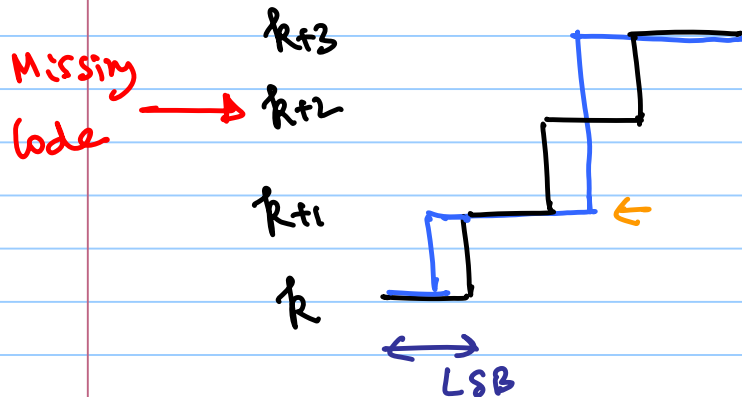
Static characteristics

DNL  $\rightarrow$  INL

$$DNL(k) \triangleq \frac{\text{Width of code 'k'} - 1 \text{ LSB}}{1 \text{ LSB}}$$

← k<sup>th</sup> code

→ specifying the DNL defines the entire static characteristics



$$DNL(k) = -0.3$$

$$DNL(k+1) = +0.6$$

$$DNL(k+2) = -1 ? \leftarrow \text{Missing code}$$

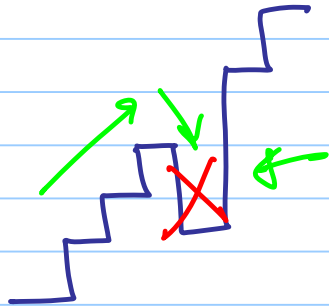
$$DNL(k+3) = +0.7$$

$|DNL| \leq 0.5 \text{ LSB}$ , is sufficient to ensure no missing codes  
↳ sufficient by necessary

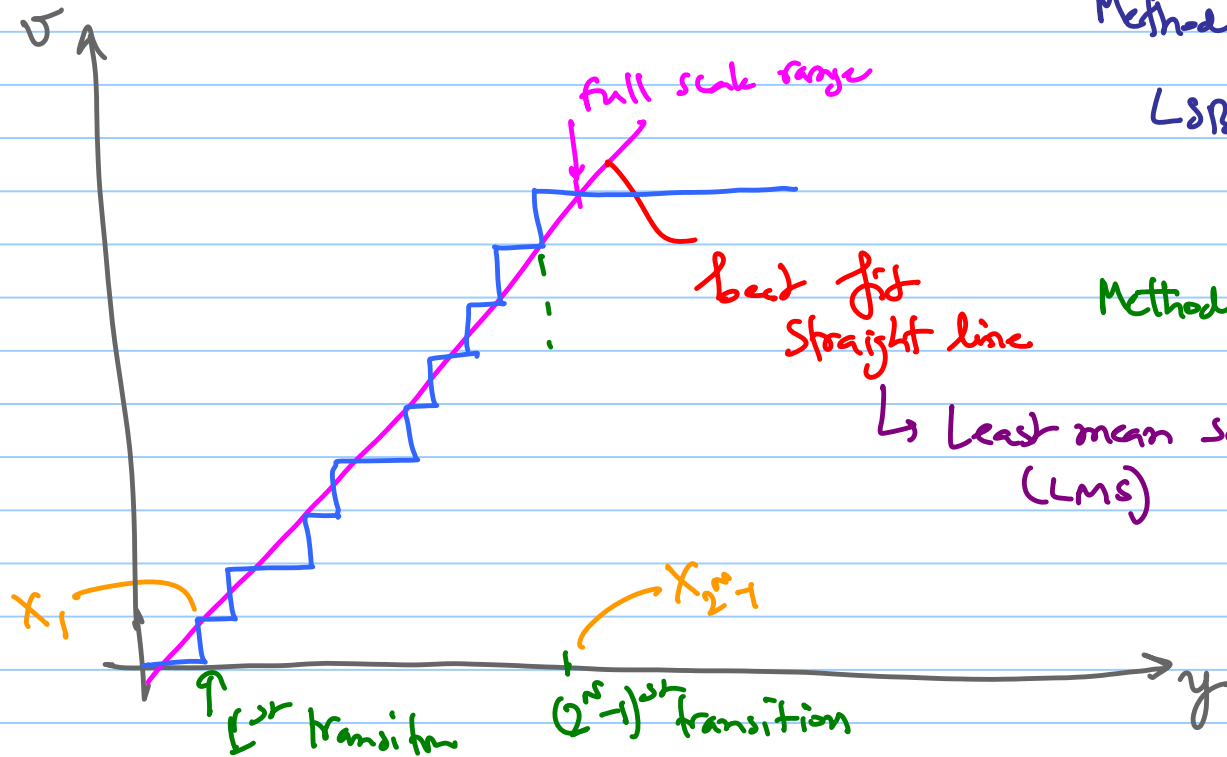
\* However, there can be situations where  $DNL_k > 1 \text{ LSB}$ , yet no missing codes.

Need to ensure  $|DNL(k)| \leq 0.5 \text{ LSB}$

Quantizer characteristics must be monotonic



+ How do we define LSB



\* Numerically fit a straight line (LMS)

↳ Remove the offset & gain error from the staircase

↳ best fit straight line

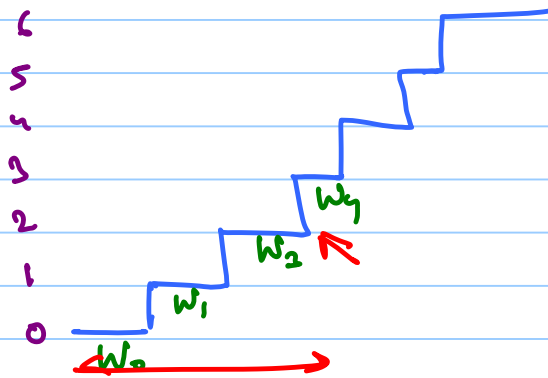
↳ from the slope, compute ideal LSB

↳ Compute DNL (k)

\* INL (Integral Non Linearity) ← another common metric

INL ( $k$ ) = deviation in LSB of the code transition w.r.t to the ideal transition.

↳ don't care about the individual code widths, but the cumulative effect on the code transition



Ideal transition for the  $k^{\text{th}}$  code  $\Rightarrow k \cdot \text{LSB}$   
Real transition =  $\sum_{i=0}^{k-1} w_i$

$$INL(k) = \frac{\sum_{i=0}^{R-1} w_i - k \cdot LSB}{1 \text{ LSB}}$$

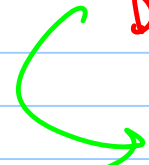
$$(-) \quad INL(k) = \sum_{i=0}^{R-1} w_i - k$$

$$\underline{\underline{LSB \triangleq 1}}$$

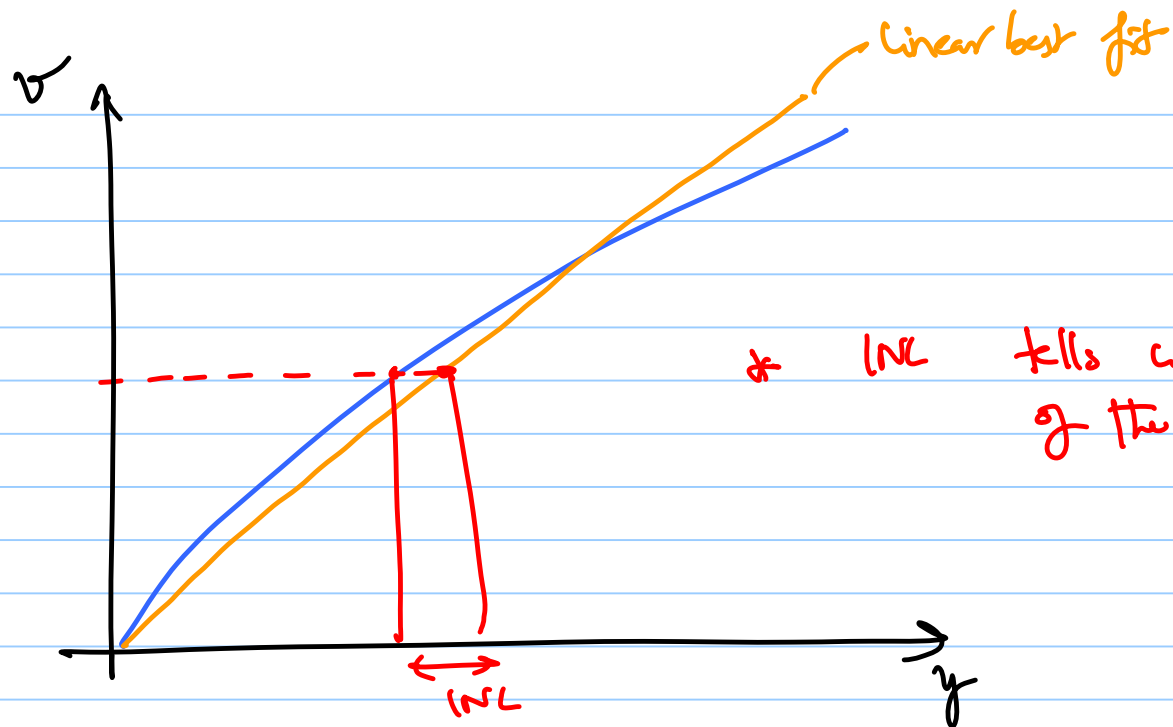
$$(+) \quad INL(k+1) = \sum_{i=0}^R w_i - k+1$$

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$$INL(k+1) - INL(k) = \underbrace{w_{R-1}}_{DNL(k)}$$

$$DNL(k) = INL(k+1) - INL(k)$$

$$INL(k) = \sum_{i=0}^{k-1} DNL(i)$$

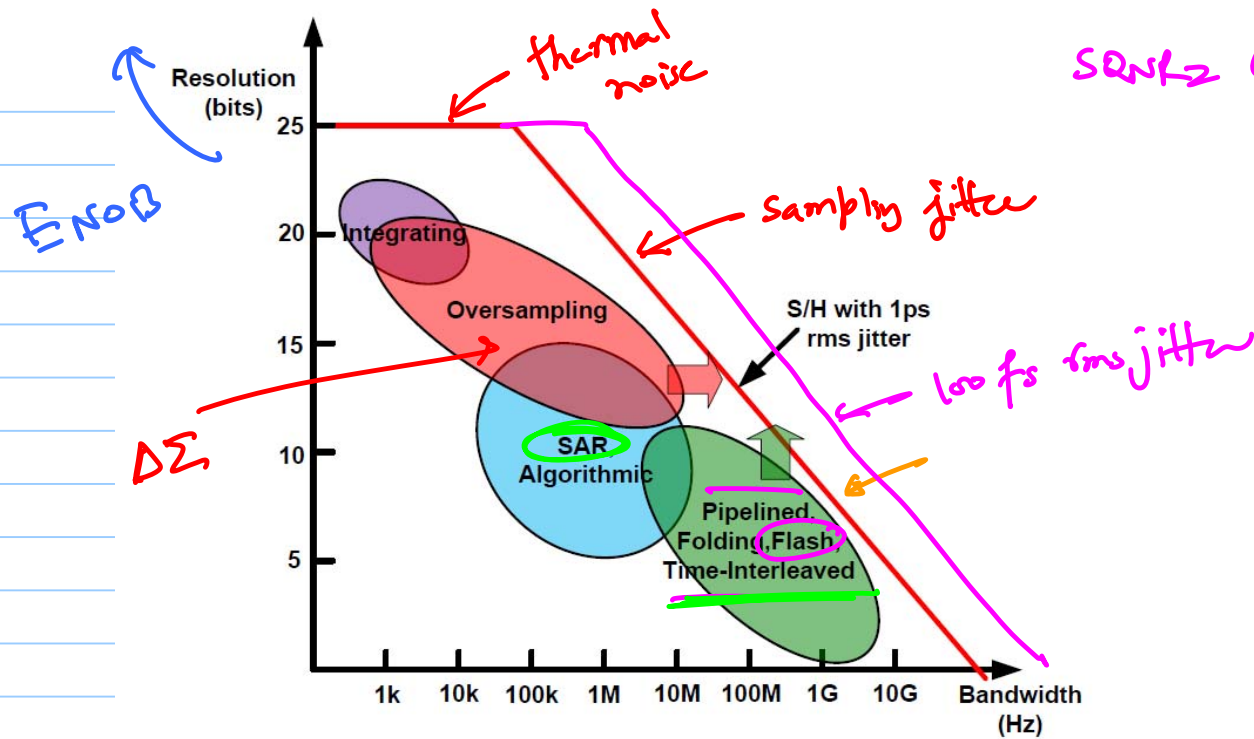
\* INL is the running sum of the DNL



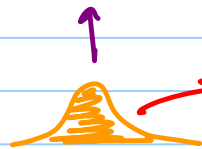
\*  $INL$  tells us the overall trend of the ADC

Communication  $\Rightarrow$   $INL$  needs to be small

Video  $\Rightarrow$   $DNL$  needs to be small



Conversion BW



jitter  $\longleftrightarrow$  phase noise

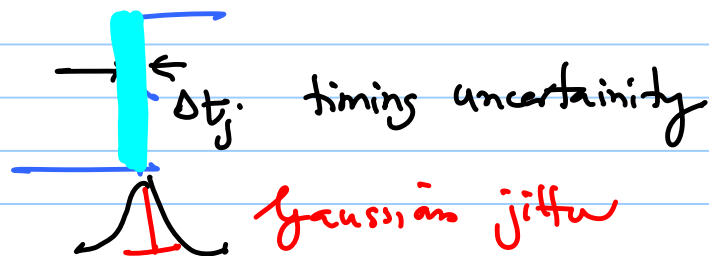
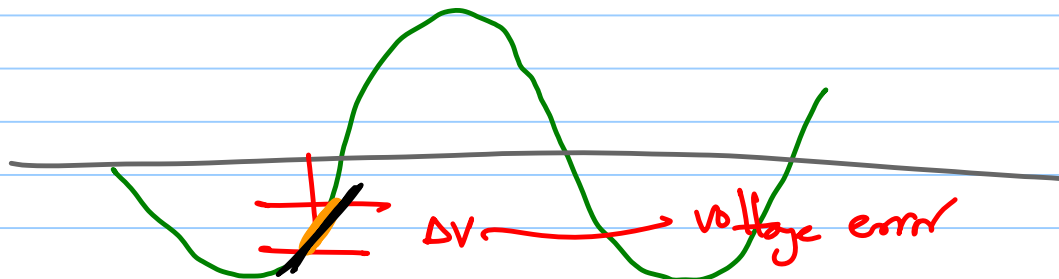
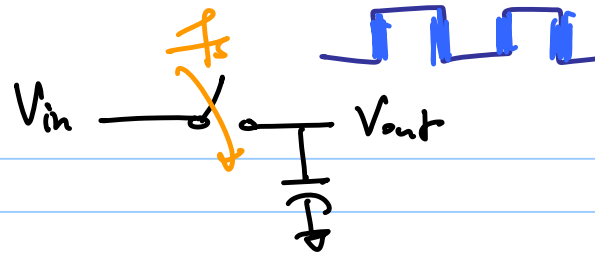
$\hookrightarrow$  oscillator

$\hookrightarrow$  PLL

$\sigma_j \Rightarrow$  rms value of the clock source jitter

$$\sigma_j = 100 \frac{1}{f} \text{ rms}$$

Sampling jitter



$$V_{in} = A \sin(2\pi f_{in} t)$$

Voltage error,  $\Delta V = \left( \frac{dV_{in}}{dt} \right)_{t=nT_s} \cdot \Delta t_j$

↓ random variable

↓ slope

$$V_{in} = A \sin(2\pi f_{in} t)$$

$$\frac{dV_{in}}{dt} = 2\pi f_{in} A \cos(2\pi f_{in} t)$$

$$E\left(\left(\frac{dV_{in}}{dt}\right)^2\right) = (2\pi f_{in} A)^2 \cdot \frac{1}{2}$$

$$\hat{\sigma}_{\Delta V}^2 = E[\Delta V^2] = E\left[\left(\frac{dV_{in}}{dt}\right)^2 \cdot \Delta t_j^2\right]$$

$$= E\left[\left(\frac{dV_{in}}{dt}\right)^2\right] \cdot E[\Delta t_j^2]$$

$$= \frac{1}{2} \cdot (2\pi f_{in} A)^2 \cdot \sigma_j^2$$

$$\sigma_{\Delta v}^2 = \frac{1}{2} (2\pi f_{in} A)^2 \cdot \sigma_j^2$$

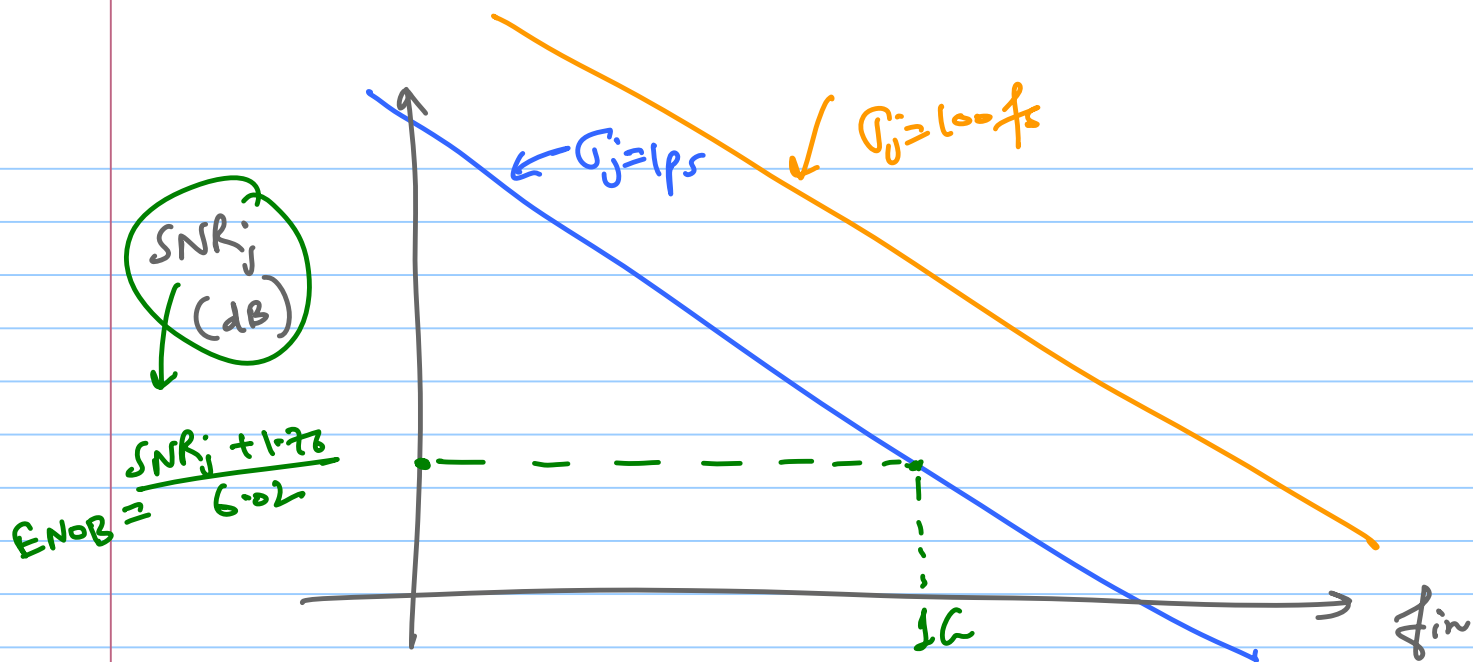
noise due to  
sampling jitter

jitter limited SNR

$$SNR_j = 10 \log_{10} \left( \frac{P_s}{P_n} \right) = 10 \log_{10} \left( \frac{\cancel{A^2/2}}{(2\pi f_{in} \cancel{A})^2 \cdot \cancel{1/2} \cdot \sigma_j^2} \right)$$

$$= 20 \log_{10} \left[ \frac{1}{2\pi f_{in} \sigma_j} \right]$$

$$\boxed{SNR_j = -20 \log_{10} (2\pi f_{in} \sigma_j)}$$



# Flash ADC

Nbit  $\Rightarrow 2^N - 1$  Comparators

