Sampling Switches:

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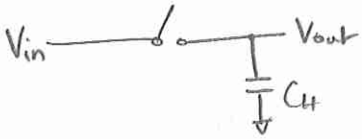
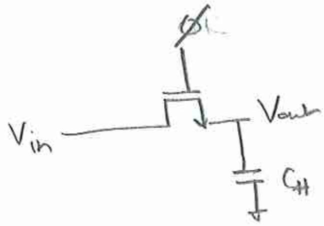




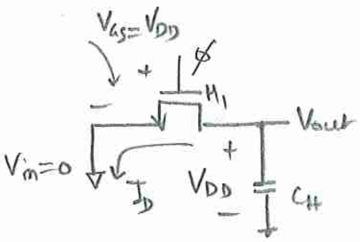
⇒ sampling switch → MOS transistor

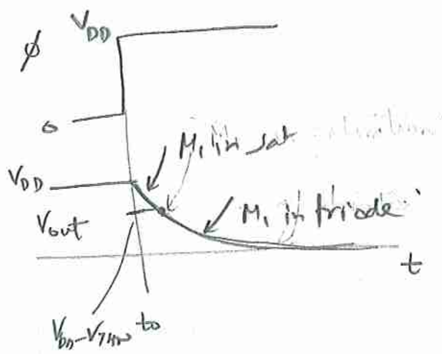
a) it can be ON while carrying zero current

b) its source and drain voltages are not 'pinned' to the gate voltage ⇒ if V_G varies, source or drain voltage need not follow the variation

↳ BJT's lack both these properties

(a)



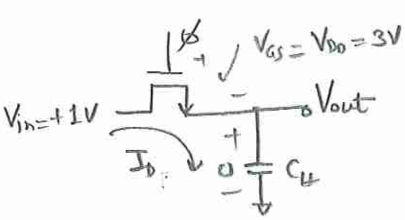


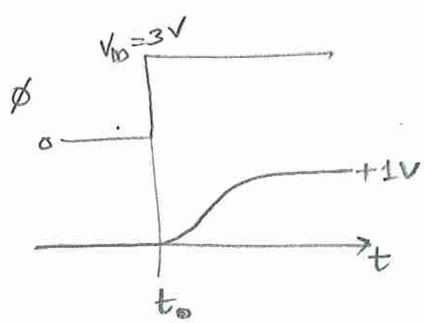
$V_{out}=V_{DD}$, $V_{DS}=V_{DD}$ ⇒ $I_D(t_0)=\dfrac{\mu_n C_{ox} W}{2L}(V_{DD}-V_{THN})^2$

$V_{out} < V_{DD}-V_{THN}$ ← M_1 enters triode

for $V_{out} \ll (V_{DD}-V_{THN})$ ← deep triode ⇒ $\boxed{R_{on}=\dfrac{1}{\mu_n C_{ox}\frac{W}{L}(V_{DD}-V_{THN})}}$

(b)





M_1 operates in triode charging C_H till V_{out} reaches $V_{in}=+1V$

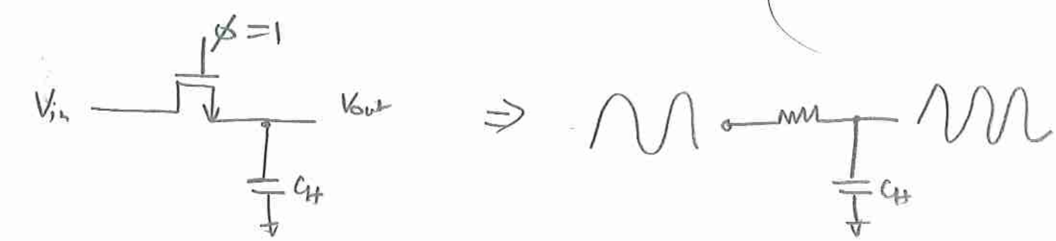
$$\Rightarrow R_{on}=\frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{DD}-V_{in}-V_{THN})}$$

Observations :

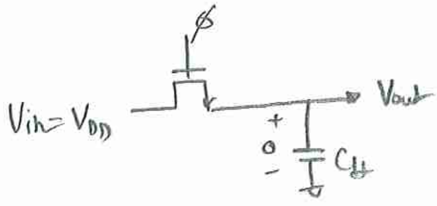
* MOS can conduct current in either direction by exchanging the role of its source and drain

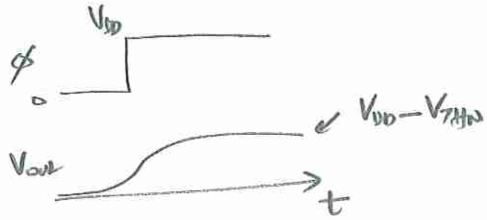
* When switch is "On", output V_{out} follows the input V_{in} when the switch is "off", V_{out} remains constant.

$\Rightarrow$ The circuit "tracks" the signal when $\phi =$ is high and "freezes" the instantaneous value of V_{in} across C_H when ϕ goes low.



Track and hold capability of a sampling circuit.

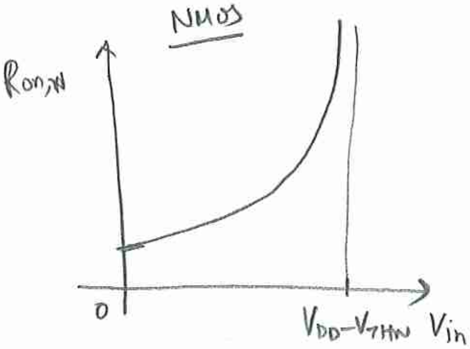


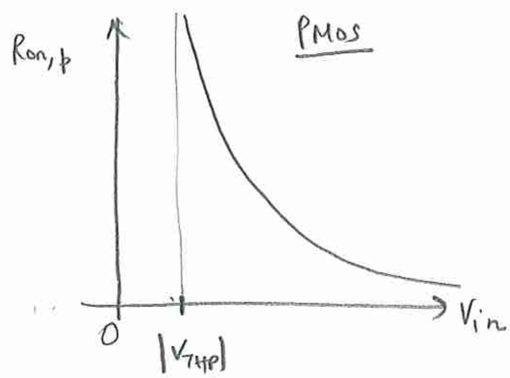


* Eventually subthreshold current will flow and V_{out} will reach V_{DD}.
* for typical operation speeds, reasonable to assume that V_{out} doesn't exceed $V_{DD} - V_{THN}$.

⇒ V_{out} can't track inputs close to V_{DD}

↳ R_{on} increases considerably as V_{in} reaches closer to $(V_{DD} - V_{THN})$

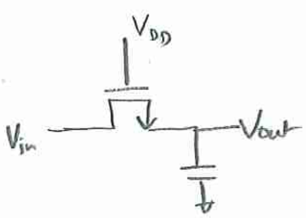




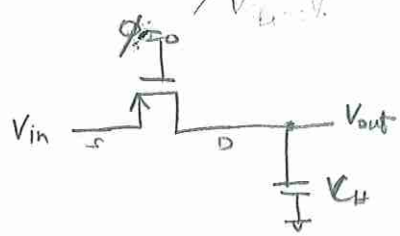
$$R_{on,N} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{THN})}$$

$$R_{on,p} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{in} - |V_{THP}|)}$$

V_{SG}



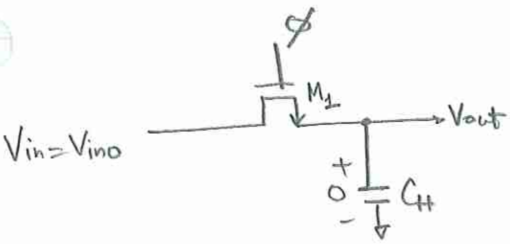
$V_{GS} = V_{DD} - V_{out}$
$= V_{DD} - V_{in}$

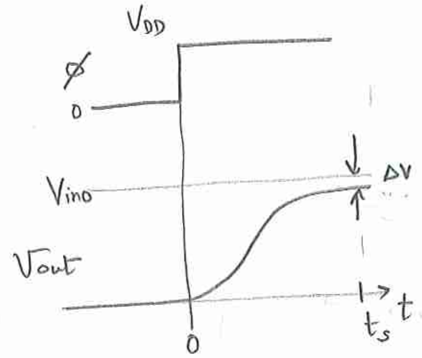


$V_{SG} = V_{in}$

* Similarly, for PMOS switches, the on resistance rises rapidly as input & output drop closer to $|V_{THP}|$.

Speed Considerations





How to define switch speed?

time taken to settle within an "error band" ΔV, say $\frac{\Delta V}{V_{in0}} = 0.1\%$

$\Rightarrow$ speed spec must be accompanied by an accuracy spec as well.

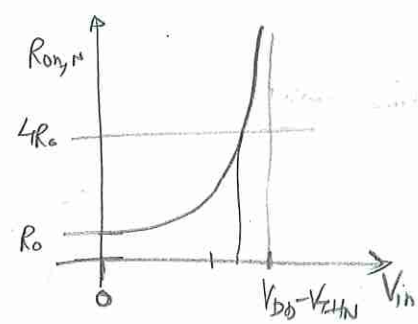
$\Rightarrow$ at $t = t_s$ we can consider drain & source voltages to be equal

$\Rightarrow$ switching speed $\rightarrow$ R_{on} & C_H

$R_{on} \downarrow$ large $\frac{W}{L}$

$C_H \downarrow$ small sampling cap

But R_{on} depends upon input signal level



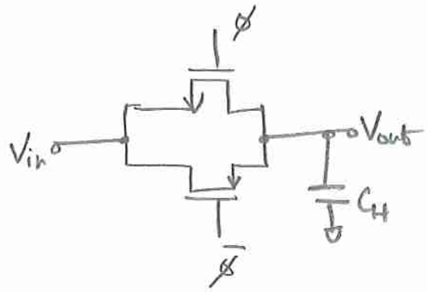
If we restrict R_{on} to a range of 4 to 1, then the maximum input range

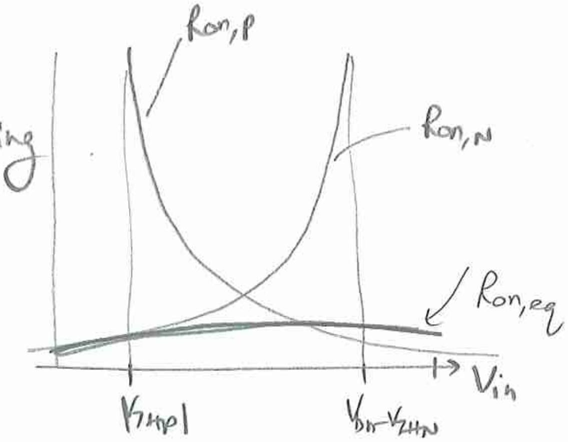
$$\underbrace{\frac{1}{\mu_n C_{ox}\frac{W}{L}\left(V_{DD}-V_{in,max}-V_{THN}\right)}}_{R_{on}(V_{in,max})} = \underbrace{\frac{4}{\mu_n C_{ox}\frac{W}{L}\left(V_{DD}-V_{THN}\right)}}_{R_{on}(V_{in}=0)}$$

$4R_o$

$$\Rightarrow \boxed{V_{in,max} = \frac{3}{4}\left(V_{DD}-V_{THN}\right)} \simeq \frac{V_{DD}}{2} \quad \text{severe sizing limitation}$$

Larger voltage swing





Complementary switch

$$R_{on,eq} = R_{on,N} \| R_{on,P}$$

$$= \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{DD} - V_{in} - V_{THN})} \Bigg\| \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_P (V_{in} - |V_{THP}|)}$$

$$= \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{DD} - V_{THN}) - \left[\mu_n C_{ox} \left(\frac{W}{L}\right)_N - \mu_p C_{ox} \left(\frac{W}{L}\right)_P\right] V_{in} - \mu_p C_{ox} \left(\frac{W}{L}\right)_P |V_{THP}|}$$

mostly indep of input-level except that $V_{THN,P}$ vary with V_{in} through body-effect.

Time-constants

$$\tau = R_{on,eq} \cdot C_H$$

$$\frac{V_{out}}{V_{in_0}} = \left(1 - e^{-t_s/\tau}\right)$$

$\Rightarrow$ for $V_{out} = (1-\epsilon) V_{in_0}$ accuracy

$$\Rightarrow 1-\epsilon = 1 - e^{-t_s/\tau}$$

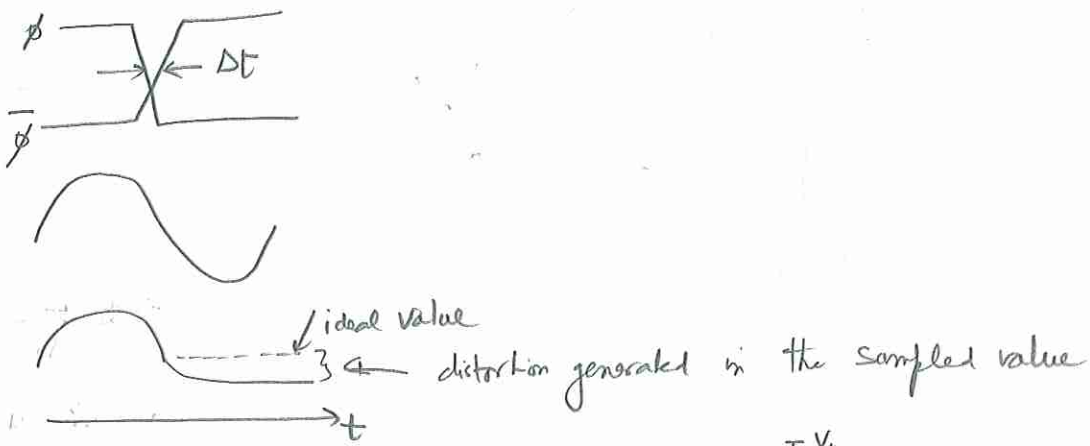
$$\Rightarrow e^{-t_s/\tau} = \epsilon$$

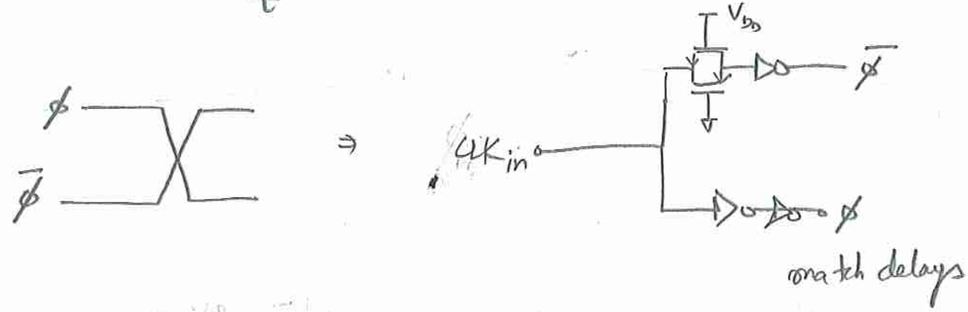
$$\Rightarrow \frac{t_s}{\tau} = \ln\left(\frac{1}{\epsilon}\right)$$

$$\Rightarrow \boxed{t_s = \tau \ln\left(\frac{1}{\epsilon}\right)}$$

	ϵ	t_s/τ
10%	0.1	2.3
1%	0.01	4.6
0.1%	0.001	6.9
0.01%	0.0001	9.21

* for high-speed input signals, NMOS & PMOS switches should turn-off simultaneously to avoid ambiguity in the sampled value





Precision Considerations

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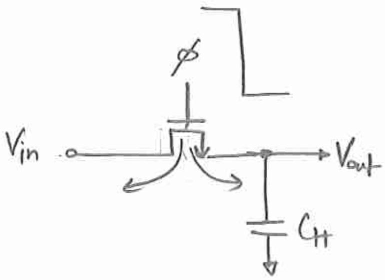
Precision Considerations

① channel "charge injection"
② clock feedthrough
③ kT/C Noise



Assuming $V_{in} \simeq V_{out}$:

$$Q_{ch} \simeq WLC_{ox}(V_{DD} - V_{in} - V_{THN})$$

$$V_{THN} = V_{THN0} + \gamma\left(\sqrt{2\phi_B + V_{in}} - \sqrt{2\phi_B}\right)$$

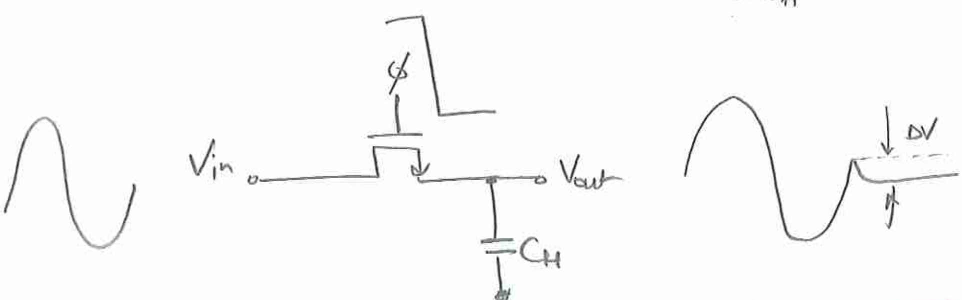
* when the switch turns off, Q_{ch} exits through the source & drain terminals → "channel charge injection"

* Charge on the left side is absorbed into the input source (V_{in}) and no error is created

* Charge on the right side is deposited on C_H → introducing an error in the voltage stored in the capacitor.

→ If $-\frac{Q_{ch}}{2}$ is injected into C_H

$$\Delta V = \frac{-WLC_{ox}(V_{DD} - V_{in} - V_{THN})}{2C_H} \quad \text{(negative)}$$



pedestal error

Note that $\cancel{\Delta V} \propto WL$

~~[illegible]~~

$\propto \frac{1}{C_H}$

* Assumption of half channel charge injected into C_H
  - in reality a function of impedances seen at drain & source and the transition time of the clock
  - no exact expression available
  - as a worst estimate assume all of the Q_{ch} is injected

Q. How does charge injection affect the precision

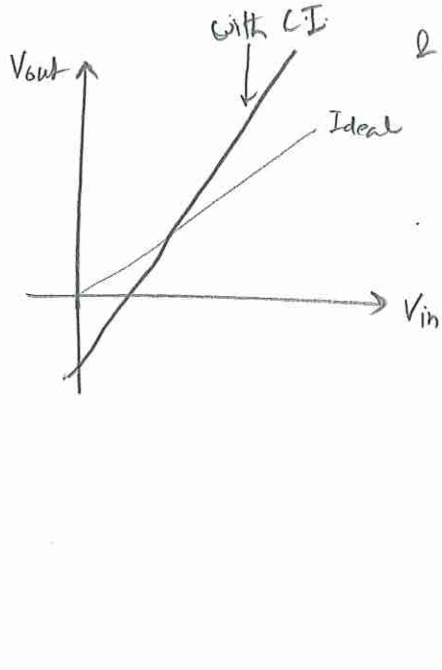
$$V_{out} \simeq V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{THN})}{C_H}$$

∘ neglecting the phase shift between V_{in} & V_{out}

$$\Rightarrow V_{out} = \underbrace{V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right)}_{\text{gain}} \underbrace{- \frac{WLC_{ox}}{C_H}(V_{DD} - V_{THN})}_{\text{offset}}$$

non unity gain $\Rightarrow$ $1 + \frac{WLC_{ox}}{C_H}$ ← gain error

& constant offset voltage $\Rightarrow$ $\underbrace{-\frac{WLC_{ox}}{C_H}(V_{DD} - V_{THN})}_{\text{offset}}$



So far we assumed V_{THN} is constant

but $V_{THN} = V_{THN0} + \gamma\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right)$

& $V_{SB} \simeq V_{in}$

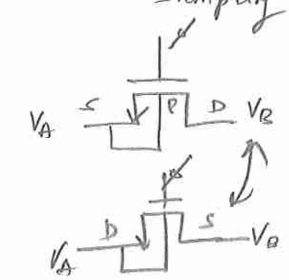
⇒

$$V_{out} = V_{in} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{in} - V_{THN0} - \gamma\sqrt{2\phi_B + V_{in}} + \gamma\sqrt{2\phi_B}\right)$$

$$= V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) + \underbrace{\gamma\frac{WLC_{ox}}{C_H}\sqrt{2\phi_B + V_{in}}} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{THN0} + \gamma\sqrt{2\phi_B}\right)$$

* Non-linearity in the input-output characteristics
*

For body connected PMOS, S & D terminals may interchange during sampling



⇒ Charge injection contributes errors in S/C circuits
↳ gain error
↳ DC offsets
) can be tolerated
↳ non linearity) cannot be tolerated

* Speed-precision trade-off

FoM $\Rightarrow$ $F = (\tau \Delta V)^{-1}$ large value desired

$$\tau = R_{on} C_H$$

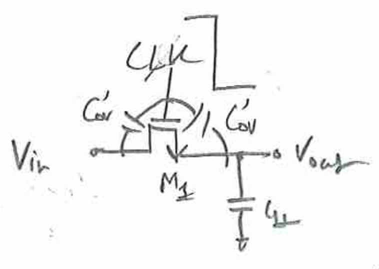
$$= \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{THN})} C_H$$

$$\Rightarrow \Delta V = \frac{W L C_{ox}}{C_H} (V_{DD} - V_{in} - V_{THN})$$

$$F = \frac{1}{\tau \Delta V} = \frac{\mu_n}{L^2}$$

$\leftarrow$ to the first order, the tradeoff is indep of switch width & Sampling Cap

Clock feedthrough



$$\Delta V = V_{CLK} \cdot \frac{W C'_{ov}}{W C'_{ov} + C_H}$$

overlap Cap

$C'_{ov} \leftarrow$ overlap Cap p.u. width $\frac{C}{W}$

$\Delta V \leftarrow$ indep of input level

$\hookrightarrow$ Constant offset in the sampled output

Large $W \Rightarrow \Delta V \uparrow$

$\Rightarrow$ for precision $C_H \gg \underbrace{W C'_{ov}}_{\text{overlap Cap}}$

Thermal Noise in a Switched Capacitor

+ $\frac{kT}{C}$ Noise

$$\bar{V}_n = \sqrt{\frac{kT}{C_H}}$$

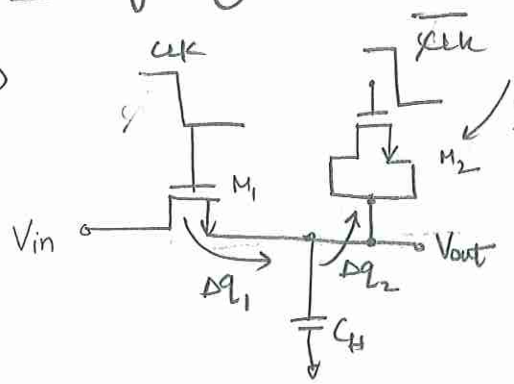
⇒ C_H must be sufficiently large for precision

$$SNR = 20 \log\left(\frac{V_{in,rms}}{\bar{V}_n}\right) = 6N +$$

⇒ large C ⇒ more loading on circuits
lower speed or more power.

Charge Injection Cancellation:

1



* driven by $\overline{CLK}$ to cancel the charge.

* When M_1 turns off and M_2 turns on, the channel charge is deposited on C_H is absorbed by M_2 to create a channel

perfect cancellation for

$\Delta q_1 = \Delta q_2$

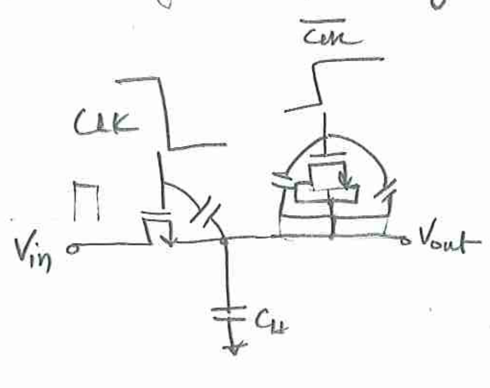
$$\frac{W_1 L_1 C_{ox}}{2}\left(V_{CLK} - V_{in} - V_{THN_1}\right) = W_2 L_2 C_{ox}\left(V_{CLK} - V_{in} - V_{THN_2}\right)$$

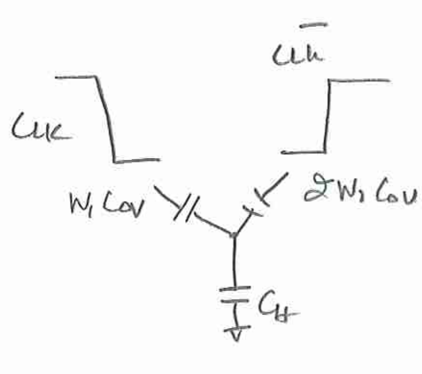
for $W_2 = \frac{W_1}{2}$ & $L_2 = L_1$, it may work

* But the assumption of equal charge splitting b/w D&S is invalid

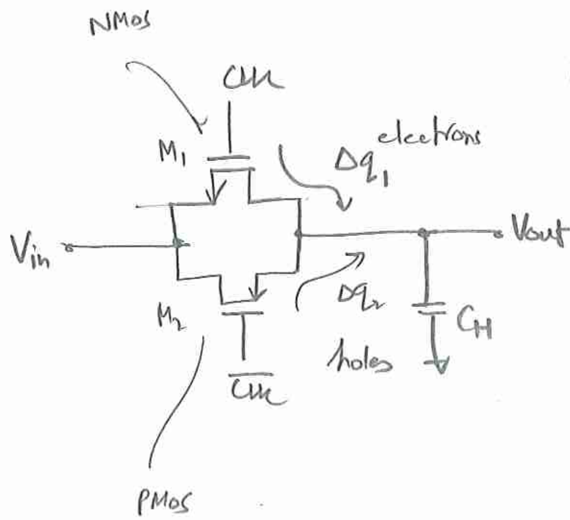
↳ makes this approach less robust

<u>However</u> ⇒ ~~cl~~ clock-feedthrough is cancelled using this scheme





② Complementary switches



NMOS & PMOS inject opposite charge packets

→ for $\Delta q_1 = \Delta q_2$

We must have

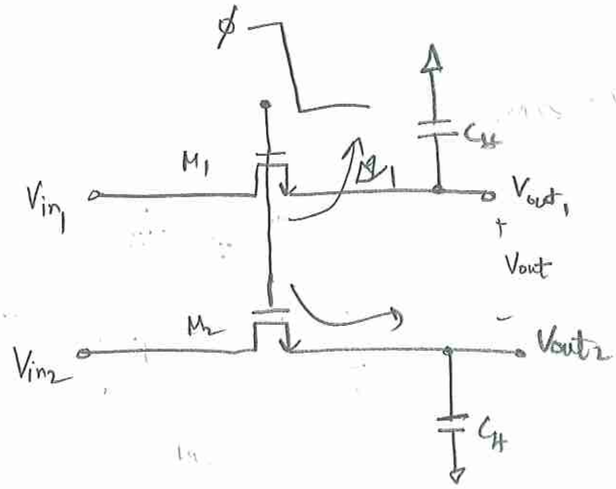
→ $$W_1 L_1 C_{ox}(V_{clk} - V_{in} - V_{THN}) = W_2 L_2 C_{ox}(V_{in} - |V_{THP}|)$$

→ cancellation only occurs for one input value not for all V_{in} values

* Also this circuit doesn't provide clock-feedthrough cancellation

$\because C_{ov_{PMOS}} \neq C_{ov_{NMOS}}$

3 Differential circuits



Does charge injection appear as CM disturbance?

Differential error "charge"

$$\Delta q_1 - \Delta q_2 = WLC_{ox}\left[(V_{in_2} - V_{in_1}) + (V_{THN_2} - V_{THN_1})\right]$$

$$= WLC_{ox}\left[\underbrace{(V_{in_2} - V_{in_1})}_{0} + \gamma\left(\underbrace{\sqrt{2\phi_B + V_{in_2}} - \sqrt{2\phi_B + V_{in_1}}}_{\text{odd function}}\right)\right]$$

* No DC offset due to charge injection
* non-linearity of body effect now appears in both Square root terms
  - → odd-order distortion
    - → even order terms in Taylor series Cancel off

4 Bottom-plate Sampling → later

Odd function

$\boxed{f(x) - f(-x)}$ ↑ has only odd-order Taylor series terms

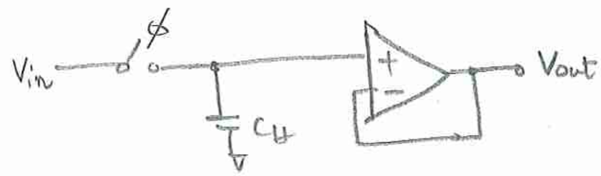
$V_{in_1} = x$
$V_{in_2} = -x$

Unity-gain Sampler/Buffer:

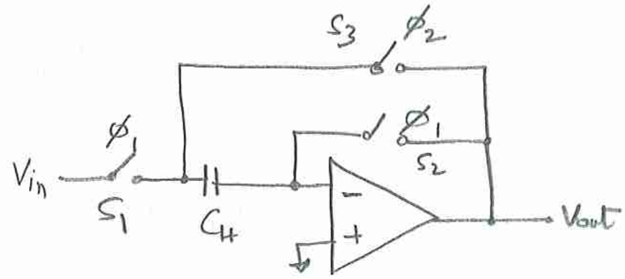
Unity-gain Sample-and-Hold/Buffer Circuit

①

Sample and buffer (hold)



Here, Input dependent charge injection limits the accuracy. Will not work.

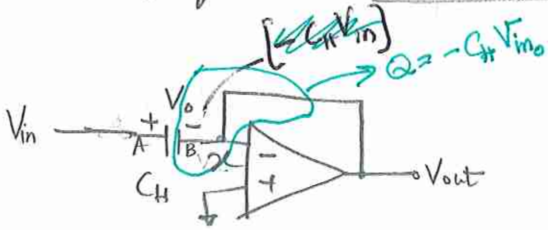


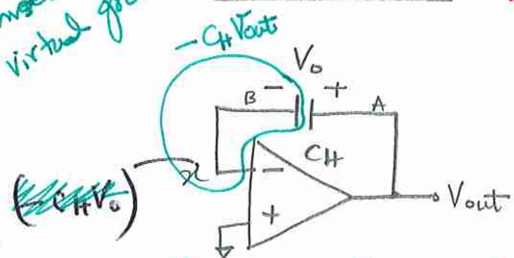
* initially neglect charge injection

Sampling mode $\phi_1 = 1, \phi_2 = 0$ ϕ_1

Charge conservation at the virtual ground

$\phi_2 = 1, \phi_1 = 0$ ϕ_2





$V_{out} = V_x \simeq 0$

Voltage across C_H tracks V_{in}

@ $t = t_0$, $V_{in} = V_0$ is stored on C_H

$-\cancel{C_H} V_{out} = -\cancel{C_H} V_{in_0} \Rightarrow V_{out} = V_{in_0}$

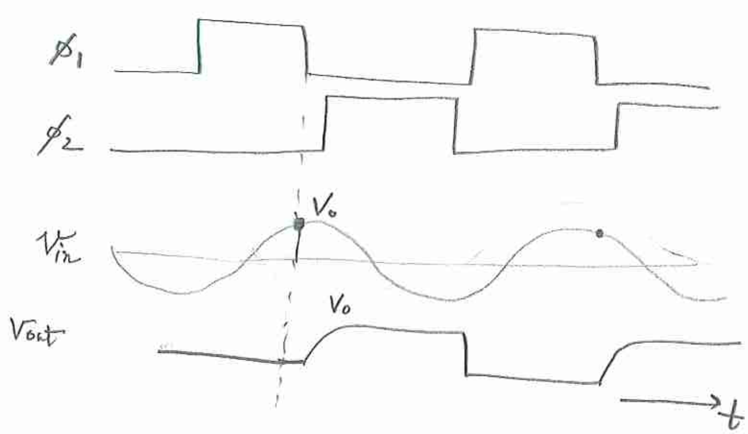
$V_x = 0$ virtual ground for the signals

Charge conservation holds at V_x.

$\Rightarrow$

V_{out} rises to $\simeq V_0$

This value is "frozen" and processed by subsequent stages

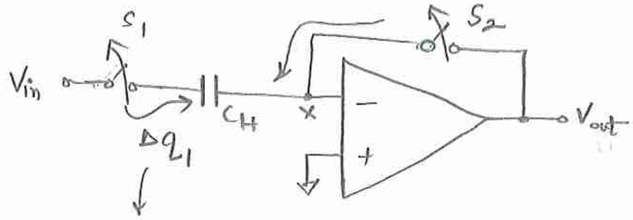


Slow motion recap of the S/H circuit

$$\Delta q_2 = WLC_{ox}(V_{clk} - V_x - V_{THN_2}) \simeq WLC_{ox}(V_{CLK} - V_{THN_2})$$

$\because V_x \simeq 0$ $\quad V_{THN_2} = f(\sqrt{V_x})$

$\Rightarrow \Delta q_2$ is constant every cycle



$$\Delta q_1 = WLC_{ox}(V_{CLK} - V_{in} - V_{THN_1})$$

$\Rightarrow$ when S_1 turns off $\Rightarrow$ charge $\Delta q_1 = WLC_{ox}(V_{CLK} - V_{in} - V_{THN_1})$ is injected into C_H $\quad f(\sqrt{V_{in}})$

* when S_2 turns off $\Rightarrow$ charge $\Delta q_2 = WLC_{ox}(V_{clk} - V_{THN_2})$ is injected into C_H

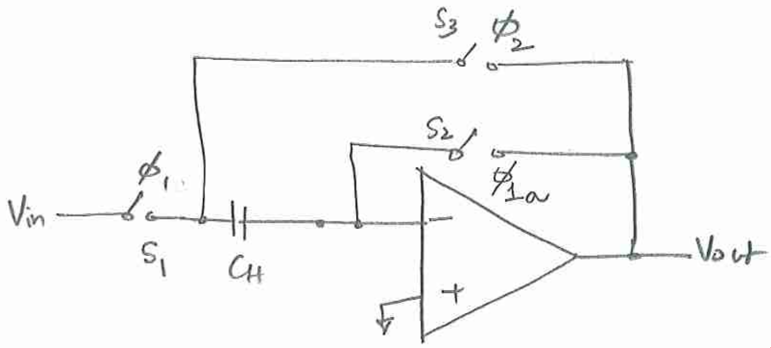
↳ constant charge as V_x is relatively independent of V_{in}

↳ important!

* Constant magnitude of Δq_2 only introduces offset in the input/output characteristics

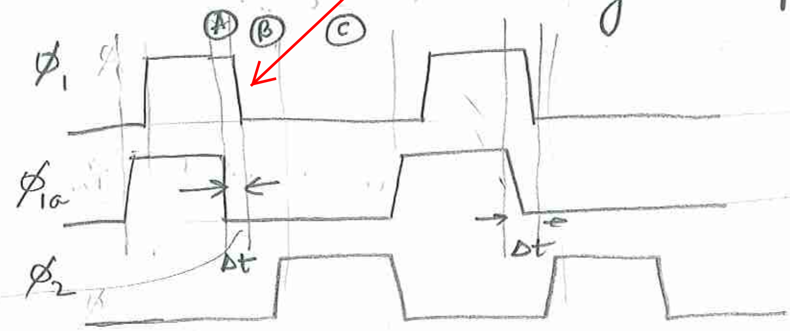
↳ Can be removed by differential operation

Trick: Delayed sampling clock



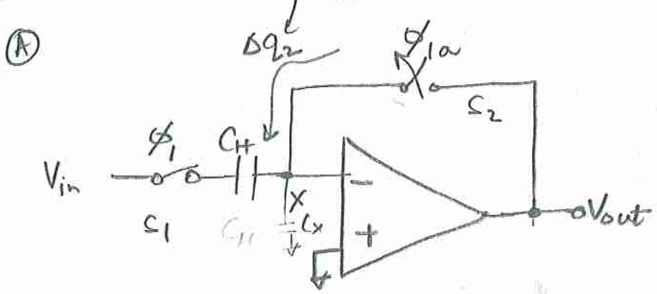
Circuit Trick for avoiding input dependent charge injection

* Turn-off "open" switch S_2 earlier than S_1 ⇒ early clock phase ϕ_{1a}



ϕ_{1a} falls earlier than ϕ_1

constant error

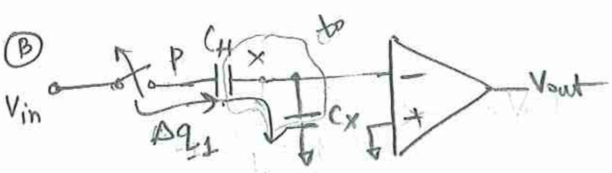


$\phi_1 = 1$

$\phi_{1a} = 0$

* Let $V_{in} = 0$

* Δq_1 is injected from S_1 into C_H



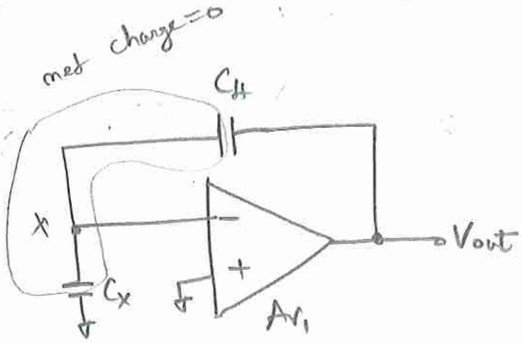
Observation:

After S_2 is off ⇒ i.e $\phi_{1a} = 0$

⇒ Total charge at node-X can not change as no path exists for electrons to flow into or out of this node.

⇒ before S_1 turns off, total charge on the right plate of C_H & top plate of $C_x = 0$

(c)



Total charge at node x = 0

$$\Rightarrow \quad C_x V_x - (V_{out} - V_x)\cdot C_H = 0 \longrightarrow (1)$$

$$\& \quad V_x = -\frac{V_{out}}{A_{v_1}} \longrightarrow (2)$$

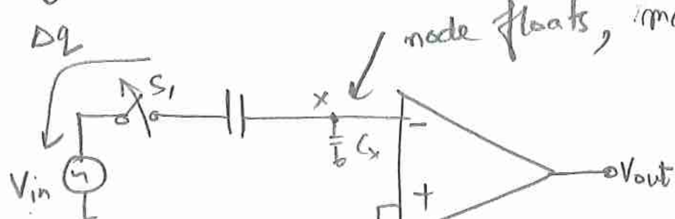
$$\Rightarrow \quad -(C_x + C_H)\cdot\frac{V_{out}}{A_{v_1}} - V_{out}\, C_H = 0$$

$$\Rightarrow \quad V_{out} = 0$$

↳ this result is independent of Δq_1, Cap values or A_v (opamp gain)

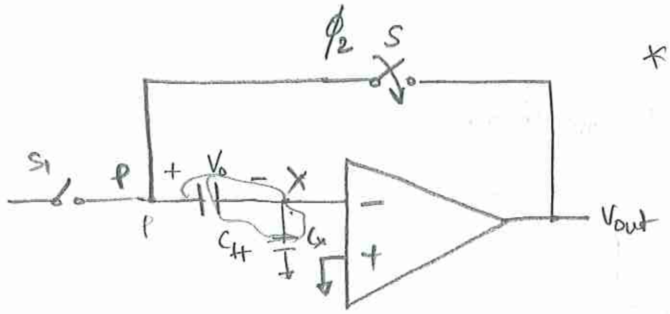
⇒ charge injection by S_1 introduces no error if S_2 "turns off first".

Summary:



node floats, maintaining a constant total charge irrespective of charge injected by S_1.

⇒ all the injected charge is sucked into the source



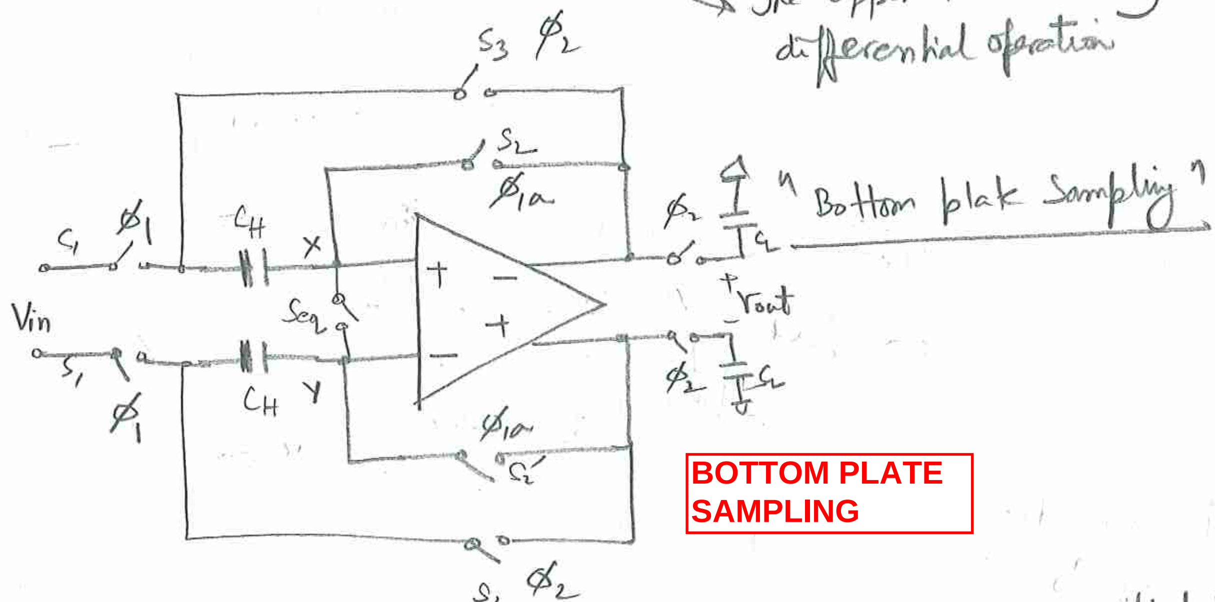
* When S_3 is turned on, is the inversion layer charge supplied by C_H or the opamp?

The previous analysis can be used again to show that after the circuit has settled charge on $C_H = V_0 C_H$

⇒ the inversion layer charge is provided by the opamp.

⇒ charge injected by S_1 & S_3 are unimportant
& S_2 charge injection results in a constant offset voltage.

→ The offset is eliminated by differential operation



⇒ non-linearity due to input-dependent charge injection is mitigated

⇒ charge injected at X & Y is a CM disturbance

* In reality, S_2 & S_2' exhibit finite charge injection mismatch

↳ add another switch S_{eq}

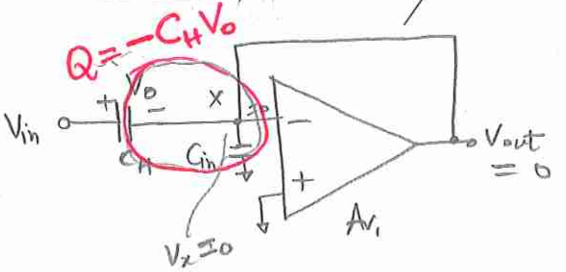
↳ turns off slightly after S_2 and S_2' but before S_1 & S_1'

↳ equalizes charge at node X & Y.

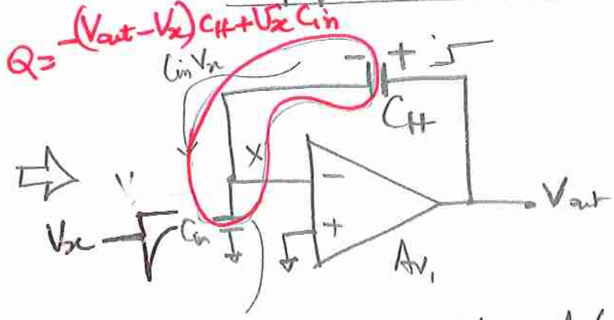
Precision Consideration:

Sampling mode

$V_x = A(0 - V_x) \Rightarrow V_x = 0$



(Hold) Amplification Mode



$C_{in} \Rightarrow$ input parasitic capacitance

$Q =$

$V_{out} = A_v(0 - V_x)$

$\Rightarrow V_x = -\dfrac{V_{out}}{A_v}$

In amplification mode

$V_x \neq 0$ due to finite opamp gain, A_v.

* Conservation of charge at X requires that it should come from C_H

$\Rightarrow$ charge on C_H is raised to $C_H V_o + C_{in} V_x$

* positive charge transfer from the left plate of C_H to the top plate of C_{in} leads to a more positive voltage across C_H.

$$Q_x = -C_H V_o = -(V_{out} - V_x)C_H + V_x C_{in}$$

$$\Rightarrow \quad \Rightarrow \quad V_{out} = \frac{V_x(C_{in} + C_H) + V_o C_H}{C_H}$$

$$\Rightarrow V_{out} = V_o + V_x\left(1 + \frac{C_{in}}{C_H}\right) \longrightarrow (1)$$

$$V_x = -\frac{V_{out}}{Av_1} \qquad (2)$$

(1) & (2) give:

$$V_{out} = \frac{V_o}{1 + \frac{1}{Av_1}\left(\frac{C_{in}}{C_H} + 1\right)}$$

$$\boxed{\simeq V_o\left[1 - \frac{1}{Av_1}\left(\frac{C_{in}}{C_H} + 1\right)\right]}$$

$\Rightarrow$ If $C_{in} \ll C_H$

$V_{out} \simeq \dfrac{V_o}{1 + A_v^{-1}}$ as expected

$$\frac{1}{\beta} = \frac{C_{in} + C_H}{C_H}$$

$$\Rightarrow \boxed{\beta = \frac{C_H}{C_H + C_{in}}} \text{ feedback factor}$$

* Circuit suffers from gain error of $-\frac{\left(\frac{C_{in}}{C_H}+1\right)}{A_{V_1}}$

$\Rightarrow$ input cap must be minimized if speed is not critical

We could increase the width of the input diff pair for the same current

i.e. $W \uparrow$ with I_D = const

$\Rightarrow V_{ov} \downarrow \Rightarrow g_m r_o \uparrow$ & $f_T \downarrow$

Ex. $C_{in} = 0.5pF$

$C_H = 2pF$

A_V for gain error $= 0.1\% = 10^{-3} = 60$ dB precision

$\searrow A_V \geq 1250 \Rightarrow > 60$ dB DC gain

---

* Opamp DC gain should be large enough to reduce S/H or amplifier's output error to $\frac{1}{2}$ LSB $\Rightarrow \frac{V_{ref}}{2^{N+1}}$

Also amplifier's $f_{3dB} = \beta f_{un}$ should be large enough for the amplifier's settling error to be $< \frac{V_{ref}}{2^{N+1}}$

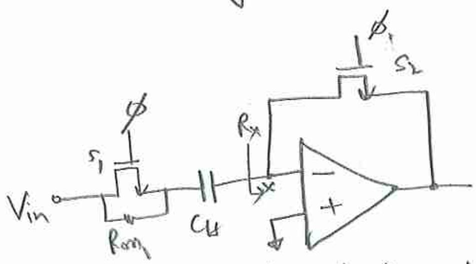
Thermal noise should be well below 1 LSB

$\hookrightarrow$ Opamp's input referred noise should be small enough.

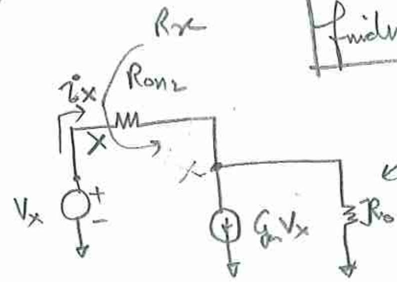
Speed Consideration for S/H

Speed Consideration

Lets first examine in sampling mode



Finding R_x



What is the time-constant?

Total resistance in series with $C_H \Rightarrow R_{on_1} + R_x$ ← resistance between X and ground

$$(I_x - g_m V_x) R_o + I_x R_{on_2} = V_x$$

$$\Rightarrow \quad R_x = \frac{R_o + R_{on_2}}{1 + g_m R_o}$$

Since typically, $R_{on_2} \ll R_o$ and $g_m R_o \gg 1$

$\Rightarrow \quad R_x \simeq 1/g_m \longrightarrow$ g_m of the input transistor in Telescopic or FC opamp

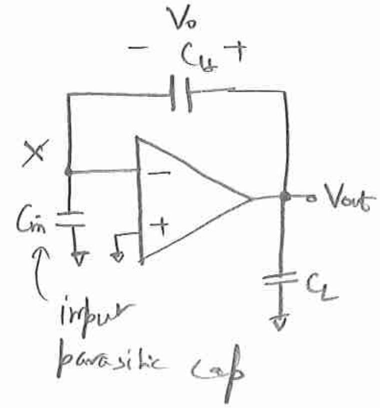
$\Rightarrow$ The time constant during sampling mode

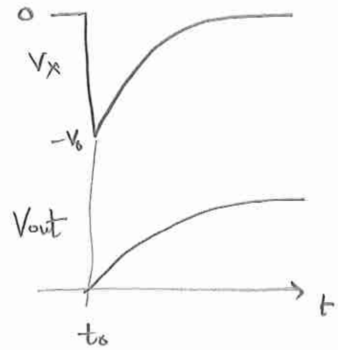
$$\tau_{samp} = \left(R_{on_1} + \frac{1}{g_m}\right) \cdot C_H$$

* τ_{samp} must be sufficiently small to allow settling for the reqd. precision

Speed in the amplification mode:

The circuit must begin with $V_{out} \doteq 0$ and eventually produce $V_{out} \doteq V_0$





Since @ $t = t_0$

$V_{out} \simeq 0$ and $V_{C_H} \doteq V_0$, Assume $C_{in} \ll C_H$

$\Rightarrow$ $V_X = -V_0$ $\because$ voltage across C_L & C_H don't change instantaneously

$\Rightarrow$ the input difference sensed by the opamp initially jumps to a large value

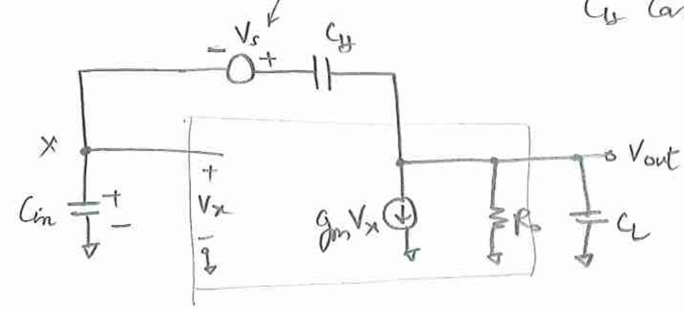
↳ causing slewing in opamp

↳ but assume linear model for now

Circuit model

Voltage across C_H, which goes from 0 to $-V_0$ @ $t = t_0$

C_H carries no charge itself



We want $\dfrac{V_{out}(s)}{V_s(s)}$ and thus the step response

$\rightarrow$

KCL $\quad V_{out}\left(\frac{1}{R_0} + sC_L\right) + g_m V_x = (V_s + V_x - V_{out})\, sC_H \longrightarrow (1)$

KVL $\quad V_x \dfrac{sC_{in}}{sC_H} + V_x + V_s = V_{out} \longrightarrow (2)$

$\because$ current through $C_{in} \rightarrow sC_{in}$

Solving:

$$\frac{V_{out}}{V_s}(s) = R_o \frac{(g_m + s C_{in}) C_H}{R_o(C_L C_{in} + C_{in} C_H + C_H C_L) + g_m R_o C_H + C_H + C_{in}}$$

Since $g_m R_o C_H >> C_H, C_{in}$

$$\Rightarrow \frac{V_{out}}{V_{in}}(s) = \frac{(g_m + sC_{in}) C_H}{(C_L C_{in} + C_{in} C_H + C_H C_L) s + g_m C_H}$$

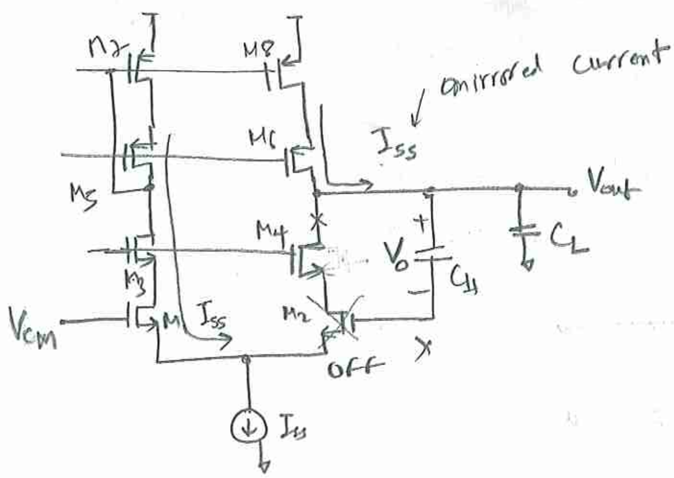
$\Rightarrow$ time-constant of the response

$$\boxed{\tau_{amp} = \frac{C_L C_{in} + C_{in} C_H + C_H C_L}{g_m C_H}}$$

if $C_{in} << C_L, C_H$, then $\tau_{amp} \simeq \frac{C_L}{g_m}$ ← expected result

for larger C_{in} $\tau_{amp} > \frac{C_L}{g_m}$

slewing: Consider single-ended Telescopic for example



upon entering amplification mode, the circuit experiences a large step at the input

M_2 turns off

All the current (I_{ss}) flows through M_1

I_{ss} is mirrored through M_8 & M_6 and charges the output cap, C_L

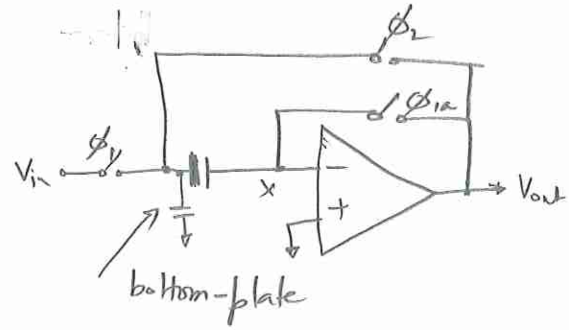
$C_{out,total} = C_L + C_H || C_{in} \simeq C_L$ ← small as M_2 is off

$$\Rightarrow \text{slewing rate} = \frac{I_{ss}}{C_{out,tot}} = \frac{I_{ss}}{C_L}$$

The slewing continues until V_x reaches closer to the gate voltage of M_1 and then the settling progress with τ_{amp}.

(4)

* C_{in} degrades both the speed and precision of the unity-gain sampler / buffer.



→ Bottom plate of the cap must be connected to the input to minimize C_{in}

also bottom plate is noisy (substrate noise) and this avoids noise injection to the input of the opamp.

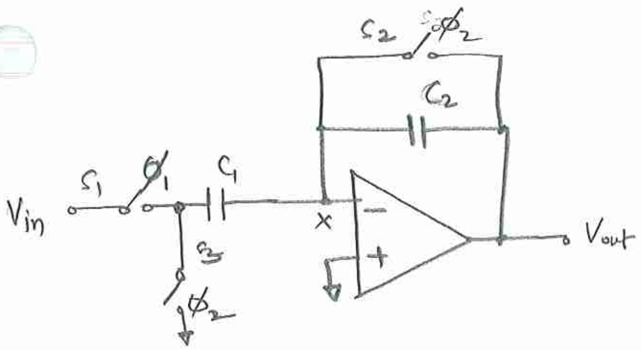
"Bottom plate Sampling". → Go simulate these effects.

→ Here amplification has finite settling time
(−) & it was instantaneous in —o o— $\frac{\;}{\;}C_s$ case

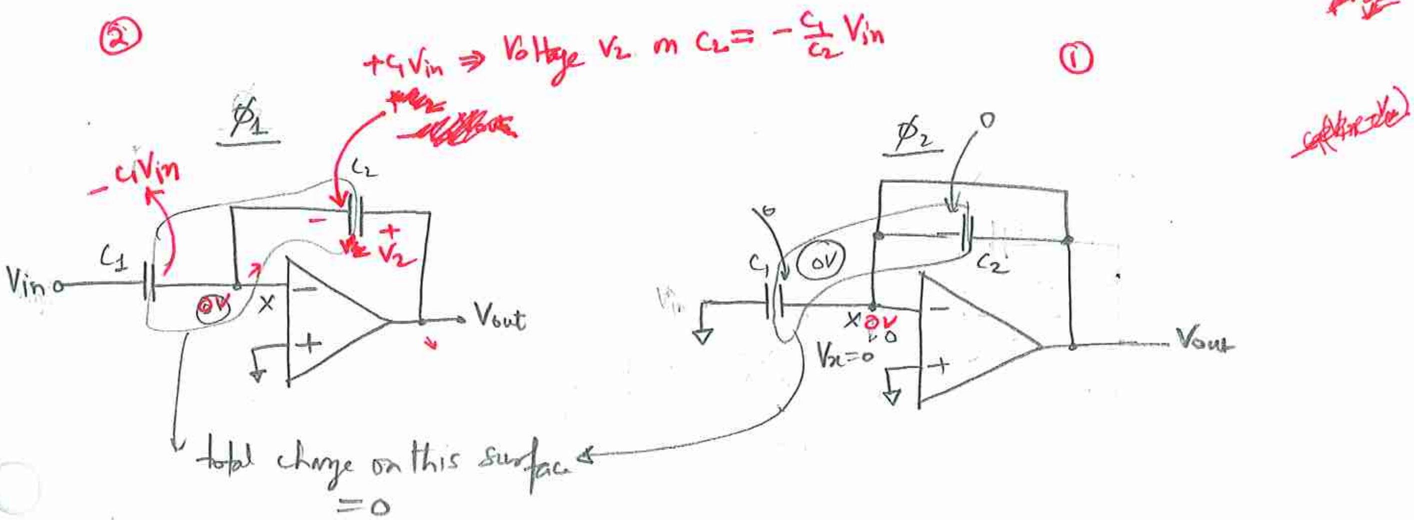
↳ (+) input-independent charge-injection.

Inverting Amplifier:

Now, we are going beyond the unity-gain S/H and looking at SC Amplifier Topologies



In steady-state $V_x \to 0$



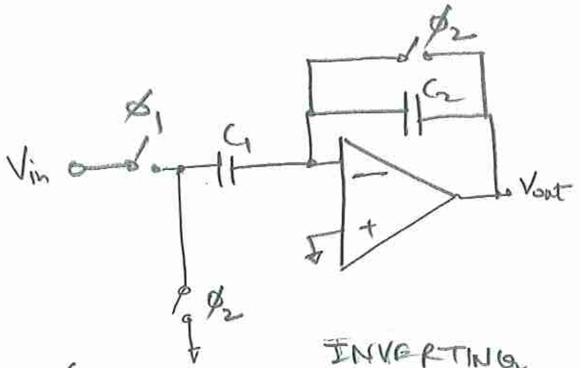
Understand as $\phi_2 \to \phi_1 \to \phi_2$

- ϕ_2: C_{in} connected to ground, C_2 reset
  reset switch provides DC feedback around the opamp $\Rightarrow V_x \approx 0$
- $\phi_1 \Rightarrow$ Input sampled on C_1; C_2 in feedback
- $\phi_2 \to \phi_1 \Rightarrow$ Charge at virtual ground (V_x) is conserved

$$Q = \underbrace{C_1(0) + C_2(0)}_{0} = -C_1 V_{in} - C_2 V_{out} = 0$$

$$\Rightarrow \boxed{V_{out} = -\frac{C_1}{C_2} V_{in}}$$

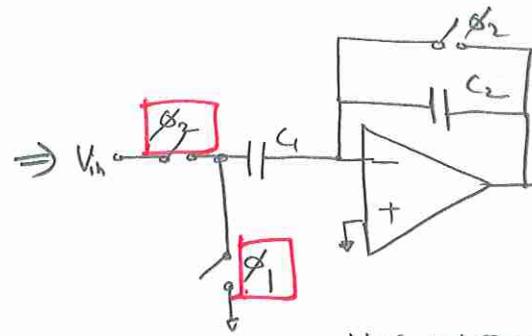
How to design non-inverting amplifier?
$\Rightarrow$ Change the phase of input sampling to invert the gain



$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$$

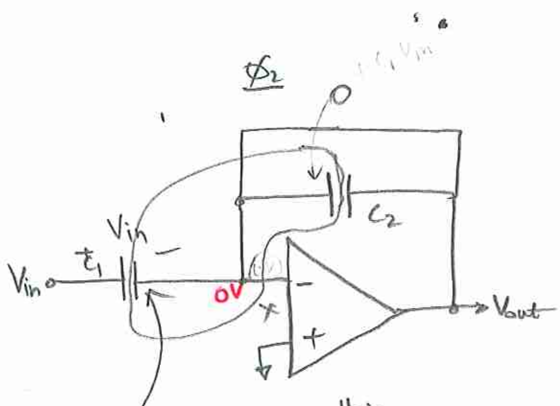
INVERTING

$\Rightarrow$

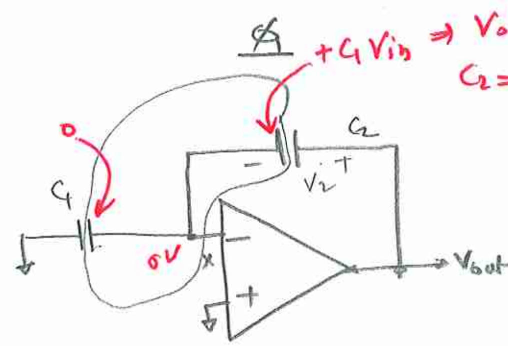


$$\frac{V_{out}}{V_{in}} = +\frac{C_1}{C_2}$$

NON-INVERTING



total charge on this surface $= -C_1 V_{in}$



$+C_1 V_{in} \Rightarrow$ Voltage V_2 on $C_2 = \cancel{\pm} + \frac{C_1}{C_2} V_{in}$

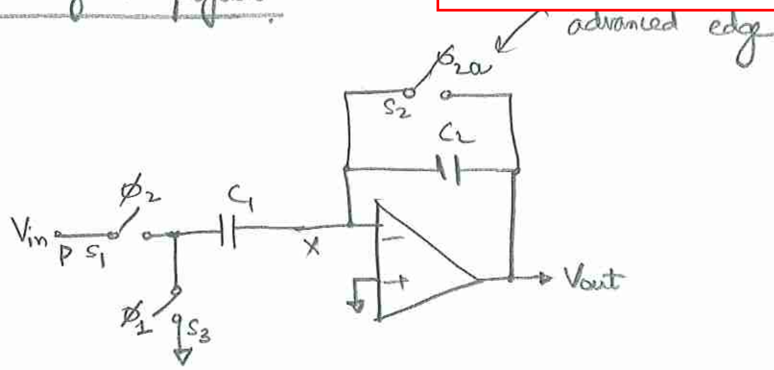
$\Rightarrow$ charge conservation at node X

$$(0 - V_{in})C_1 + (0)C_2 = (0)C_1 + (-V_{out})C_2$$

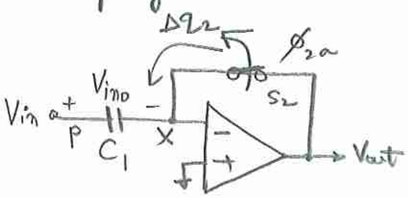
$$\Rightarrow \boxed{\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2}}$$

Noninverting amplifier

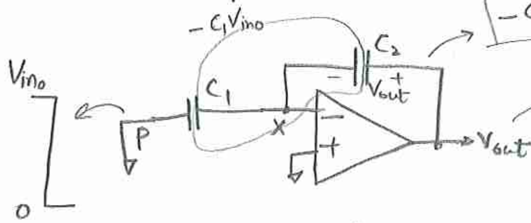
Non-inverting Amplifier



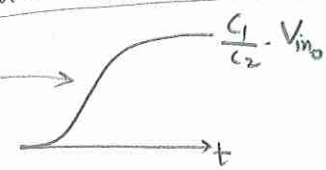
Sampling mode (ϕ_2)



amp mode (ϕ_1)



$$\boxed{-C_2V_{out} = -C_1V_{in0} \Rightarrow V_{out} = \frac{C_1}{C_2}V_{in0}}$$



* Voltage across C_1 tracks V_{in}
* S_2 (ϕ_{2a}) turns off first injecting constant charge Δq_2 onto node X.
* Then S_1 (ϕ_2) turns off (CI sucked into Vin Source)

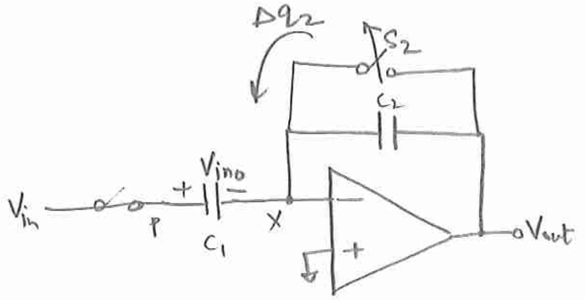
* S_3 (ϕ_1) turns on

V_P goes from V_{in0} to 0

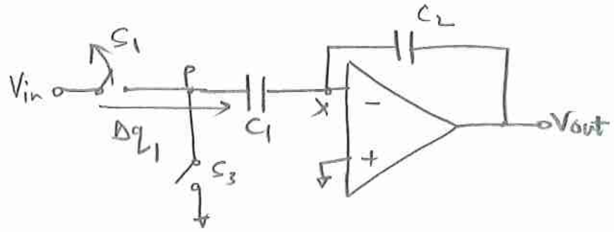
V_{out} changes from 0 to $V_{in0}\left(\frac{C_1}{C_2}\right)$

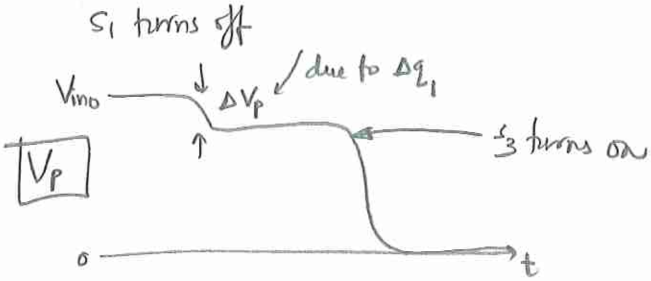
voltage gain $= \frac{C_1}{C_2}$

* Total charge at node X remains constant, making the circuit insensitive to charge injection of S_1 & charge absorption of S_3.



Δq_2 is a constant charge injected into C_1





Let's carefully study the effect of S_1 charge injection carefully

→ Δq_1 changes the voltage at node P by $\Delta V_P \simeq \frac{\Delta q_1}{C_1}$

↳ V_{out} changes by $-\Delta q_1 \times \frac{C_1}{C_2} = -\frac{\Delta q_1}{C_2}$

↳ However, after S_3 turns ON, V_P drops to zero

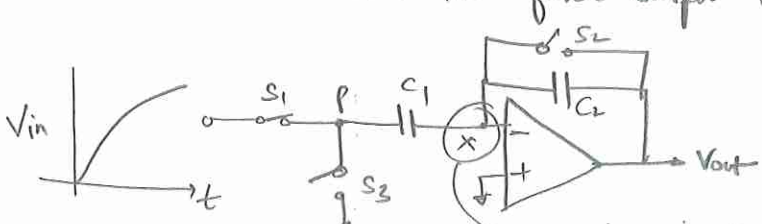
⇒ Overall change in $V_P \Rightarrow 0 - V_{ino} = -V_{ino}$

⇒ Overall change in output $\Rightarrow -V_{ino}\left(-\frac{C_1}{C_2}\right) = V_{ino}\cdot\frac{C_1}{C_2}$

⇒ intermediate perturbations due to S_1 don't matter as the total charge at node X must remains fixed.
↓
or conserved.

* Also the input may change significantly after S_2 is turned off

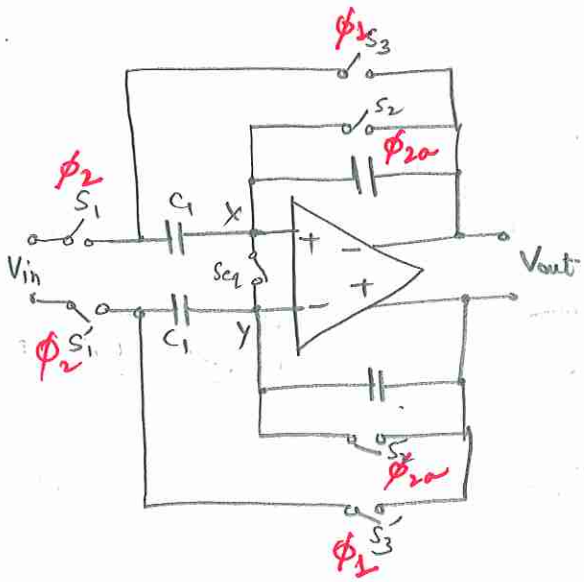
↳ still the final output is not changed.



→ Charge is conserved.

FD implementation:

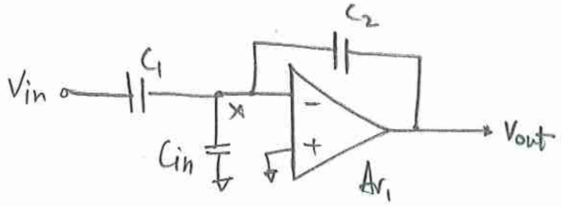
Fully-Differential Implementation



Precision Considerations

The circuit provides a nominal voltage gain of $\frac{C_1}{C_2}$.

Opamp gain A_{v_1}



$$(V_{out} - V_x)sC_2 = V_x sC_{in} + (V_x - V_{in})sC_1 \longrightarrow ①$$

$$\& \quad V_{out} = -A_{v_1} V_x \longrightarrow ②$$

$$\Rightarrow \left|\frac{V_{out}}{V_{in}}\right| = \frac{C_1}{C_2 + \frac{C_2 + C_1 + C_{in}}{A_{v_1}}}$$

for large A_{v_1}

Precision considerations

$$\left|\frac{V_{out}}{V_{in}}\right| \simeq \frac{C_1}{C_2}\Bigg[1 - \underbrace{\frac{C_2 + C_1 + C_{in}}{C_2} \cdot \frac{1}{A_{v_1}}}_{\text{gain error}}\Bigg] = \frac{C_1}{C_2}\left[1 - \frac{1}{A\beta}\right]$$

$\Rightarrow$ gain error increases with the nominal gain $\left(\frac{C_1}{C_2}\right)$

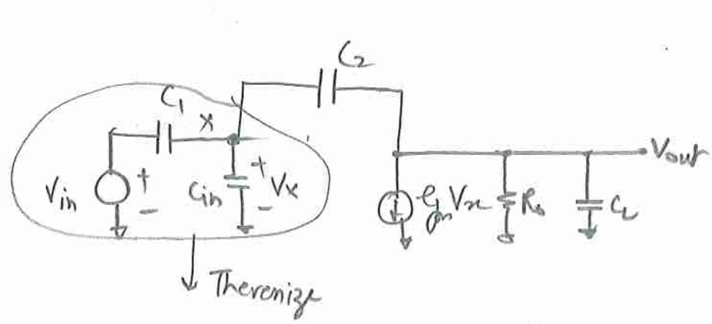
feedback factor $\beta = \frac{C_2}{C_2 + C_1 + C_{in}}$

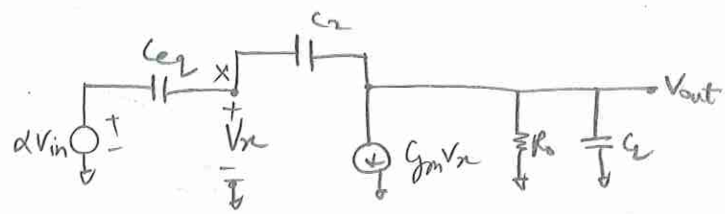
Speed Considerations

Speed Considerations :

A lower $\beta \Rightarrow f_{3dB} = \beta f_{un}$

$\Rightarrow$ slower time response





Thevenize the input side:

$$\alpha = \frac{C_1}{C_1 + C_{in}}$$

$$C_{eq} = C_1 + C_{in}$$

$$\Rightarrow \quad V_x = (\alpha V_{in} - V_{out}) \frac{C_{eq}}{C_{eq} + C_2} + V_{out}$$

$\Rightarrow$

$$\left[(\alpha V_{in} - V_{out}) \frac{C_{eq}}{C_{eq}+C_2} + V_{out}\right] G_m + V_{out}\left(\frac{1}{R_o} + sC_L\right) = (\alpha V_{in} - V_{out})\, s \frac{C_{eq} C_2}{C_{eq} + C_2}.$$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}}(s) = \frac{-C_{eq}\frac{C_1}{C_1 + C_{in}}(G_m - sC_2)R_o}{C_2 G_m R_o + C_{eq} + C_2 + R_o\left[C_L(C_{eq}+C_2) + C_{eq}C_2\right]s}$$

Assume $G_m R_o >> 1$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}}(s) \simeq \frac{-C_{eq}\frac{C_1}{C_1 + C_{in}}(G_m - sC_2)R_o}{R_o\left(C_L C_{eq} + C_L C_2 + C_{eq} C_2\right]s + G_m R_o C_2}$$

$\Rightarrow$ Time constant

$$\tau_{amp} = \frac{C_L C_{eq} + C_L C_2 + C_{eq} C_2}{G_m C_2}$$

Same as the S/H τ_{amp} if C_{in} is replaced by $C_{in} + C_1$

for $C_2 = 0$

$$\tau_{amp} = \frac{C_1 + C_{in}}{-g_m}$$ ← independent of feedback cap C_2

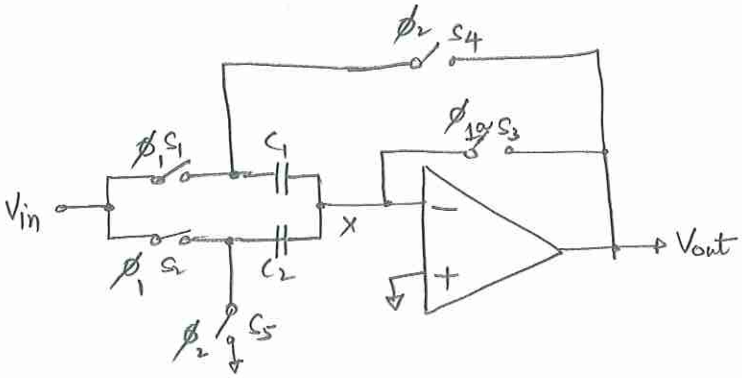
a larger C_2 introduces heavier loading
it also provides a greater feedback factor

- The negative gain in the equation means when the input plate of C_1 is stepped down, the output goes up.

Precision Multiply-by-2 Circuit

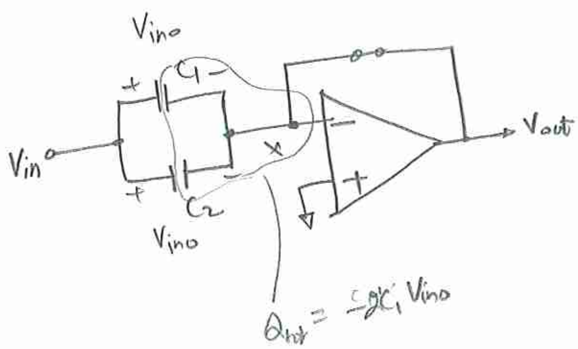
Precision Multiply by 2 Circuit

* The previous circuit can realize large loop gain but suffer from a low feedback factor

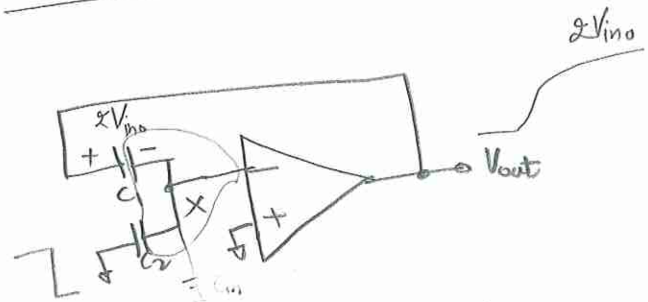


$C_1 = C_2 = C$

ϕ_1 (sampling mode)



ϕ_2 (amplification mode)



$-2V_{ino} \cdot C_1 = -C_1 V_{out}$

$\Rightarrow$ $\underline{V_{out} = 2V_{ino}}$.

↓

higher feedback factor for a given loop-gain

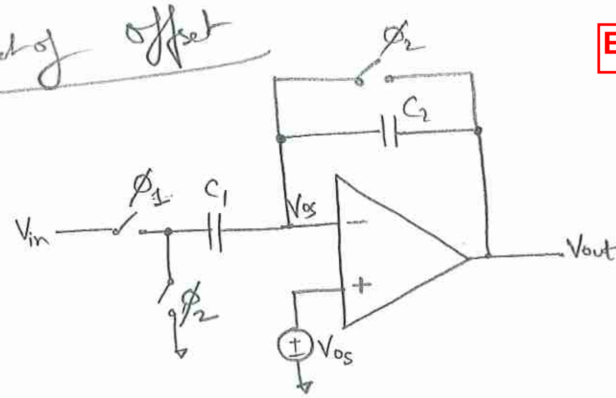
previous

$$\frac{C_2}{\underbrace{2C_1 + C_2 + C_{in}}_{C_1}} \longrightarrow \frac{C_1}{C_1 + C_2 + C_{in}}$$

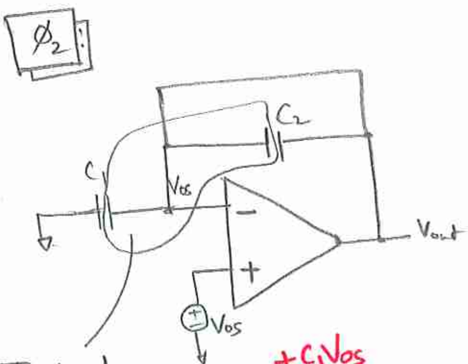
However input cap is twice in the sampling mode.

Effect of Opamp Offset

Effect of Offset

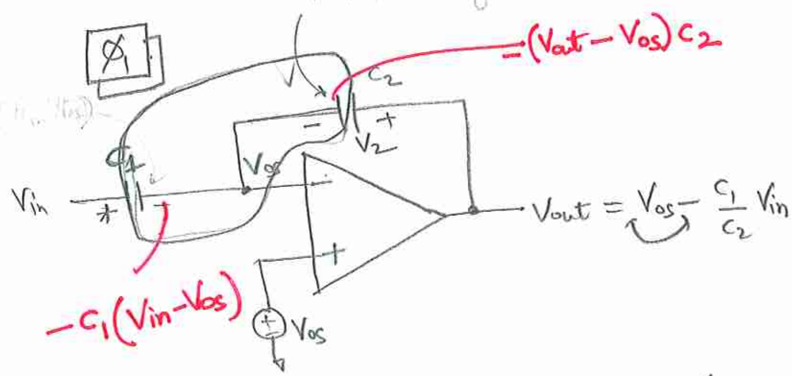


$\boxed{\phi_2}$:



Total charge on the surface $= C_1 V_{os}$ $+C_1V_{os}$

$\boxed{\phi_1}$



$$-C_1 V_{in} + \cancel{C_1 V_{os}} - C_2 V_{out} + C_2 V_{os} = \cancel{C_1 V_{os}}$$

$$\Rightarrow \quad V_{out} = -\frac{C_1}{C_2} V_{in} + V_{os}$$

$\boxed{\phi_2}$ C_1 is charged to $(V_{in}-V_{os})$ instead of V_{in}

$\Rightarrow$ input offset cancellation

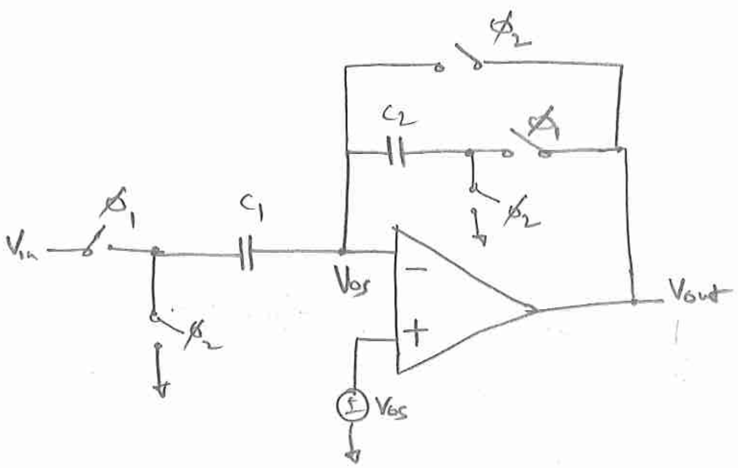
↳ no offset in voltage across $C_2 \Rightarrow V_2 = -\frac{C_1}{C_2} V_{in}$

$\boxed{\phi_1}$

* $V_{out} = -\frac{C_1}{C_2} V_{in} + V_{os}$ $\Leftarrow$ unity gain for offset instead of $\left(1+\frac{C_1}{C_2}\right)$ as in CT amplifier.

Correction of offset on C_2

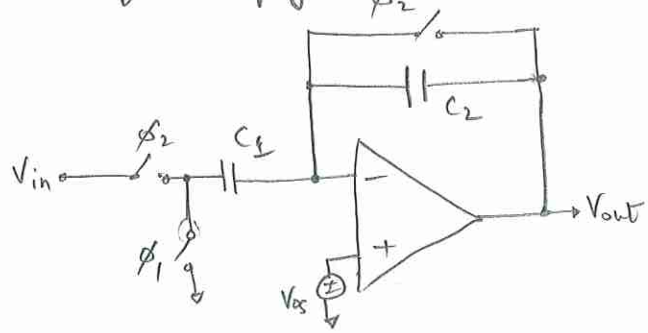
Correction of offset on C2



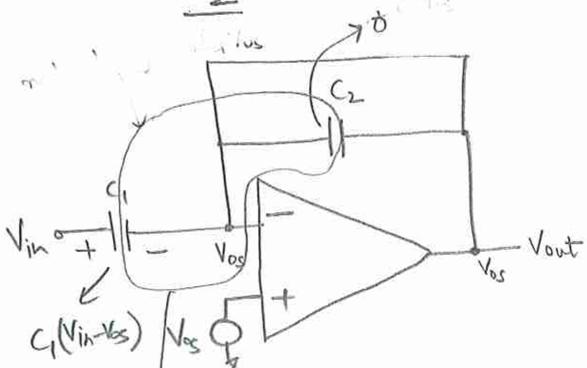
ϕ_2: charge C_2 to the offset voltage instead of 0V

ϕ_1: $V_{out} = -\frac{C_1}{C_2} V_{in}$ $\Rightarrow$ offset completely cancelled non-inverting Amplifier Offset Effect.

1B



$\underline{\phi_2}$:



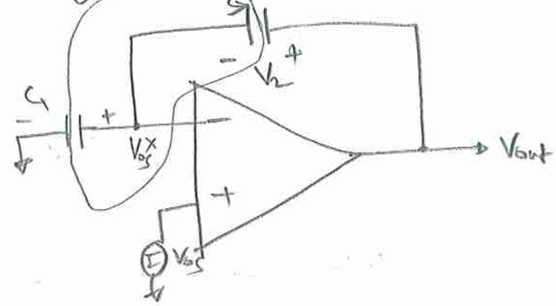
net charge on this surface $= -C_1(V_{in}-V_{os})$

net charge is conserved $= -C_1(V_{in}-V_{os})$

$\underline{\phi_1}$:

$-C_1(V_{in}-V_{os}) - C_1V_{os}$

$C_2 = -C_1V_{in}$



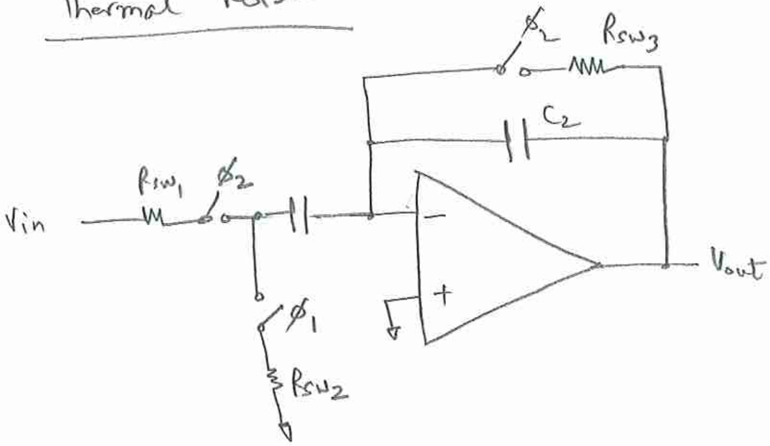
$\Rightarrow \quad -C_2V_2 = -C_1V_{in}$

$\Rightarrow \quad V_2 = \frac{C_1}{C_2}V_{in}$

$\Rightarrow \quad \boxed{V_{out} = V_{os} + \frac{C_1}{C_2}V_{in}}$

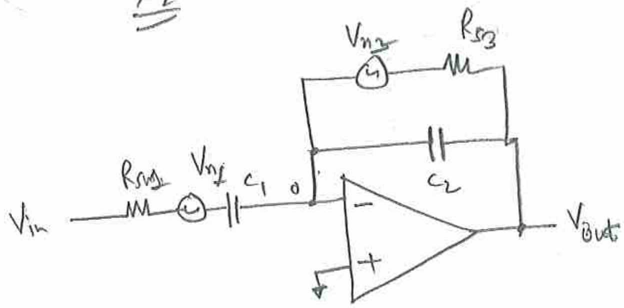
Thermal Noise in SC Amplifiers

Thermal Noise

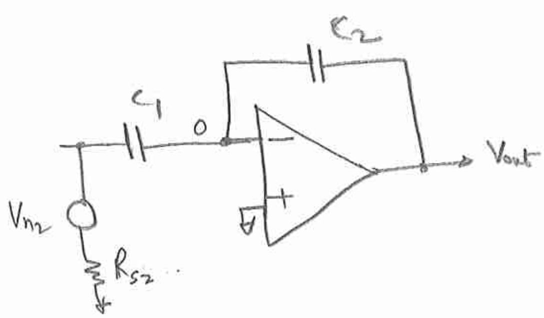


* Noise from opamp ignored here.

ϕ_2



ϕ_1



ϕ_2

$R_{s_1} \Rightarrow C_1$ has noise variance $\frac{kT}{C_1}$

$R_{s_3} \Rightarrow C_2$ has noise variance $\frac{kT}{C_2}$

ϕ_1

- $R_{s_1} \Rightarrow$ It's contribution in ϕ_2 i.e. $\frac{kT}{C_1}$ is amplified by $\left(\frac{C_1}{C_2}\right)^2$

$\Rightarrow \frac{kT}{C_1} \cdot \left(\frac{C_1}{C_2}\right)^2$

* $R_{s_3} \Rightarrow$ It's contribution in ϕ_2 i.e. $\frac{kT}{C_2}$ is held

* $R_{s_2} \Rightarrow$ Results in a noise $\frac{kT}{C_1}$ on C_1 and $\frac{kT}{C_1} \cdot \left(\frac{C_1}{C_2}\right)^2$ at the output

$\Rightarrow$ Total output noise $= 2\frac{kT}{C_1}\left(\frac{C_1}{C_2}\right)^2 + \frac{kT}{C_2} = \frac{kT}{C_1}\left[2\left(\frac{C_1}{C_2}\right)^2 + \frac{C_1}{C_2}\right]$

$\Rightarrow$ Input referred noise $\Rightarrow \dfrac{\frac{kT}{C_1}\left[2\left(\frac{C_1}{C_2}\right)^2 + \frac{C_1}{C_2}\right]}{\left(C_1/C_2\right)^2} = \frac{kT}{C_1}\left[2 + \frac{C_2}{C_1}\right] = \boxed{2.5\frac{kT}{C_1}}$ for gain of 2

$\Rightarrow$ C_1 should be large enough