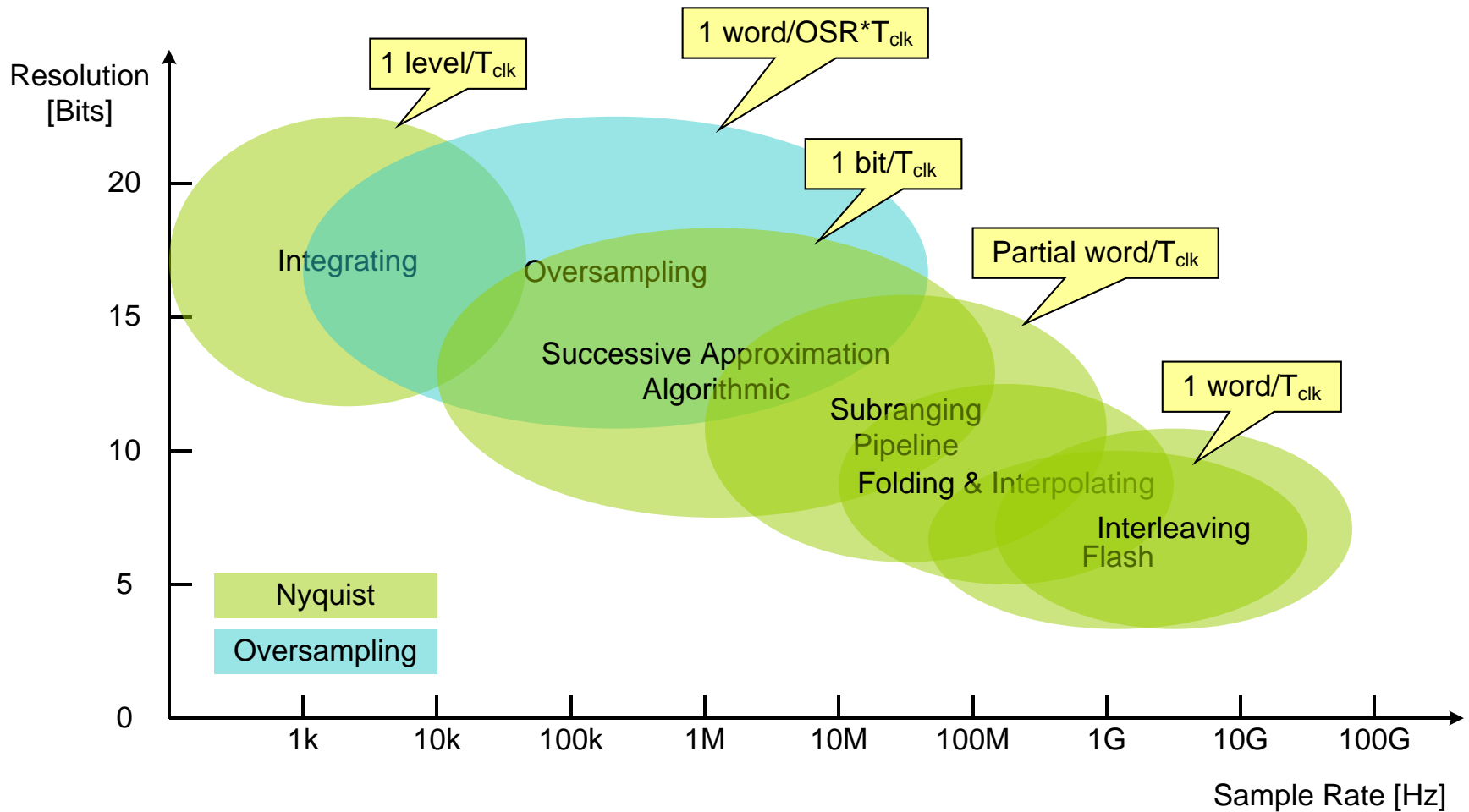


# Successive Approximation ADCs

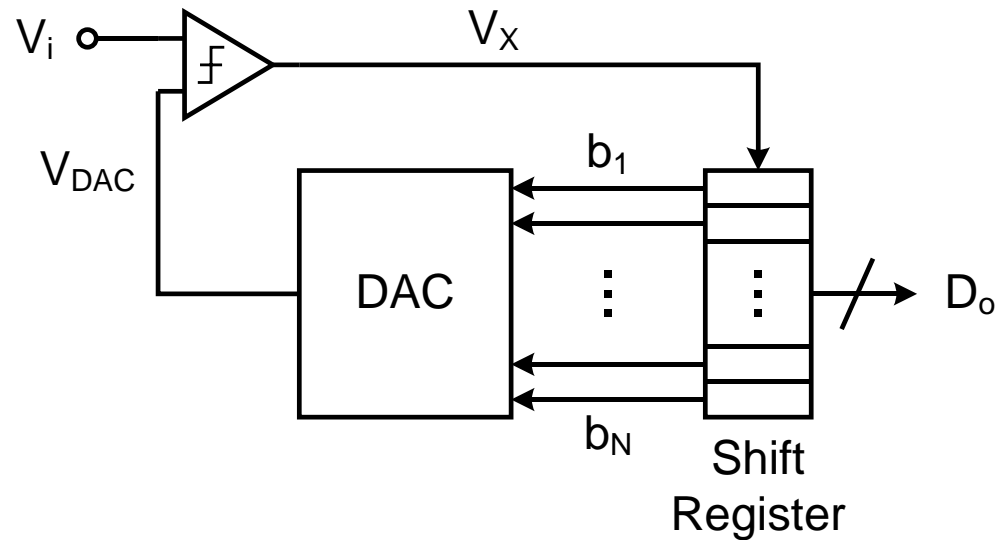
Vishal Saxena

# Successive Approximation ADC

# Data Converter Architectures

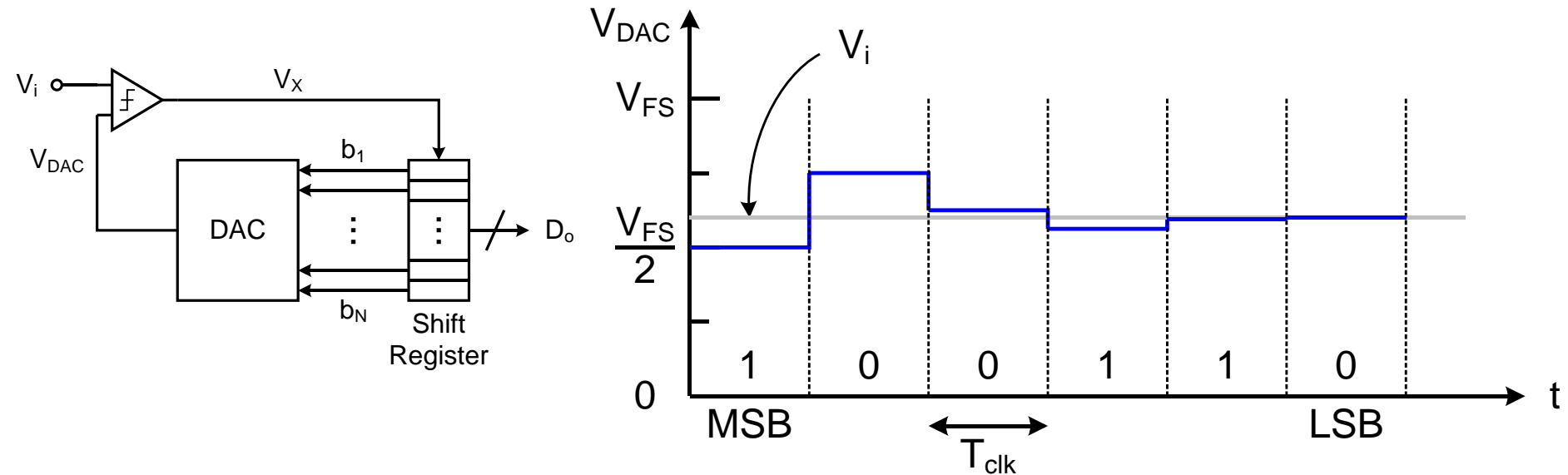


# Successive Approximation ADC



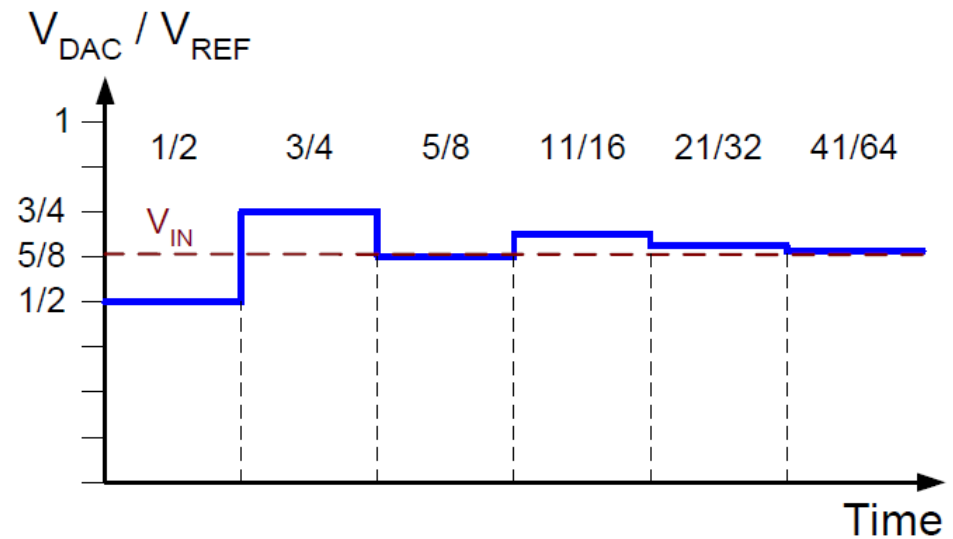
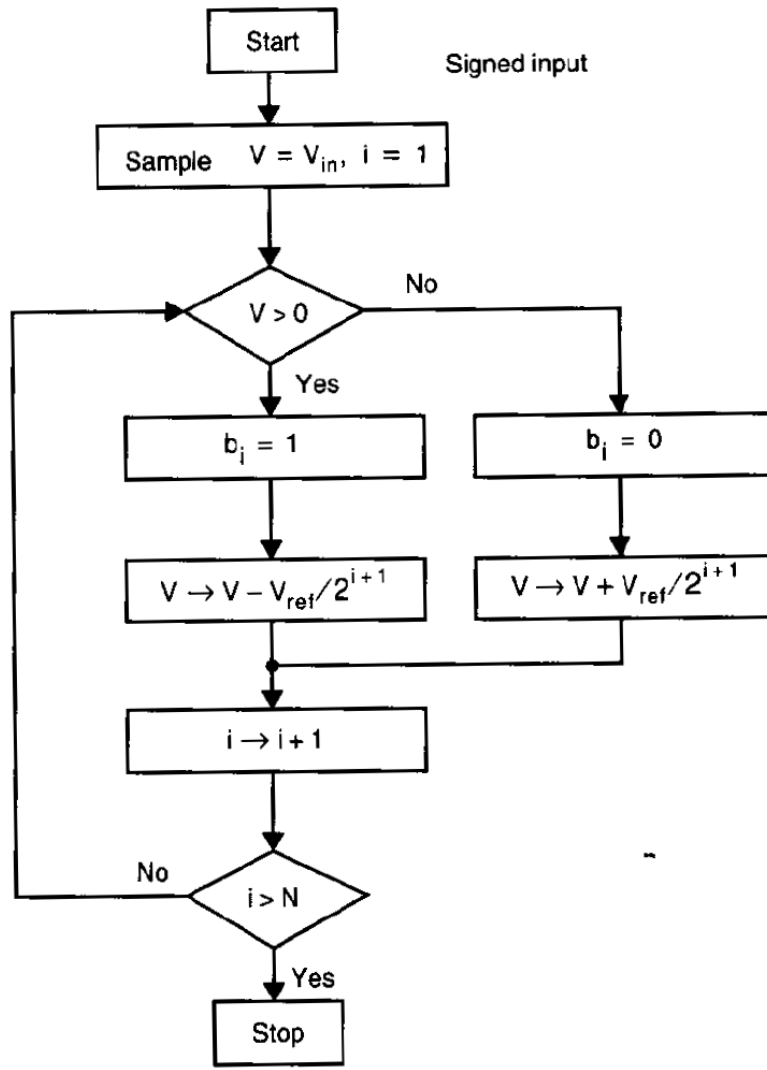
- Binary search over DAC inputs
  - $N \cdot T_{clk}$  to complete N bits
  - successive approximation register or SAR
- High accuracy achievable (16+ bits)
  - Relies on highly accurate comparator
- Moderate speeds (typically 0.1-10 MHz parts)

# Binary Search Algorithm



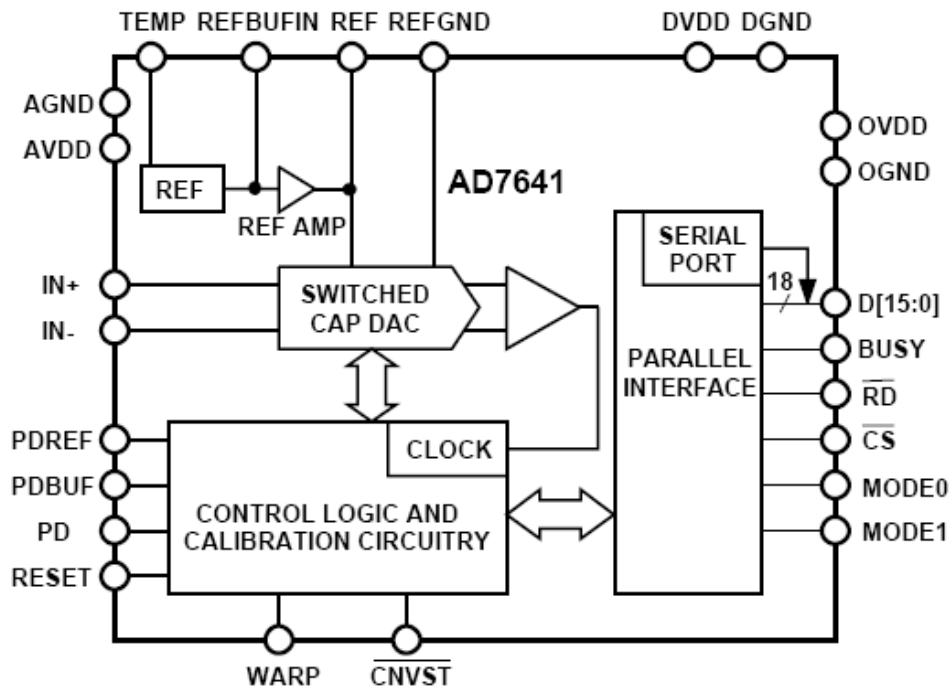
- DAC output gradually approaches the input voltage
- Comparator differential input gradually approaches zero

# Binary Search Algorithm contd.



# High Performance Example

## FUNCTIONAL BLOCK DIAGRAM

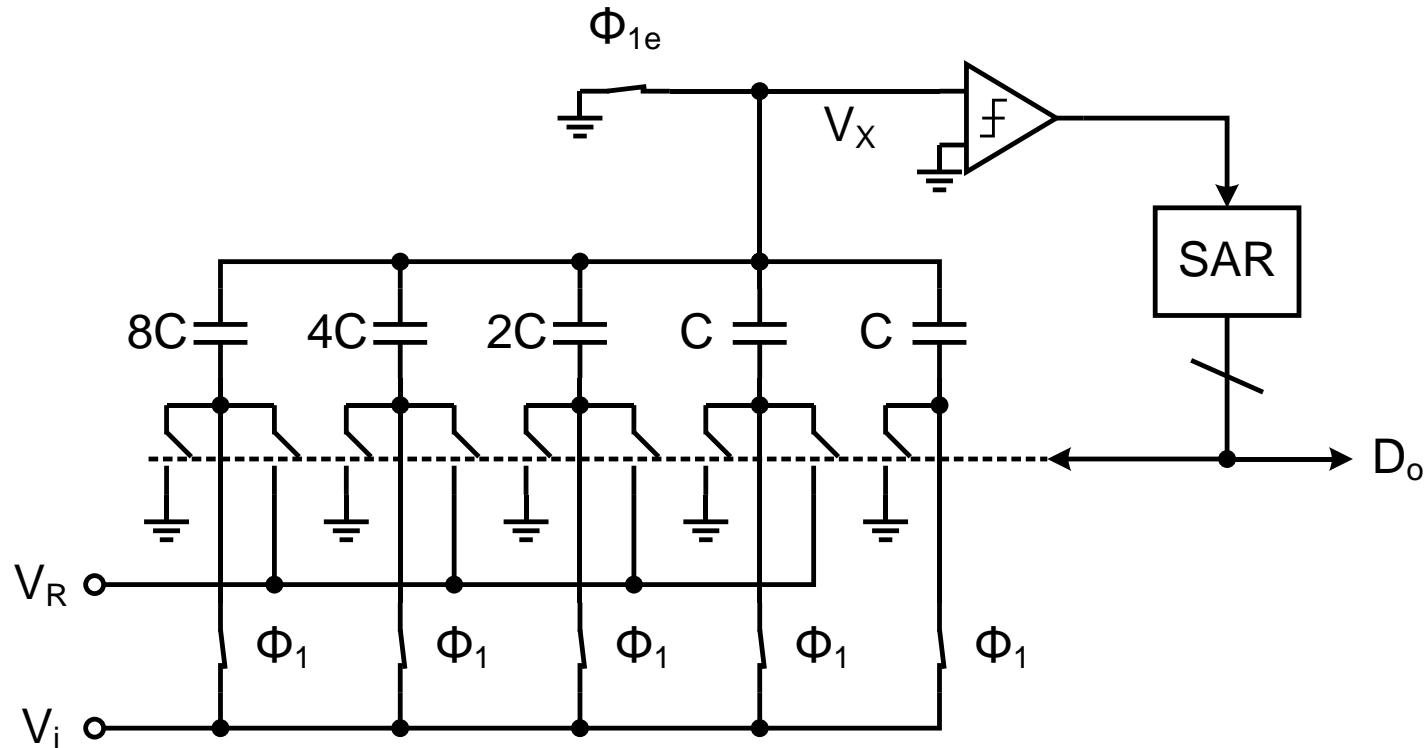


## FEATURES

### Throughput:

- 2 MSPS (Warp mode)
- 1.5 MSPS (Normal mode)
- 18-bit resolution with no missing codes
- 2.048V internal low drift reference
- INL:  $\pm 2$  LSB typical
- S/(N+D): 93 dB typical @ 20 kHz
- THD:  $-115$  dB typical @ 20 kHz
- Differential input range:  $\pm V_{REF}$  ( $V_{REF}$  up to 2.5 V)
- No pipeline delay (SAR architecture)
- Parallel (18-, 16-, or 8-bit bus)
- Serial 5 V/3.3 V/2.5 V interface
- SPI®/QSPI™/MICROWIRE™/DSP compatible
- Single 2.5 V supply operation
- Power dissipation: 65 mW typical @ 2 MSPS

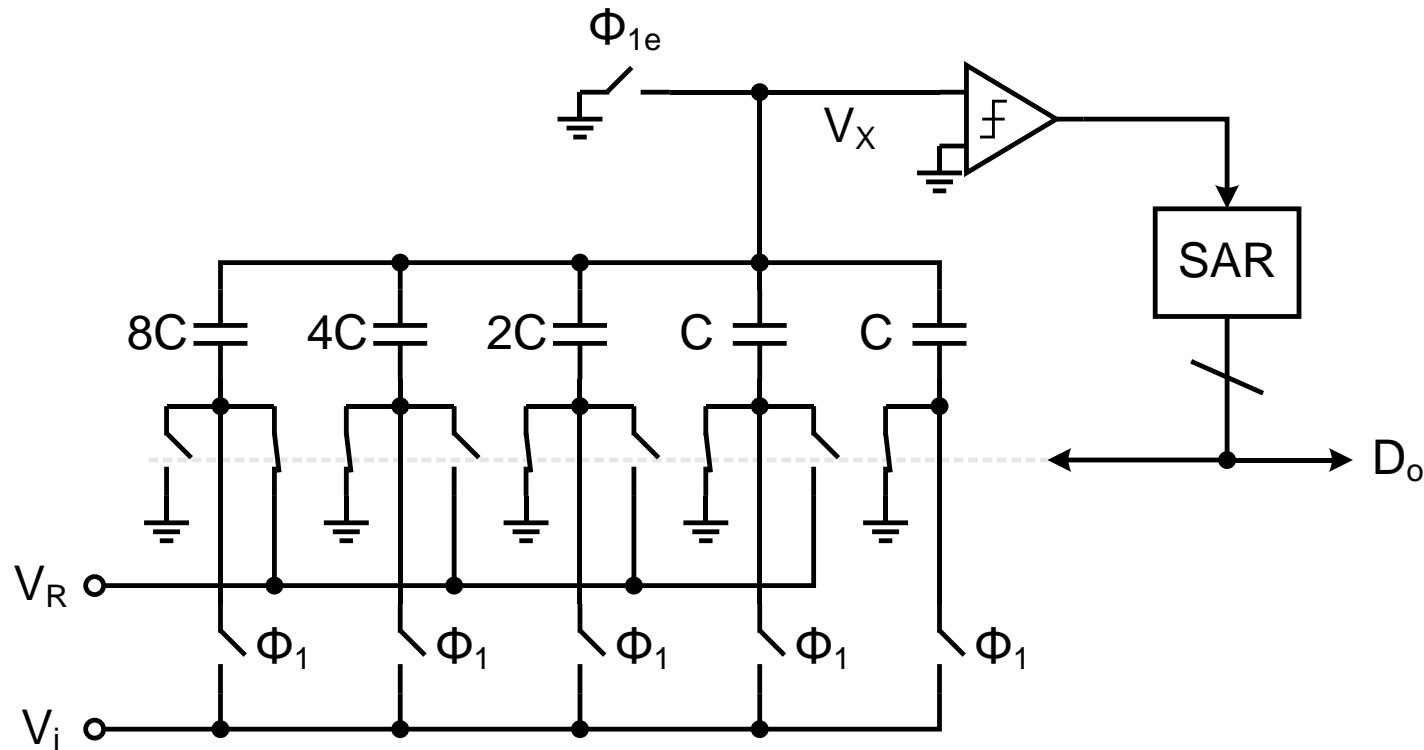
# Charge Redistribution SAR ADC



- 4-bit binary-weighted capacitor array DAC (*aka* charge scaling DAC)
- Capacitor array samples input when  $\Phi_1$  is asserted (bottom-plate)
- Comparator acts as a zero crossing detector
- Practical implementation is fully-differential



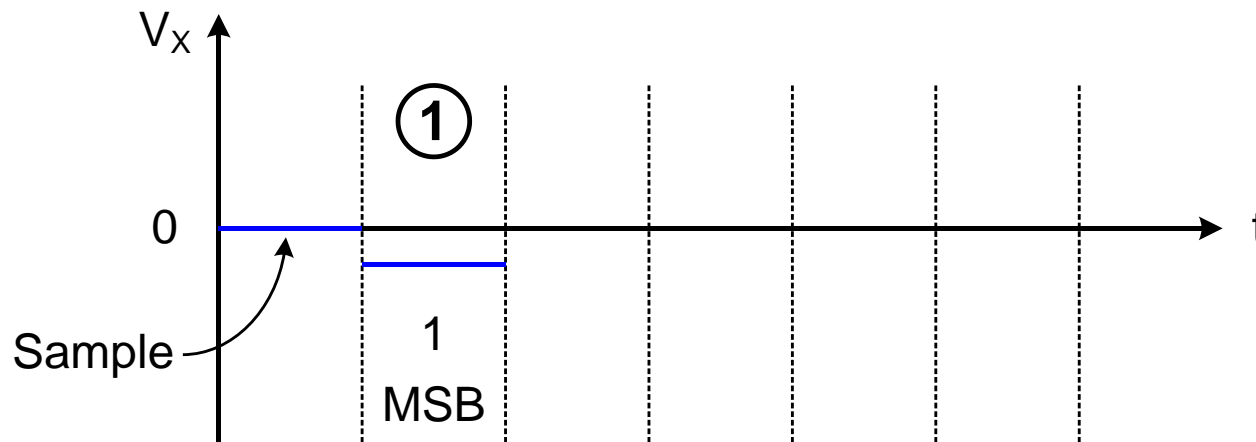
# Charge Redistribution (MSB)



- Start with  $C_4$  connected to  $V_R$  and others to 0 (i.e. SAR=1000)

$$V_i \cdot 16C = (V_R - V_X)C_4 - V_X(C_3 + C_2 + C_1 + C_0) \Rightarrow V_X = \frac{V_R \cdot 8C - V_i \cdot 16C}{16C} = \frac{V_R}{2} - V_i$$

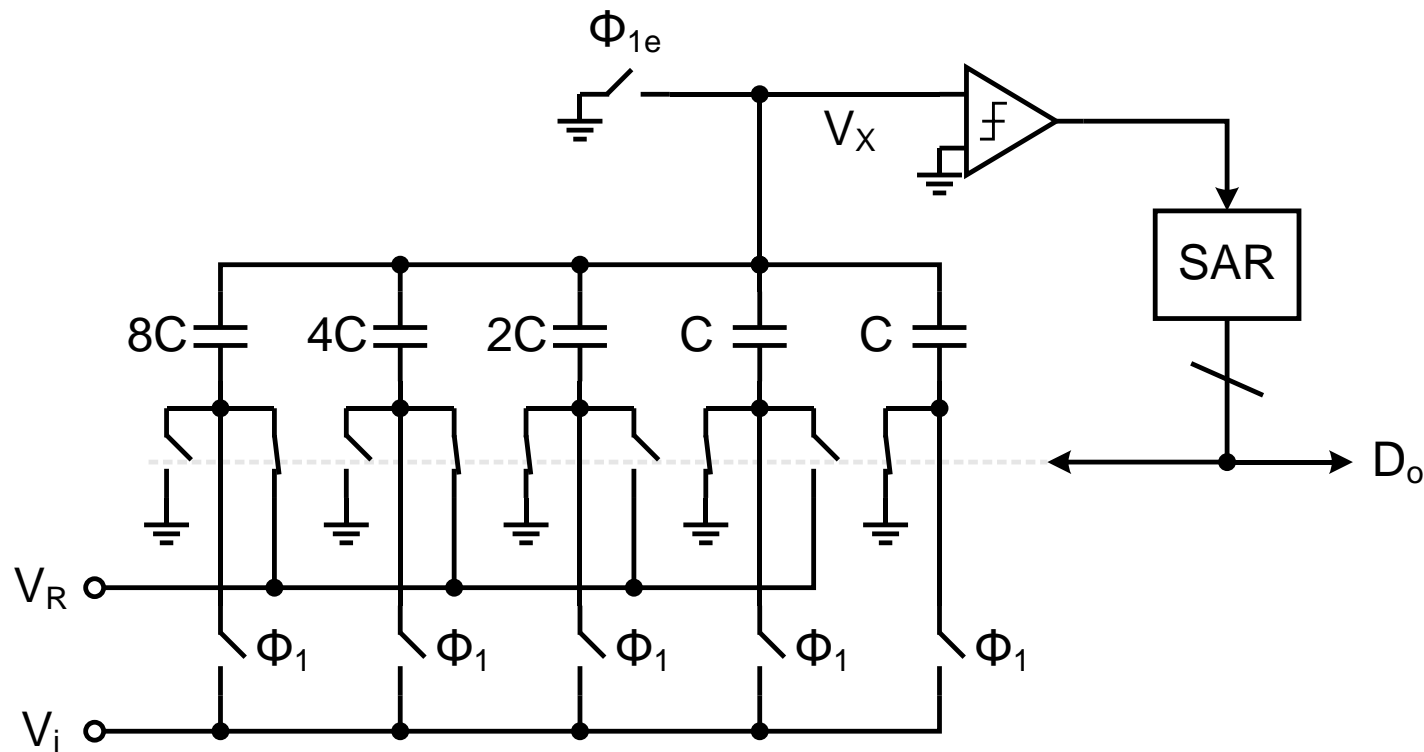
# Comparison (MSB)



$$\text{MSB TEST : } V_X = \frac{V_R}{2} - V_i$$

- If  $V_X < 0$ , then  $V_i > V_R/2$ , and  $\text{MSB} = 1$ ,  $C_4$  remains connected to  $V_R$
- If  $V_X > 0$ , then  $V_i < V_R/2$ , and  $\text{MSB} = 0$ ,  $C_4$  is switched to ground

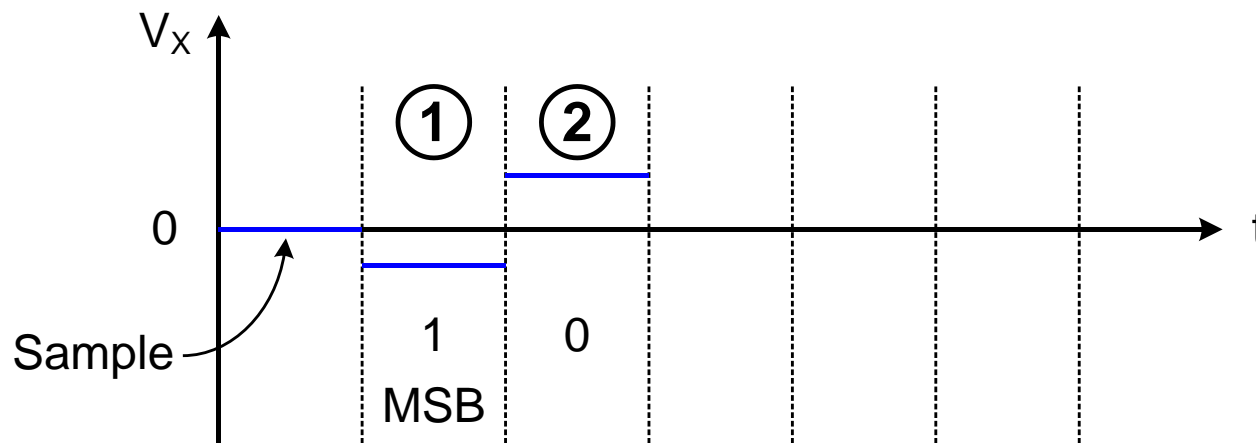
# Charge Redistribution (MSB-1)



- SAR=1100

$$V_i \cdot 16C = (V_R - V_X) \cdot 12C - V_X \cdot 4C \Rightarrow V_X = \frac{V_R \cdot 12C - V_i \cdot 16C}{16C} = \frac{3}{4} V_R - V_i$$

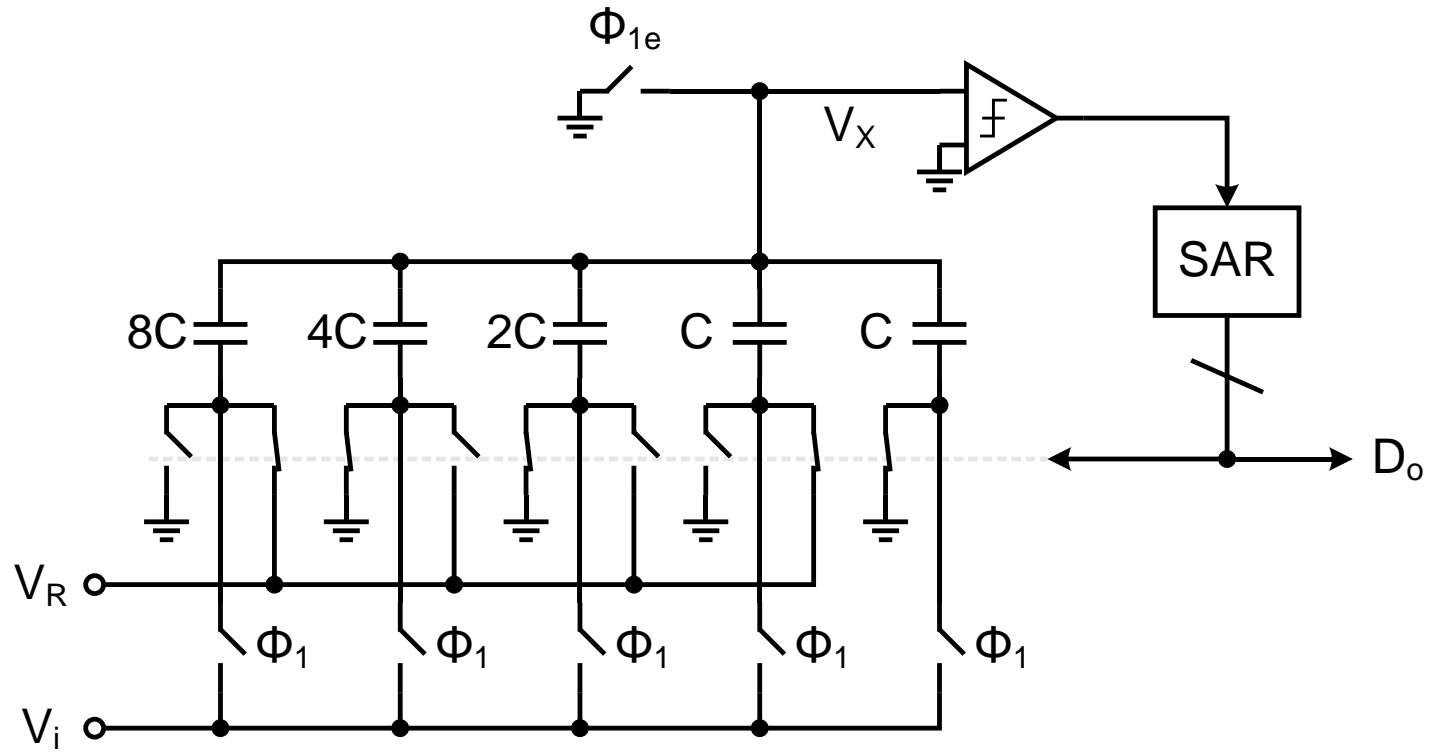
# Comparison (MSB-1)



$$(\text{MSB-1}) \text{ TEST: } V_X = \frac{3}{4} V_R - V_i$$

- If  $V_X < 0$ , then  $V_i > 3V_R/4$ , and  $\text{MSB-1} = 1$ ,  $C_3$  remains connected to  $V_R$
- If  $V_X > 0$ , then  $V_i < 3V_R/4$ , and  $\text{MSB-1} = 0$ ,  $C_3$  is switched to ground

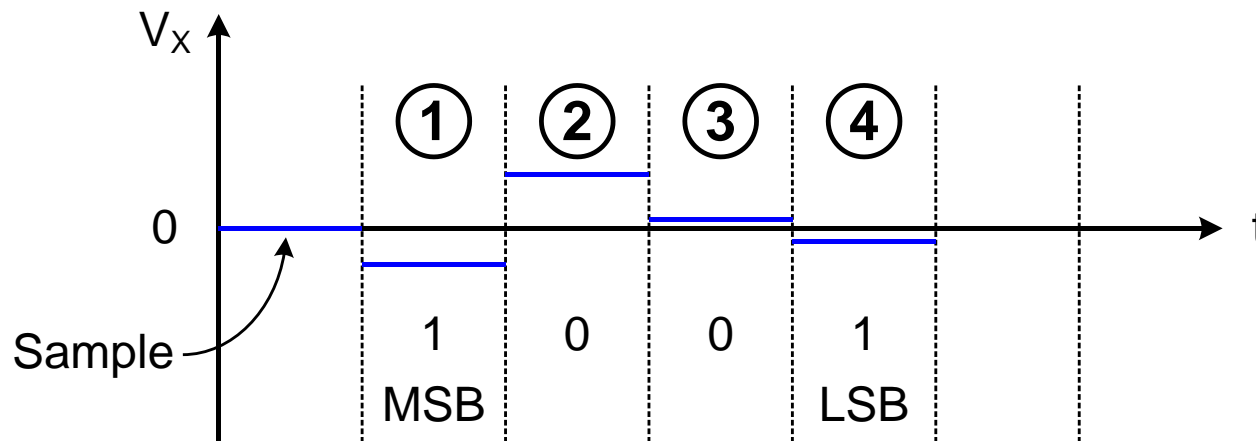
# Charge Redistribution (Other Bits)



- SAR=1010, and so on...

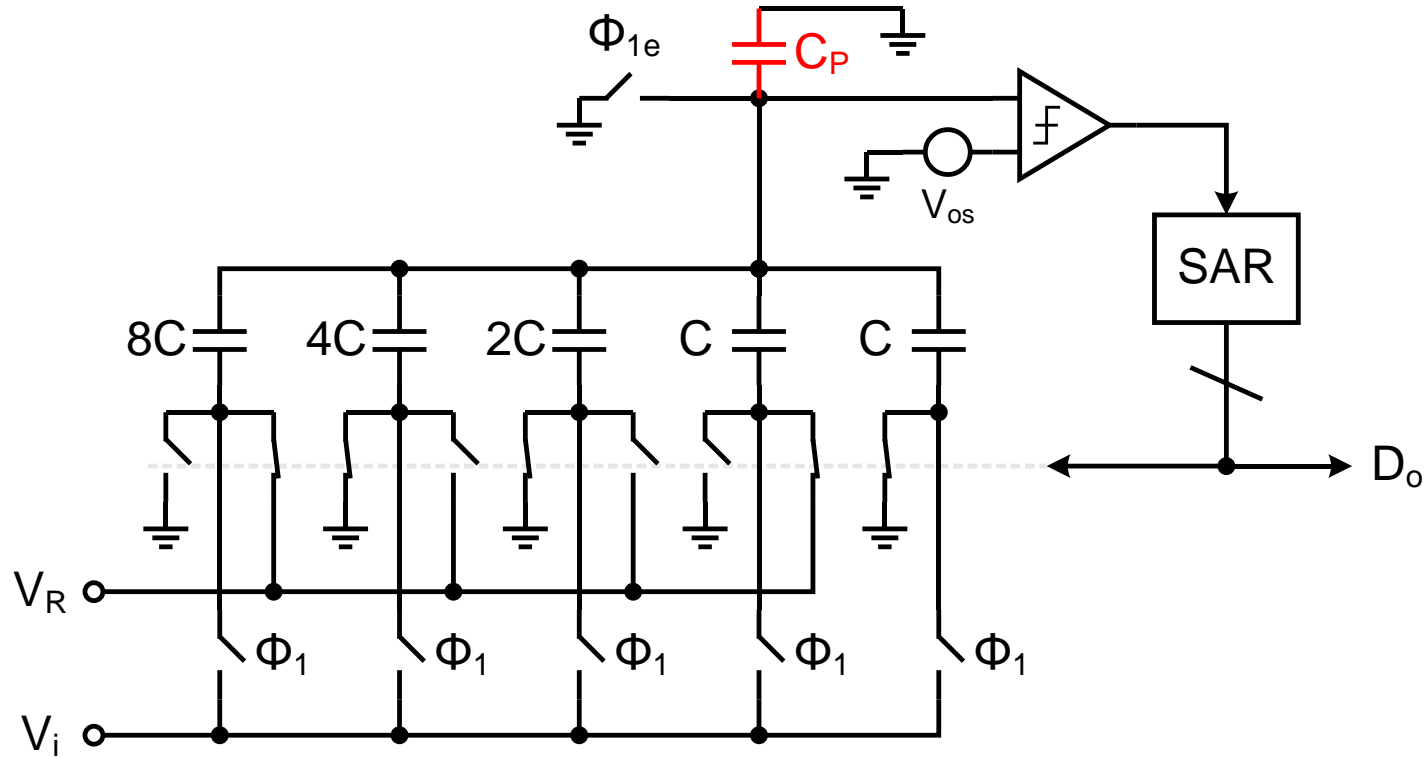
Test completes when all four bits are determined w/ four charge redistributions and comparisons

# After Four Clock Cycles...



- Usually, half  $T_{\text{clk}}$  is allocated for charge redistribution and half for comparison + digital logic
- $V_X$  always converges to 0 ( $V_{\text{os}}$  if comparator has nonzero offset)

# Summing-Node Parasitics



- If  $V_{OS} = 0$ ,  $C_P$  has no effect eventually; otherwise,  $C_P$  attenuates  $V_X$
- Auto-zeroing can be applied to the comparator to reduce offset

# SAR ADC Considerations

- Power efficiency – only comparator consumes DC power
- Conversion rate typically limited by finite bandwidth of RC network during sampling and bit-tests
- For high resolution, the binary weighted capacitor array can become quite large
  - E.g. 16-bit resolution,  $C_{\text{total}} \sim 100\text{pF}$  for reasonable  $kT/C$  noise contribution
- If matching is an issue, an even larger value may be needed
  - E.g. if matching dictates  $C_{\text{min}} = 10\text{fF}$ , then  $2^{16}C_{\text{min}} = 655\text{pF}$



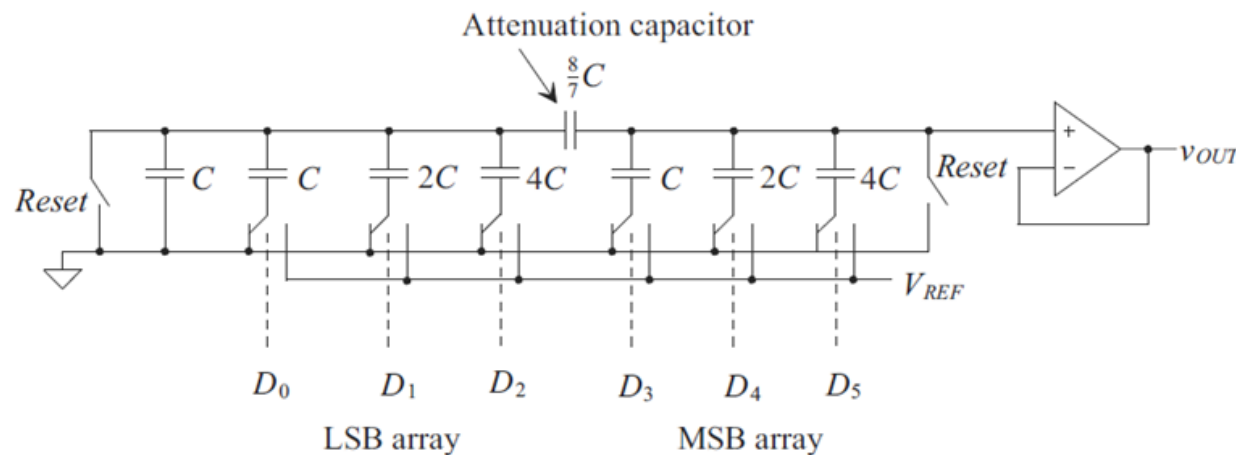
# SAR ADC Considerations contd.

- Comparator offset  $V_{os}$  introduces an input-referred offset  $\sim (1+C_P/\Sigma C_j)*V_{os}$
- $C_P$  in general has little effect on the conversion ( $V_X \rightarrow 0$  at the end of the search)
  - however,  $V_X$  is always attenuated due to charge sharing of  $C_P$
- Binary search is sensitive to intermediate errors made during search – if an intermediate decision is wrong, the digitization process cannot recover
  - DAC must settle into  $\pm 1/2$  LSB bound within the time allowed
  - Comparator offset must be constant (no hysteresis or time-dependent offset)
  - Non-binary search algorithm can be used (Kuttner, ISSCC'02)

# SAR ADC Considerations contd.

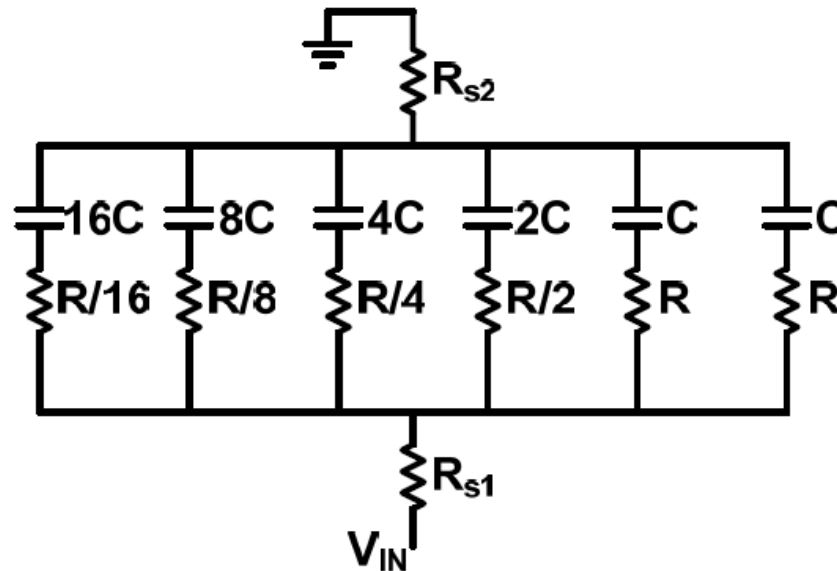
- Commonly used techniques

- Implement "two-stage" or "multi-stage" capacitor network to reduce array size [Yee, JSSC 8/79]
  - Split DAC or C-2C network
- Calibrate capacitor array to obtain precision beyond raw technology matching [Lee, JSSC 12/84]



# SAR ADC Speed Estimation

- Model RC network when  $V_{IN}$  is charged
  - Replace switches with R's
  - Assume switches are sized proportional to capacitors



# SAR ADC Speed Estimation contd.

- Speed limited by RC time constant of capacitor array and switches

$$\tau_{eq} = (R_{s1} + R_{s2} + R/2^N)2^N C$$

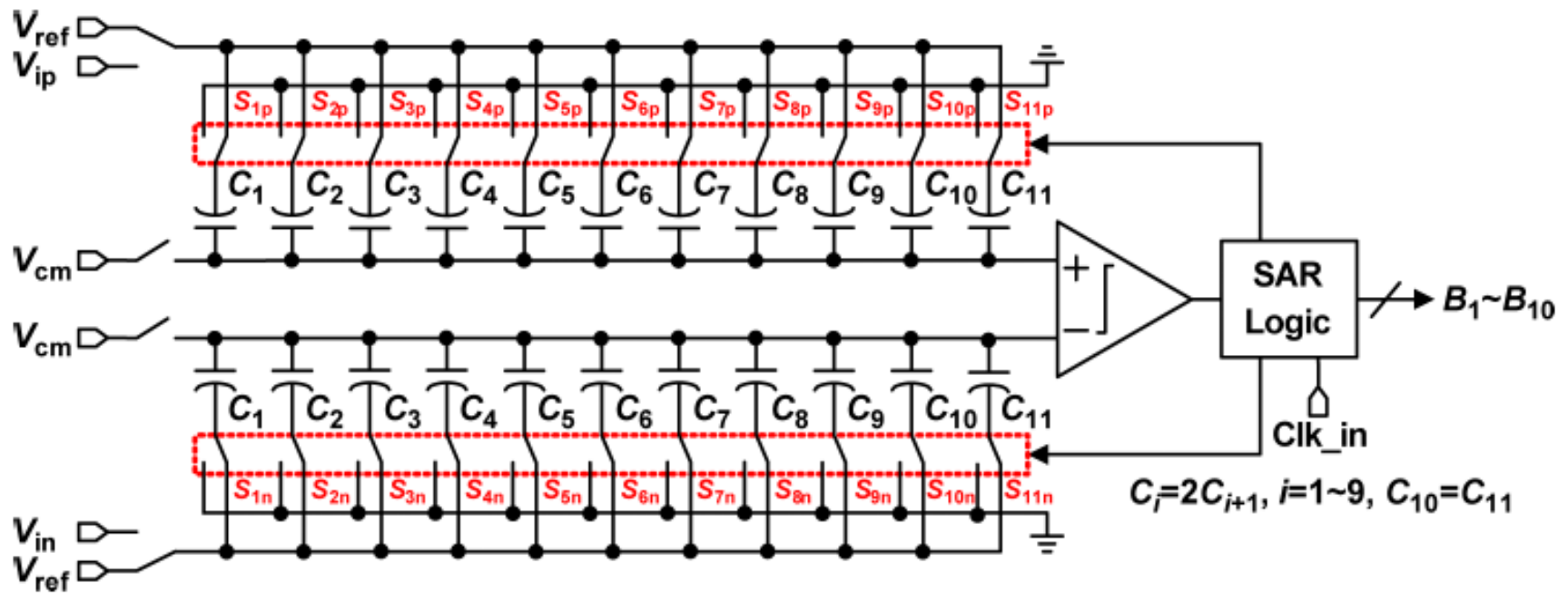
- For better than 0.5 LSB accuracy

$$e^{-T/\tau_{eq}} < \frac{1}{2^{N+1}}$$

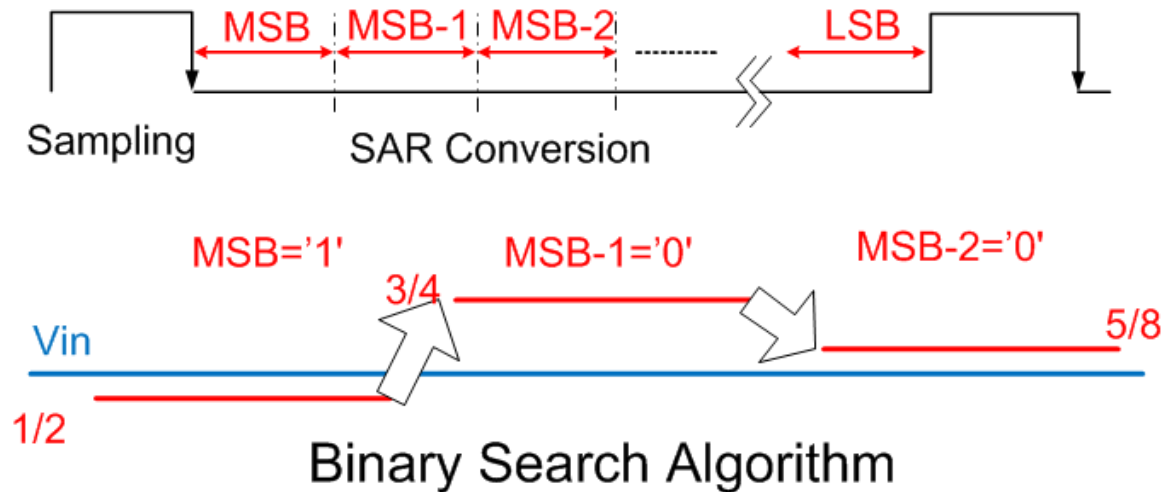
- Sets minimum value for the charging time T

$$T > 0.69(N+1)(R_{s1} + R_{s2} + R/2^N)2^N C$$

# Fully-differential Implementation

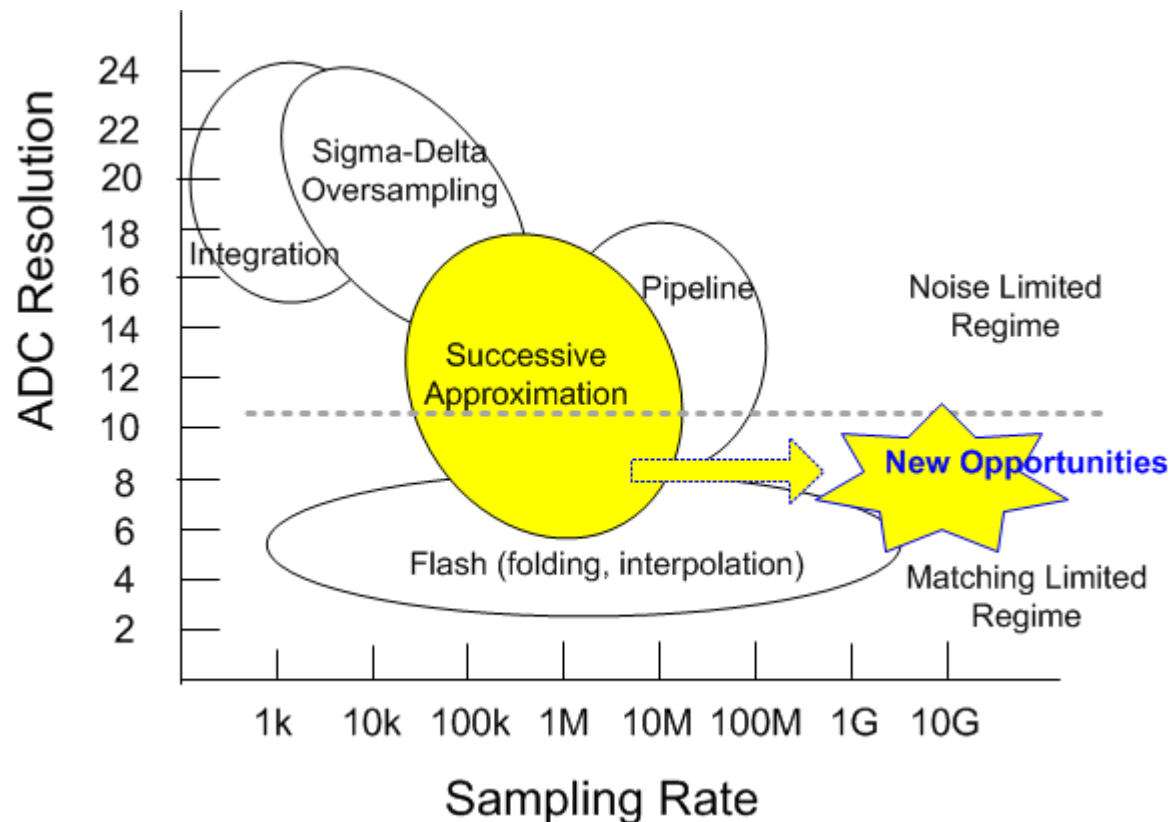


# Recap: Advantages of SAR ADC



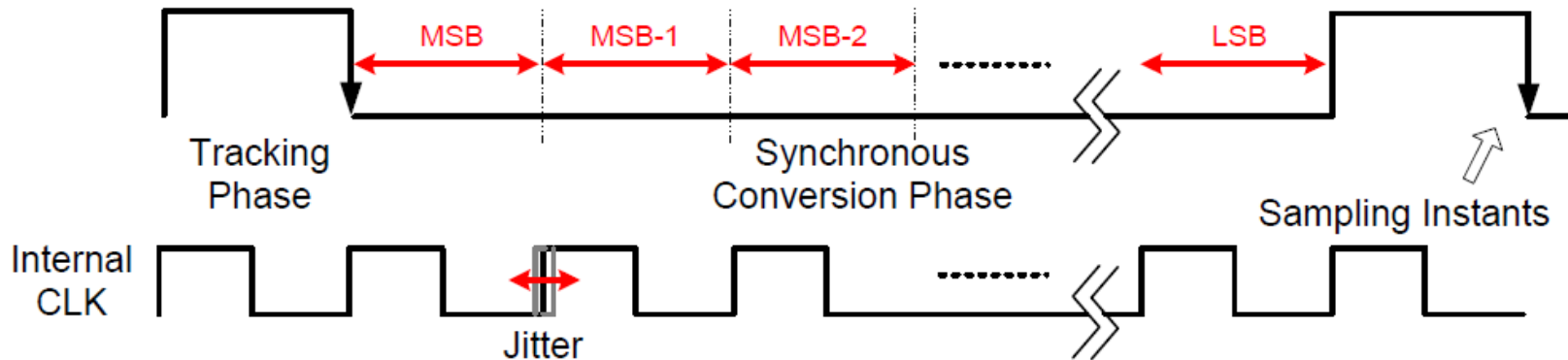
- Mostly digital components
  - good for technology scaling
- No linear, high precision amplification is required
  - fast, low power
- Minimal hardware
  - 1 comparator is needed

# SAR Evolution



- Digital friendly architecture in scaled CMOS has renewed interest in SAR innovation

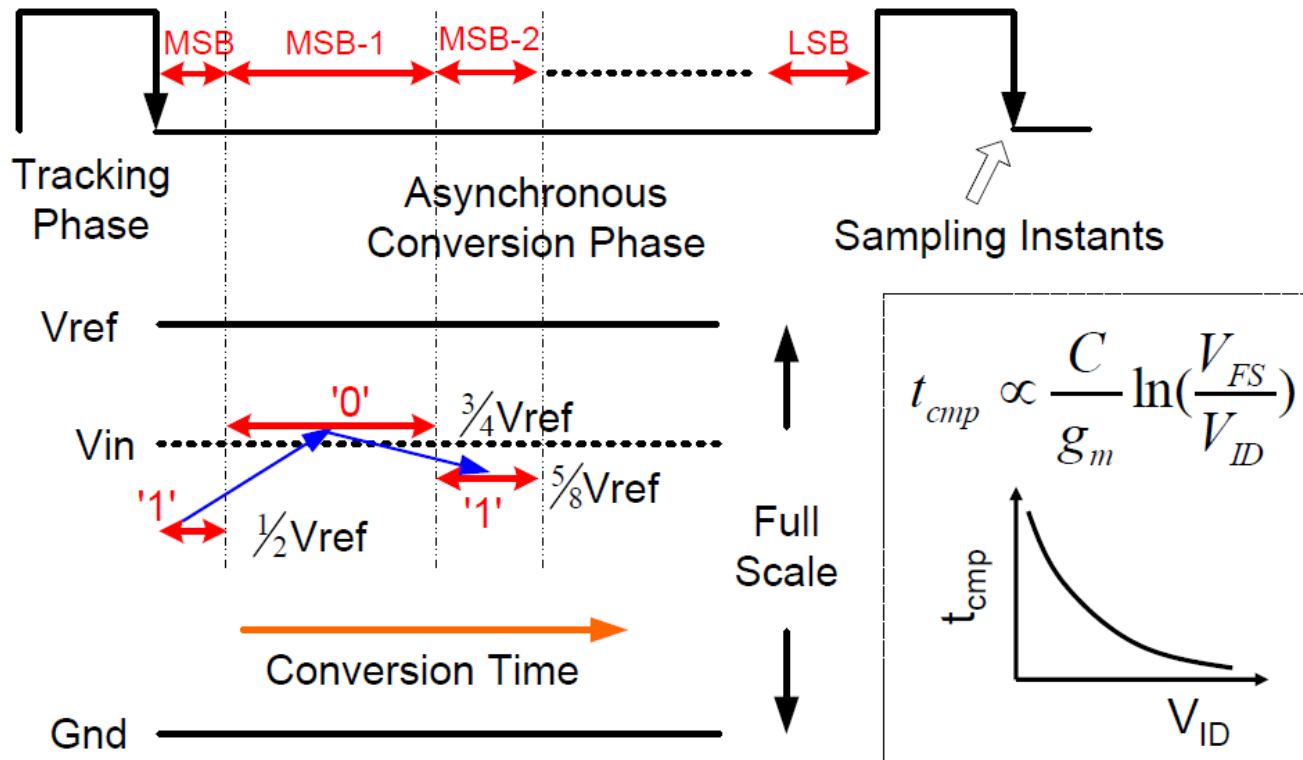
# Limitations of Synchronous SAR



- Cost
  - High-speed internal clock needed ✖
- Speed Limitation
  - Worst-case cycle time ✖
  - Margin for clock jitter ✖



# Asynchronous SAR Concept



- Self-timed Asynchronous comparisons
- Master clock used for synchronizing with the sample rate

M. S.W. Chen, R. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13 $\mu$ m CMOS," ISSCC 06.

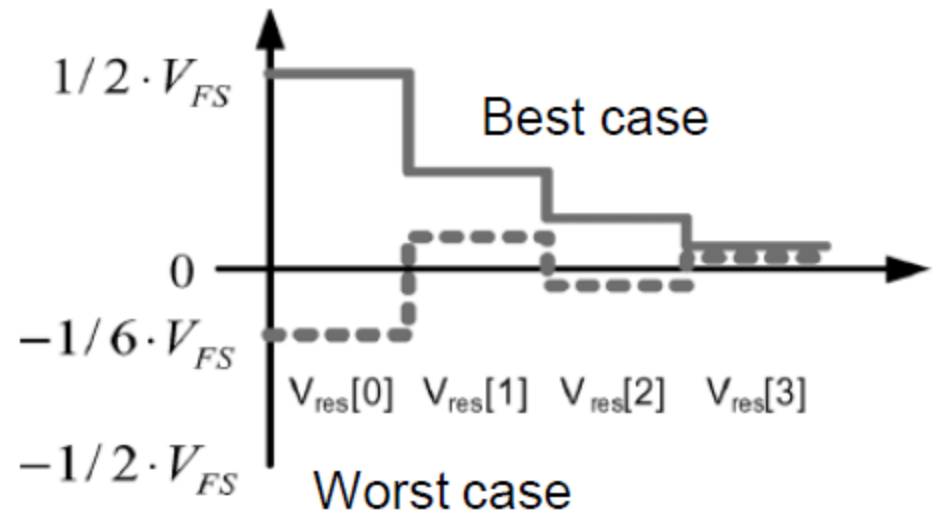
# How much comparison time is saved?

- Conv. time between sync. and async. SAR, assuming regenerative comparator is used.
- It varies with residue voltage profile

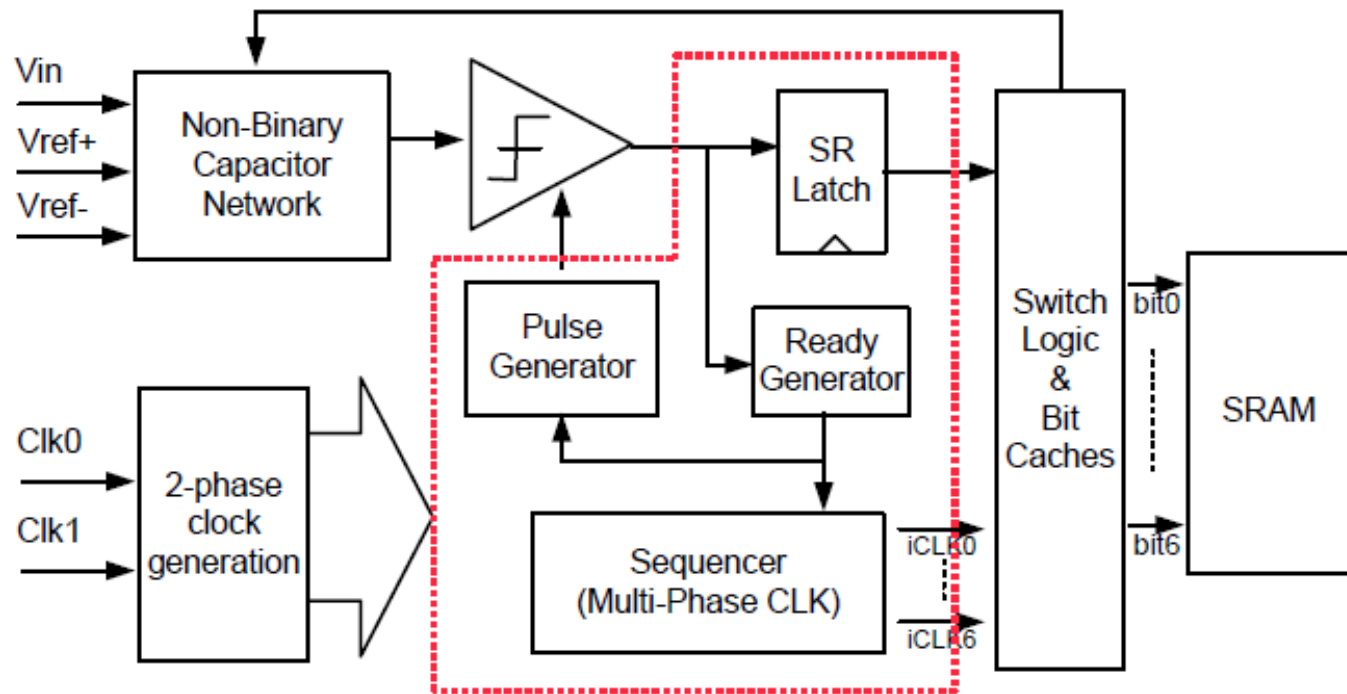
$$T_{\text{cmp}} = \frac{\tau}{A_o - 1} \cdot \ln \frac{V_{\text{FS}}}{V_{\text{res}}} = K \cdot \ln \frac{V_{\text{FS}}}{V_{\text{res}}}$$

$$T_{\text{async}} = \sum_{i=0}^{N-1} K \cdot \ln \frac{V_{\text{FS}}}{V_{\text{res}}[i]}$$

$$T_{\text{sync}} = N \cdot K \cdot \ln \frac{V_{\text{FS}}}{V_{\text{min}}}$$



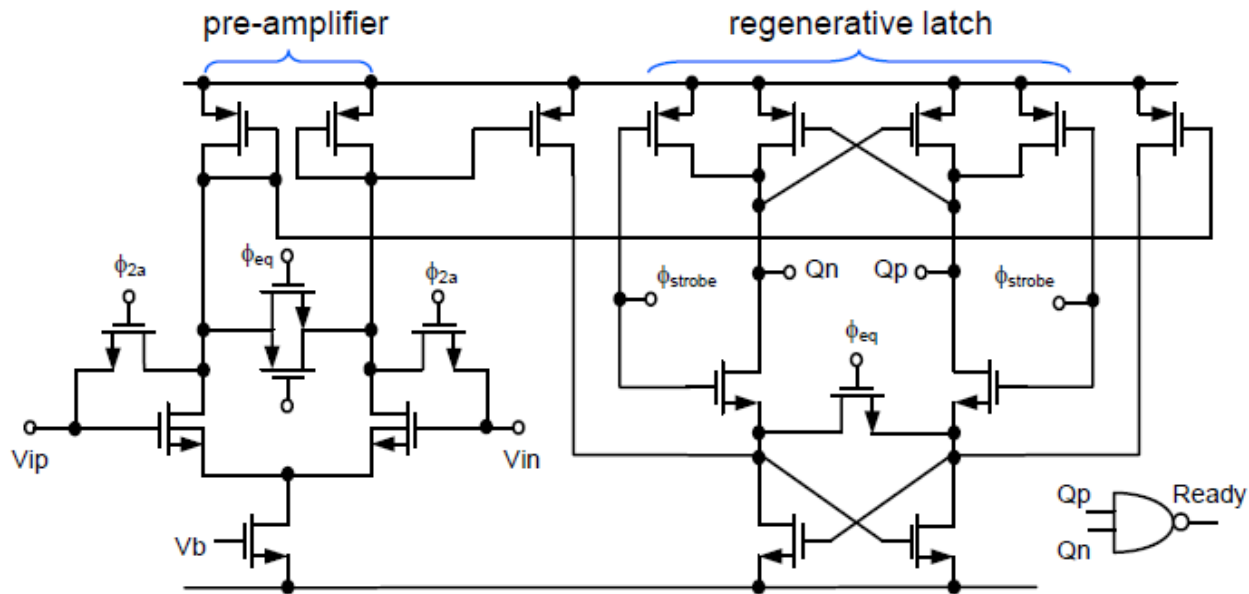
# Asynchronous SAR ADC Concept



Asynchronous digital circuits

*M. S.W. Chen, R. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13 $\mu$ m CMOS," ISSCC 06.*

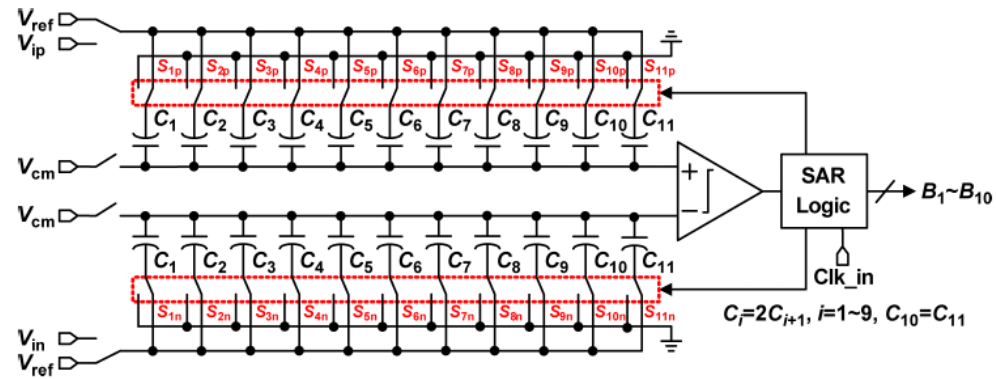
# Asynchronous SAR ADC Concept



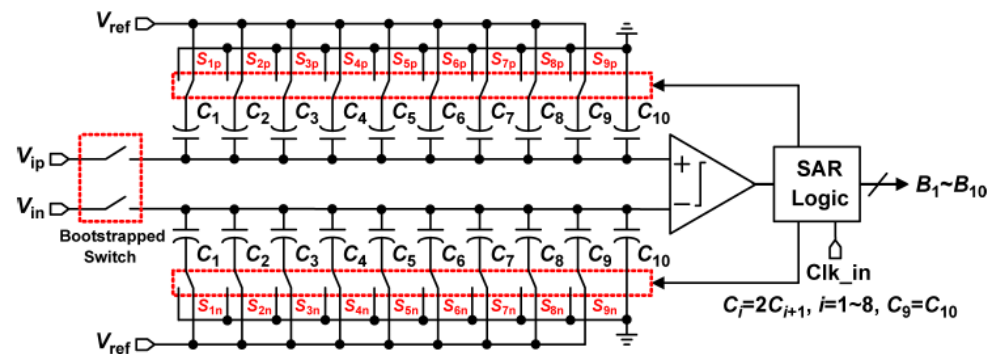
- Dynamic to save power and generate ready signal
- Reset switches for fast recovery
- Ready signal is generated by NAND gate!

# Monotonic Capacitor Switching

- Monotonic switching procedure
  - Input-common mode voltage gradually converges to ground
  - Exploit differential configuration
- Asynchronous comparisons
- Switching energy reduced by 81%



A conventional 10-bit SAR ADC.



The proposed SAR ADC architecture.

## A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure

Chun-Cheng Liu, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*,  
Guan-Ying Huang, *Student Member, IEEE*, and Ying-Zu Lin, *Student Member, IEEE*

# Monotonic Capacitor Switching contd.

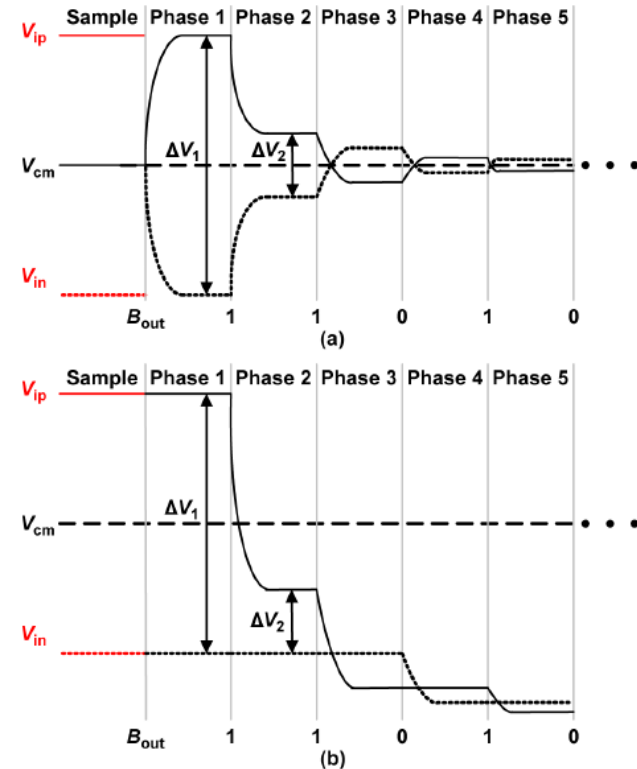
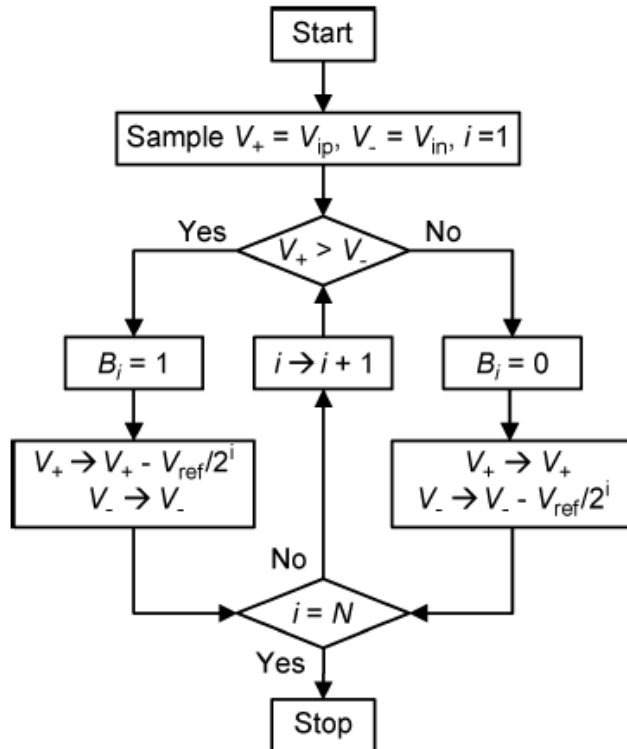


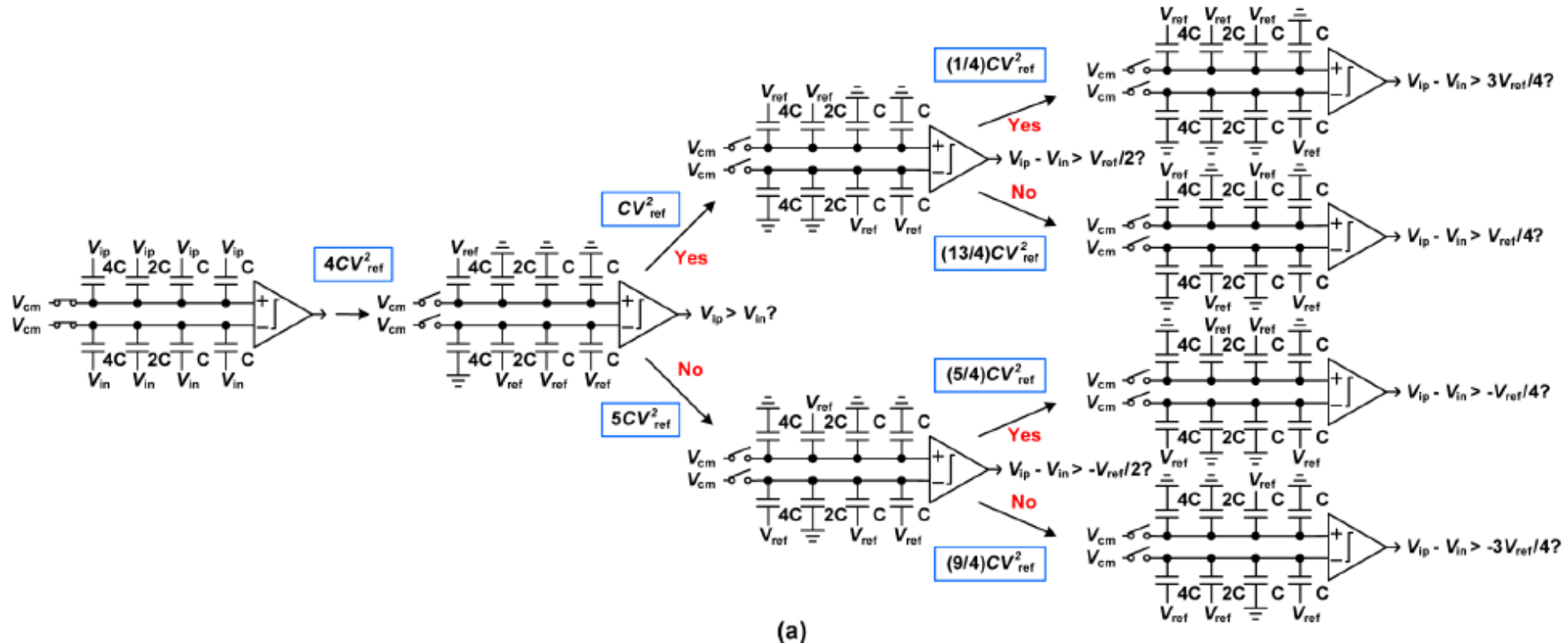
Fig. 4. (a) Waveform of conventional switching procedure. (b) Waveform of monotonic switching procedure.

## A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure

Chun-Cheng Liu, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*,  
Guan-Ying Huang, *Student Member, IEEE*, and Ying-Zu Lin, *Student Member, IEEE*

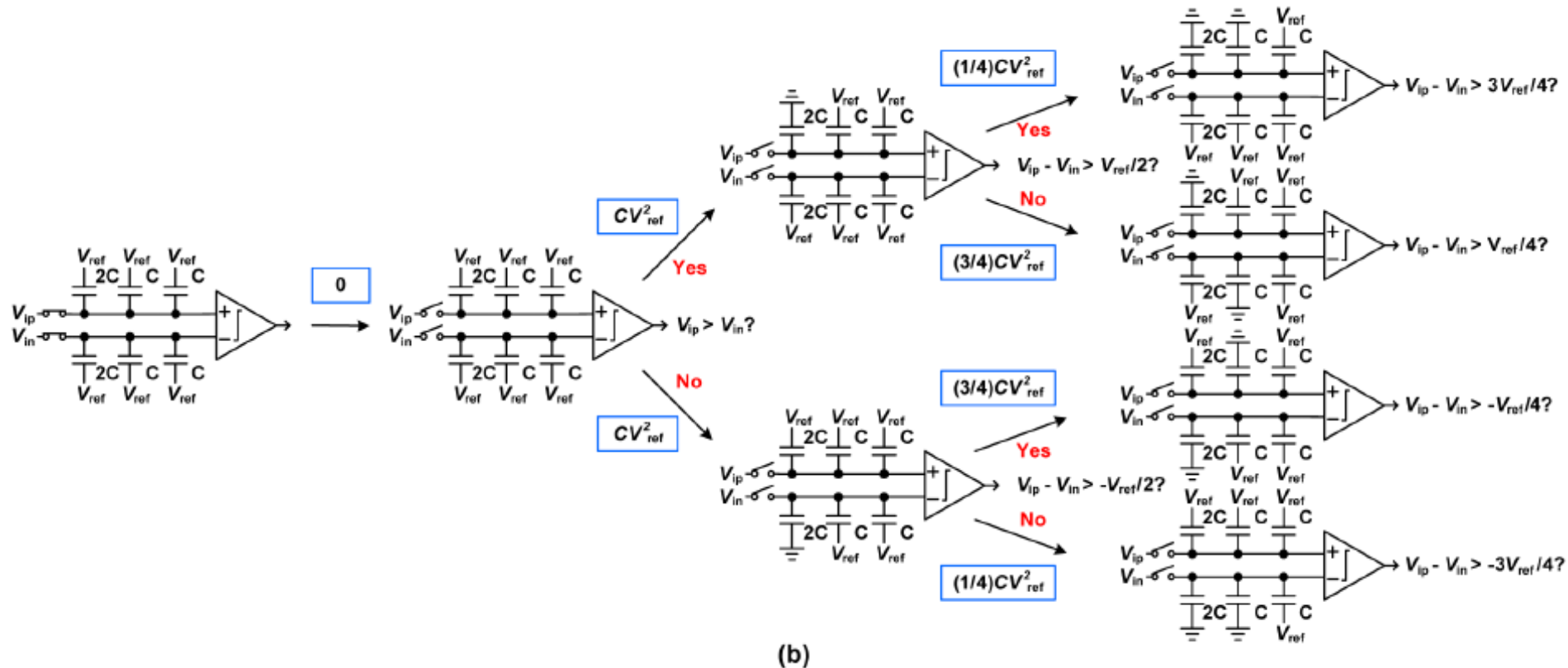
# Monotonic Capacitor Switching contd.

- Conventional switching procedure



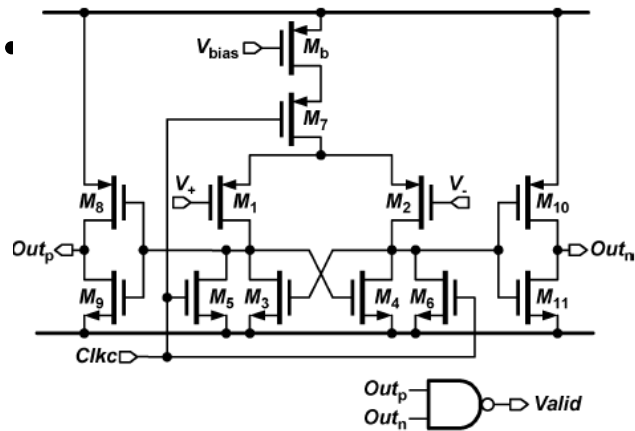
# Monotonic Capacitor Switching contd.

- Monotonic switching procedure

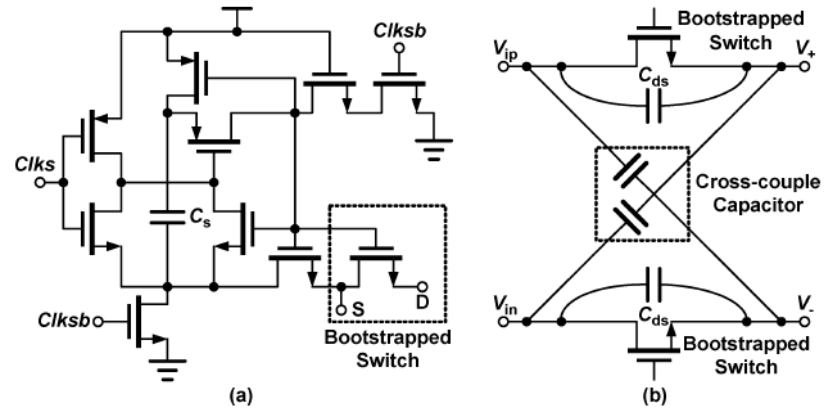




# Monotonic Capacitor Switching contd.



Dynamic comparator with a current source.



(a) Bootstrapped switch. (b) Cross-coupled capacitors.

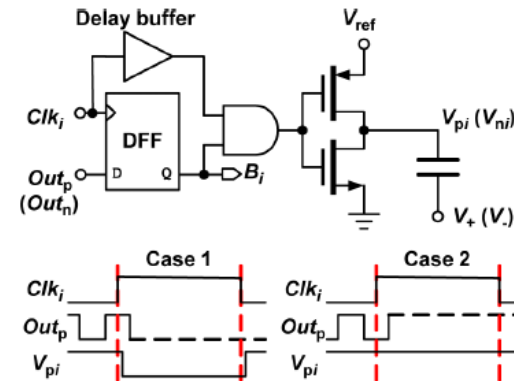
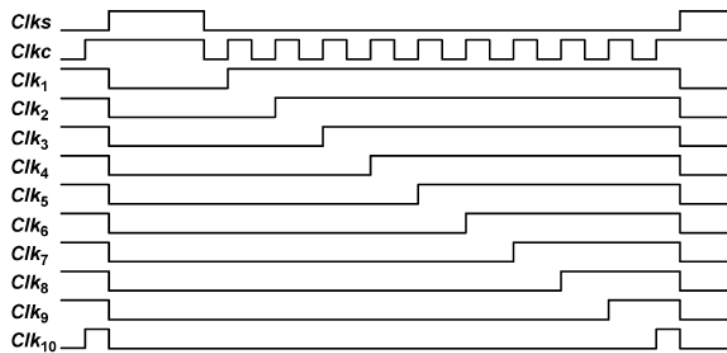
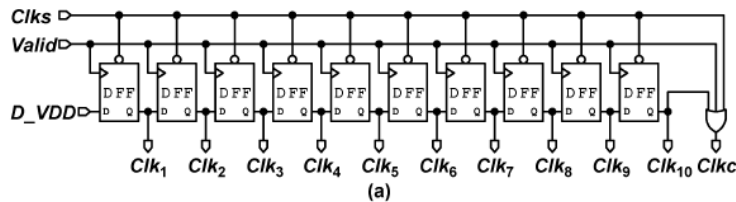


Fig. 10. DAC control logic.



# Loop-unrolled SAR ADC contd.

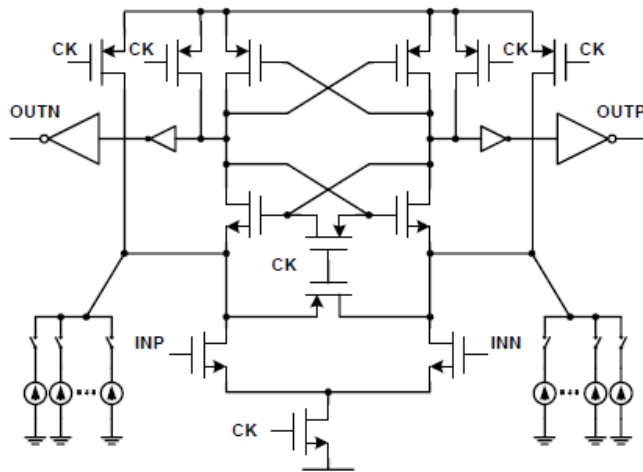


Fig. 4. Comparator design with current steering offset cancellation circuit

- High speed comparator
- IDAC for offset cancellation
- Metastability detection

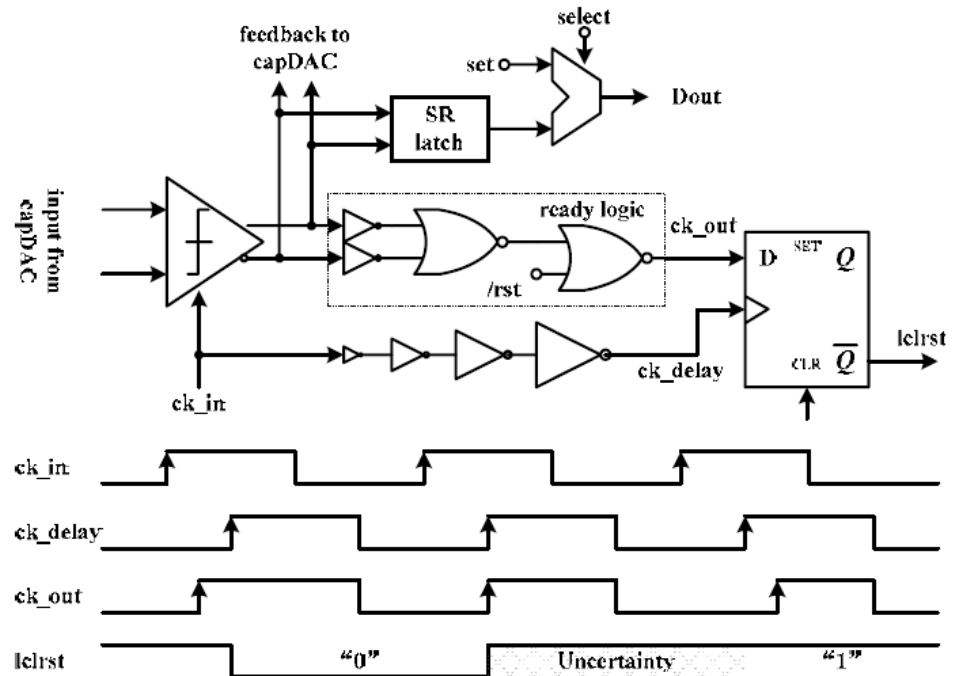


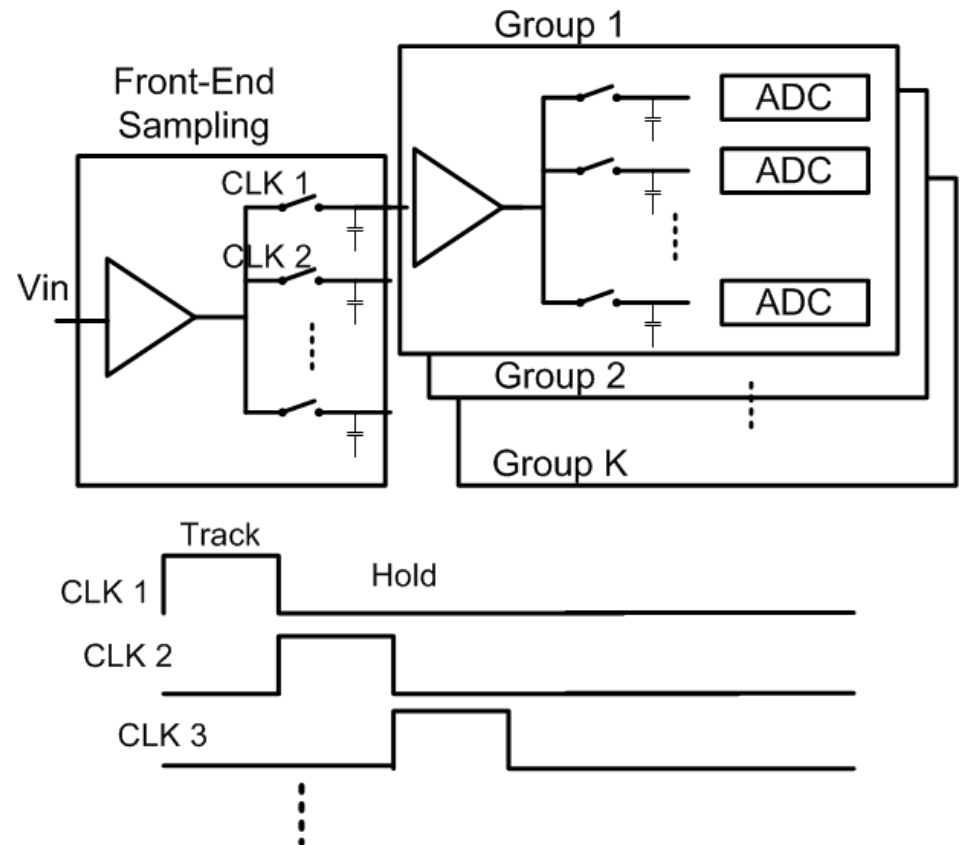
Fig. 6. Metastability detection circuit and its working process.

# Single-Channel, 1.25-GS/s, 6-bit, Loop-Unrolled Asynchronous SAR-ADC in 40nm-CMOS

Tao Jiang<sup>1</sup>, Wing Liu<sup>2</sup>, Freeman Y. Zhong<sup>2</sup>, Charlie Zhong<sup>2</sup>, Patrick Y. Chiang<sup>1</sup>

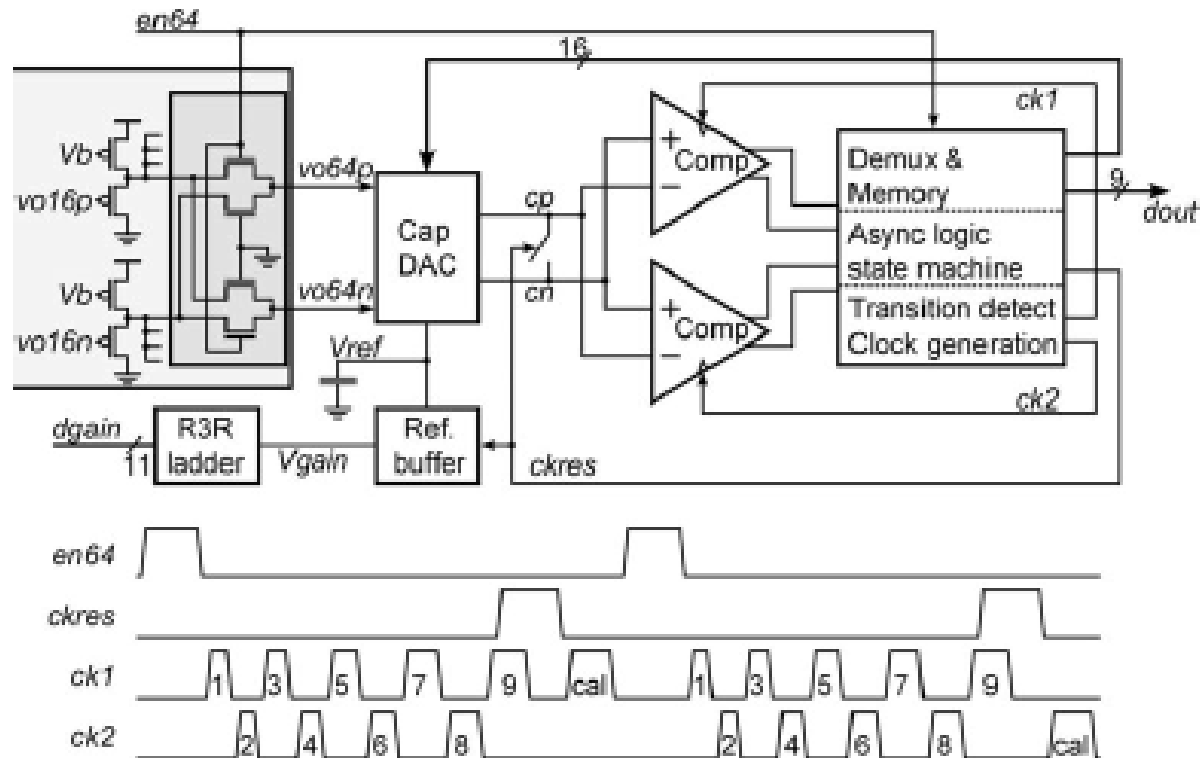
# Time Interleaving

- Sampling rate scale proportionally to the number of interleaved channels
- Calibration is required for inter-channel mismatch
- Relaxed clock distribution
- For example:
  - 8bit 56GS/s
  - 320 of 175MS/s SAR (Fujitsu)



# 90GS/s 8bit with 64x Time Interleave

- Two comparators 'ping-pong' in two consecutive conversions implemented in 32nm SOI



L. Kull, et al., "A 90GS/s 8b 667mW 64x Interleaved SAR ADC in 32nm Digital SOI CMOS," ISSCC 14.

# References

1. Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters," 2<sup>nd</sup> Ed., Springer, 2005..
2. Y. Chiu, *Data Converters Lecture Slides*, UT Dallas 2012.
3. B. Boser, *Analog-Digital Interface Circuits Lecture Slides*, UC Berkeley 2011.