HW 3

ECE 4/517– Mixed Signal IC Design

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the ENGR-410 server for the homework problems.
2. Use 180nm CMOS models with a supply voltage of $V_{DD} = 1.8V$.

Problem 1. Latch design: Consider the latch circuits shown in Fig. 1. The first latch on the left was discussed in the class. Another latch, called the StrongARM latch is shown towards the right. The latter has the advantage of simplified clocking. In both the latches, L is the latch signal, while $\overline{L}$ is its complement. Use an ideal clock generators (V_{source} in Cadence) to realize the various phases for simplicity. The input is fully-differential with a common-mode voltage, $V_{CM} = 0.9V$. The clock frequency is 10 MHz. Use minimum size for all transistors. Choose appropriate implementations for the switches.

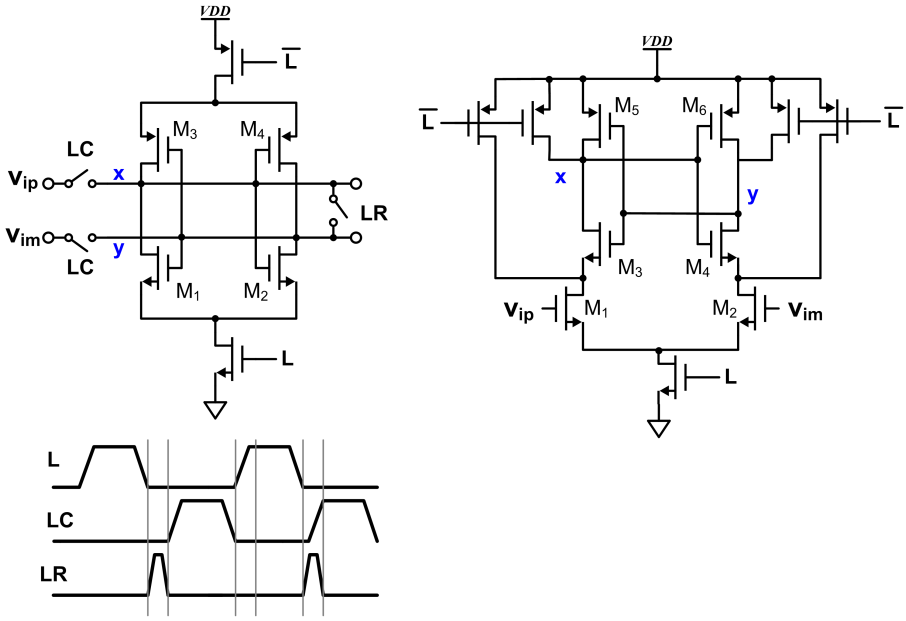

Figure 1: Latch circuits for Problem 1.

1. Determine dynamic offset using the following procedure: the differential input is to be made a slow ramp, increasing at 2mV every clock period, starting from $-V_{DD}/5$ and gradually increased to $V_{DD}/5$. We hope that the offset will lie within this range. The "threshold" of the latch (ideally zero) can be found to within 2mV by observing when the regenerated output flips sign. Take care of the following during simulation - choose the time step of the simulation

to be sufficiently small so that the waveforms during regeneration do not change appreciably. Which of the two latches has more dynamic offset ? Why ?

2. Simulate and show latch operation (for both the designs) for differential inputs. In your report, draw the circuit diagrams with all device sizes marked. Also on one graph, plot the waveforms of all latch nodes in that clock period where the latch flips sign.

3. Deliberately add a capacitance of 0.5 fF at the drain of M_1 only, and repeat part (a). What do you notice? Explain the observations?

Problem 2 Comparator design: This problem discusses switched capacitor based reference subtraction, as discussed in class. This is accomplished through the capacitor C_1

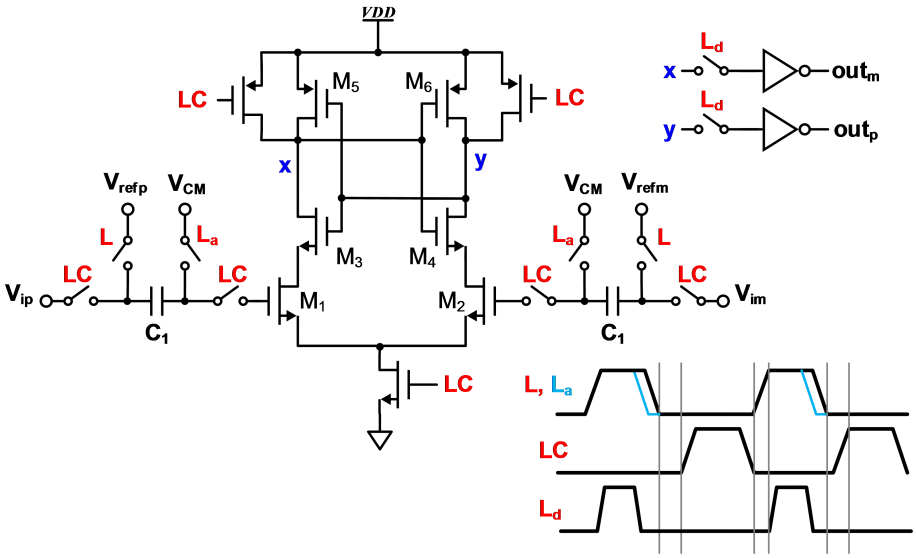

Figure 2: Comparator circuit for Problem 2.

1. Simulate the circuit, show the plots and explain how it works. The clock frequency is 10 MHz. *Alter the clock phases accordingly.*

2. What is the capacitance looking in from the input when LC is high? How will you choose a value for C_1.

Save this design as this will be useful for the project.