Project 2

ECE 5/417 – Mixed Signal IC Design

1 Problem Statement

Design of a SAR ADC: Design a SAR ADC with the specifications listed below. The design is to be implemented using a 180-nm mixed-mode CMOS process with a $V_{DD} = 1.8\,V$ supply voltage.

Table 1: SAR ADC design specifications.

Parameter	Specified Value
Supply voltage, V_{DD}	1.8 V
Sample rate (f_s)	≥10 MHz
Resolution	8 bits
Input Range (fully-differential)	3 $V_{pp,diff}$
$FoM = \frac{Power}{f_s \cdot 2^{ENOB}}$	Minimum

2 Design Details

The design will use differential inputs and hence should employ *fully-differential* circuits. You may assume a common-mode voltage (V_{CM}) of 0.9V. The following steps will guide you through the design and documentation process.

1. **Architecture:** You may consider various architectures discussed in the class: (i) synchronous *vs* asynchronous, (ii) Bottom-plate (traditional) sampling vs top-plate (monotonic switching) sampling. ECE 417 students can implement the simplest architecture. However, graduate (ECE 517) students should demonstrate creative solutions. Generate clocks using ideal components but ensure that the clock edges are realistic (not too sharp or slacking).

2. **Charge Redistribution DAC:**

   (a) Optimize the size of unit capacitor C based on kT/C noise, mismatch, and other relevant considerations.

   (b) Choose a suitable switch sizes based on RC delays, and switching scheme to optimize CV^2 power. You will need a linear switch if using top-plate sampling (see references from class slides).

3. **Comparator:**

   (a) Design comparator based on the offset you can tolerate for the SAR ADC. Use mismatch data for 180-nm CMOS from [1]. You must simulate your comparator in isolation to ensure functionality. Also, note that the comparator design becomes more stringent in the top-plate sampling case.

4. **Digital Logic:** You can use ideal digital circuit blocks to implement the SAR register and logic.

5. **Simulations:**

   (a) Show the spectrum of the ADC output for a full-scale sinewave at about $f_s/2$. What is the SQNR (in dB)? One way of doing this is to print the four ADC output bits into a file, read the file into MATLAB, convert from binary to decimal, and do the FFT in MATLAB. Another way of doing this is to use an ideal 8-bit DAC at the output of the ADC and run an FFT on the DAC output in Spectre.

   (b) Characterize dynamic (SNDR, dynamic range, SFDR, etc.) and static performance (DNL and INL) of the ADC. Estimate the $FoM = \frac{Power}{f_s \cdot 2^{ENOB}}$ and compare with the state-of-the-art with the survey in [1]. You many not see much deviation from ideal design, due to the absence of mismatch and parasitic extraction from layout, but its instructive that you create scripts to estimate these.

3 Project Report

Submit your neatly typed report in a two-column IEEE transactions format [3], in not more than 5 pages. Show neatly drawn schematics and block diagrams. You may download the Visio schematic symbols from the course website [4]. Provide relevant references in your report. Show the modulator overall ADC performance (peak SNR/SNDR, dynamic range, DNL/INL, and the FoM) in a neatly tabulated manner along with the conclusion.

4 Grading Scheme

Design choices and justification 25%

Functionality and performance 30%

Design characterization and presentation of results 25%

Design Novelty/Creativity 10%

Report presentation and references 10%

References

[1] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," IEEE Journal of Solid-State Circuits, vol. 40, no. 6, pp. 1212-1224, 2005.

[2] B. Murmann, "ADC Performance Survey 1997-2016," Available [Online].

[3] IEEE Transactions Templates. Available [Online].

[4] Visio Schematic Symbols. Available [Online].