Project 1

ECE 5/417 – Mixed Signal IC Design

1 Problem Statement

Design of a Flash ADC: Design a Flash ADC with the specifications listed below. The design is to be implemented using a 180-nm mixed-mode CMOS process with a $V_{DD} = 1.8\,V$ supply voltage, such that the figure of merit (FoM) is minimized..

Table 1: Flash ADC design specifications.

Parameter	Specified Value
Supply voltage, V_{DD}	1.8 V
Sample rate (f_s)	10 MHz
Resolution	4 bits
Input Range (fully-differential)	3 $V_{pp,diff}$
$FoM = \frac{Power}{f_s \cdot 2^{ENOB}}$	Minimum

2 Design Details

The design will use differential inputs and hence should employ fully-differential circuits. You may assume a common-mode voltage (V_{CM}) of 0.9V. You can use two ideal voltage sources of $V_{refp} = 1.65V$ and $V_{refm} = 0.15V$ for operating the resistor ladder. The following steps will guide you through the design and documentation process.

1. **Schematic Design:** Needless to say, use array functionality in Cadence Virtuoso to design your schematics as much as possible. This is a good design practice. Generate clocks using ideal components but ensure that the clock edges are realistic (not too sharp or slacking).

2. **Reference Ladder:**

   (a) Use the two ideal sources to generate other reference voltages using a resistor ladder. How will you choose the value of the ladder resistors?

   (b) Depending upon the kickback noise from the comparators, you may need to add bypass capacitors to the reference tap points on the ladder. What are the tradeoffs between decoupling and recovery from kickback noise when using large size of decouplng capacitors?

3. **Comparators:**

   (a) Estimate latch and pre-amp sizing based on the offset you can tolerate. Use mismatch data for 180-nm CMOS from [2]and apply as in the take-home midterm and class lectures. You must simulate your comparator in isolation to ensure functionality.

   (b) You have several approaches for reference subtraction in differential Flash-ADC. Discuss the technique that you used and show its operation using simulations.

4. **Digital Back-end:** You can use ideal digital circuit blocks to implement the backend logic for thermometer to binary conversion with single-bit bubble error correction.

5. **Simulations:**

   (a) Show the spectrum of the ADC output for a full-scale sinewave at about $f_s/2$. What is the SQNR (in dB)? One way of doing this is to print the four ADC output bits into a file, read the file into MATLAB, convert from binary to decimal, and do the FFT in MATLAB. Another way of doing this is to use an ideal 4-bit DAC at the output of the ADC and run an FFT on the DAC output in Spectre.

   (b) Estimate power consumption ($Power = V_{DD} * I_{DD}$) in your ADC by measuring average current (I_{DD}) pulled from supply in the simulation. Use realistic conditions for simulation.

   (c) Characterize dynamic (SNDR, dynamic range, SFDR, etc.) and static performance (DNL and INL) of the ADC. Estimate the $FoM = \frac{Power}{f_s \cdot 2^{ENOB}}$ and compare with the state-of-the-art with the survey in [2]. You many not see much deviation from ideal design, due to the absence of mismatch and parasitic extraction from layout, but its instructive that you create scripts to estimate these.

3 Project Report

Submit your neatly typed report in a two-column IEEE transactions format [3], in not more than 5 pages. Show neatly drawn schematics and block diagrams. You may download the Visio schematic symbols from the course website [4]. Provide relevant references in your report. Show the modulator overall ADC performance (peak SNR/SNDR, dynamic range, DNL/INL, and the FoM) in a neatly tabulated manner along with the conclusion.

4 Grading Scheme

Design choices and justification 25%

Functionality and performance 30%

Design characterization and presentation of results 25%

Design Novelty/Creativity 10%

Report presentation and references 10%

References

[1] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," IEEE Journal of Solid-State Circuits, vol. 40, no. 6, pp. 1212-1224, 2005.

[2] B. Murmann, "ADC Performance Survey 1997-2016," Available [Online].

[3] IEEE Transactions Templates. Available [Online].

[4] Visio Schematic Symbols. Available [Online].