CMOS COMPARATORS

University of Idaho
College of Engineering

COMPARATOR DESIGN CONSIDERATIONS

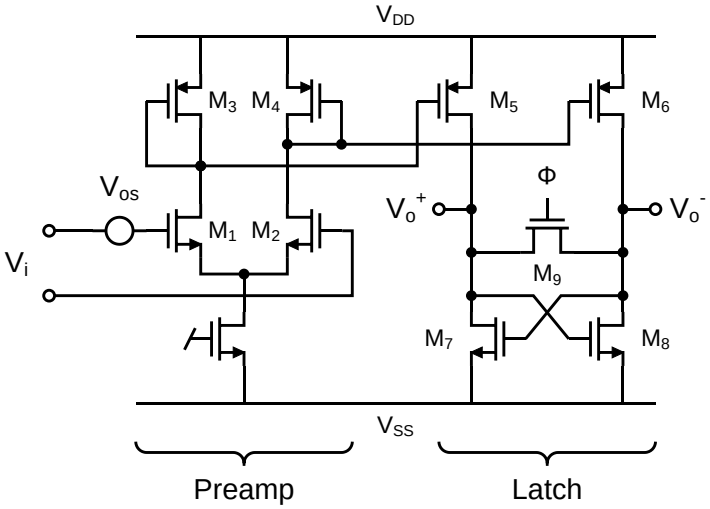
Comparator =

- Preamp (optional in some cases)
- + Reference Subtraction (optional for single-bit case)
- + Regenerative Latch

Design Considerations

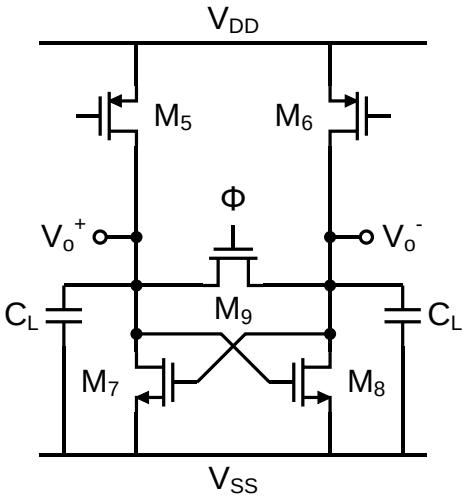
- Accuracy (dynamic and static offset, noise, resolution)
- Settling time (tracking BW, regeneration speed)
- Sensitivity/resolution (gain)
- Metastability (ability to make correct decisions)
- Overdrive recovery (memory)
- Power consumption

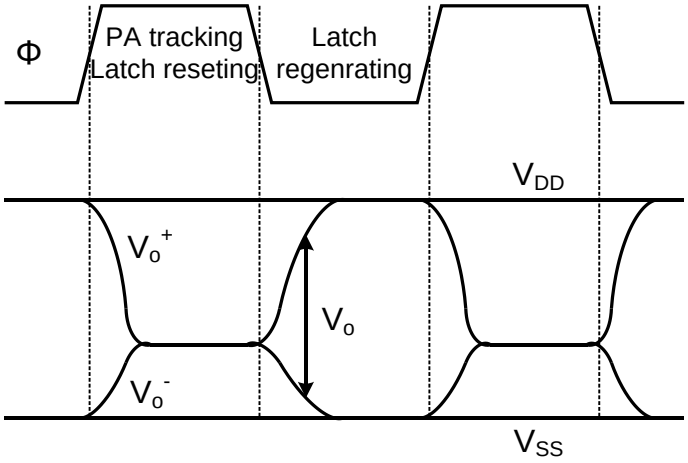
EXAMPLE CMOS COMPARATOR



- Several Preamp and latch topologies are possible
- Input-referred offset V_{os} introduced due to:
  - Preamp input pair mismatch
  - PMOS loads and current mirror
  - Latch offset
  - Charge-Injection mismatch in the reset switch
  - Clock feed-through imbalance of the reset switch
  - Clock routing
  - Parasitic mismatch

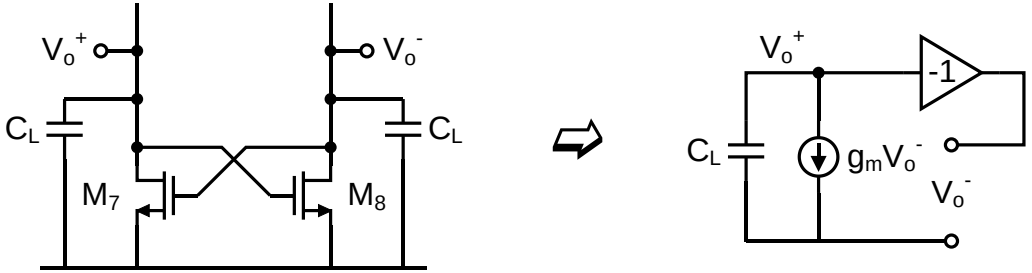
LATCH REGENERATION





- Exponential regeneration due to positive feedback of cross-coupled pair M_7 and M_8

REGENERATION SPEED – LINEAR MODEL

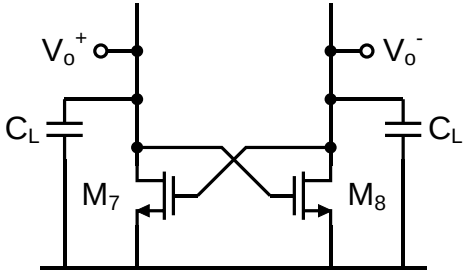


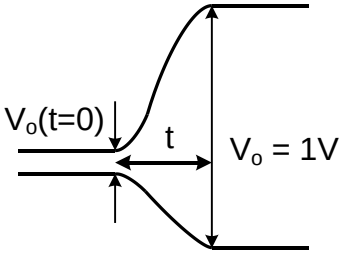
$$\begin{cases} V_o^+ = -V_o^- \\ V_o^+ = -g_m \cdot V_o^-/sC_L \end{cases} \Rightarrow \begin{pmatrix} 1 & 1 \\ 1 & g_m/sC_L \end{pmatrix} \begin{pmatrix} V_o^+ \\ V_o^- \end{pmatrix} = 0$$

$$\Delta(s) = g_m/sC_L - 1 = 0 \quad \Rightarrow \quad s_p = g_m/C_L, \quad \text{single RHP pole}$$

$$V_{out}(t) = V_o \cdot \exp(t \cdot g_m / C_L)$$

REG. SPEED – LINEAR MODEL

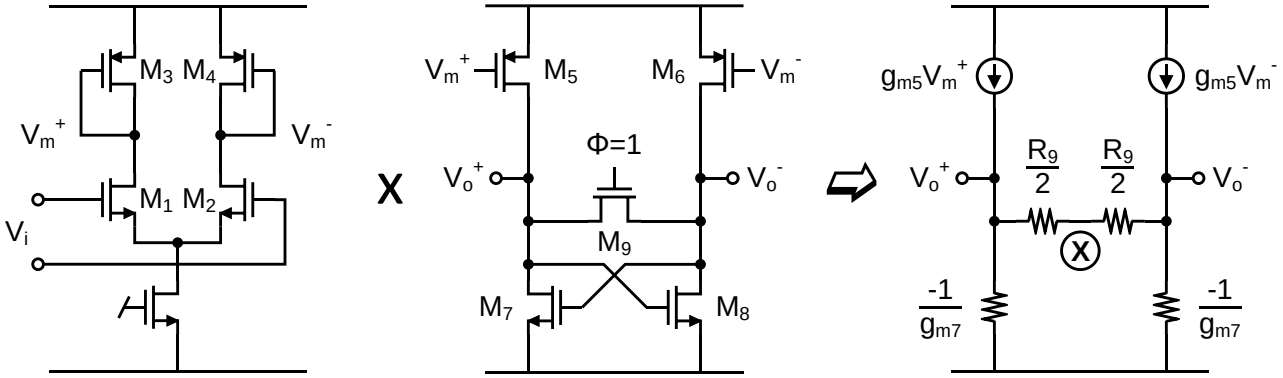




V_o	$V_o(t=0)$	$t/(C_L/g_m)$
1V	100mV	2.3
1V	10mV	4.6
1V	1mV	6.9
1V	100μV	9.2

$$t = \frac{C_L}{g_m} \cdot \ln\left[\frac{V_o(t)}{V_o(0)}\right]$$

REG. SPEED – LINEAR MODEL

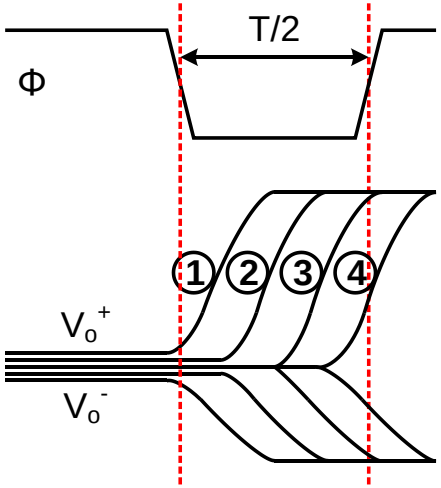


$$|A_{V1}| = \frac{g_{m1}}{g_{m3}} \qquad |A_{V2}| = \frac{g_{m5}R_9}{2 - g_{m7}R_9}, \quad \frac{R_9}{2} < \frac{1}{g_{m7}} \text{ to be amplifier.}$$

$$V_o(0) = V_i(0) \cdot A_V = V_i(0) \cdot A_{V1}A_{V2}$$

$$V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

COMPARATOR METASTABILITY

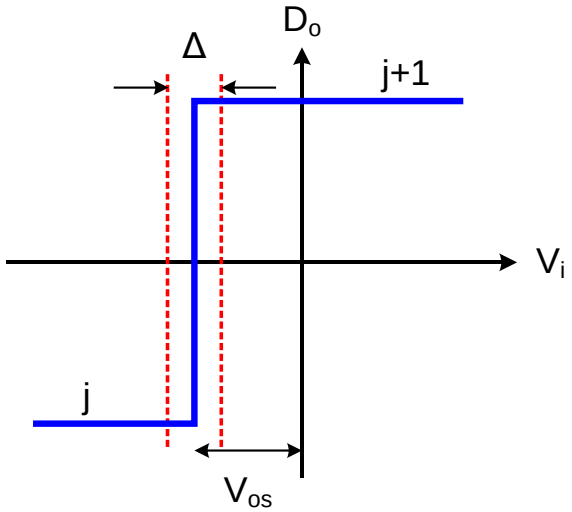


$$V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

Curve	$A_{V1}A_{V2}$	$V_i(t=0)$
①	10	10 mV
②	10	1 mV
③	10	100 μV
④	10	10 μV

- Settling time is dependent upon initial signal and regenerative gain
- When input is sufficiently close to the comparator threshold
  - Comparator fails to produce valid logic outputs within T/2
  - Sets the comparator resolution (Δ)

COMPARATOR METASTABILITY



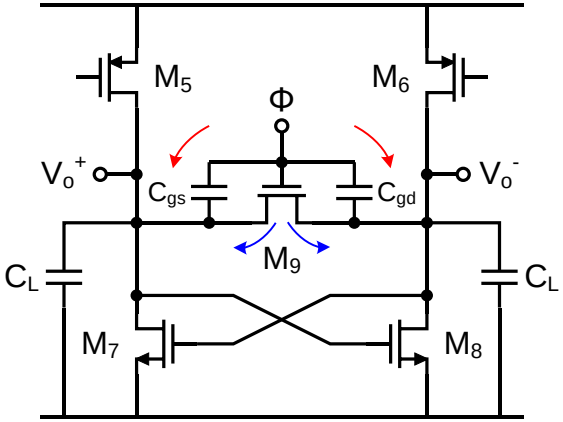
Assuming that the input is uniformly distributed over V_{FS}, then

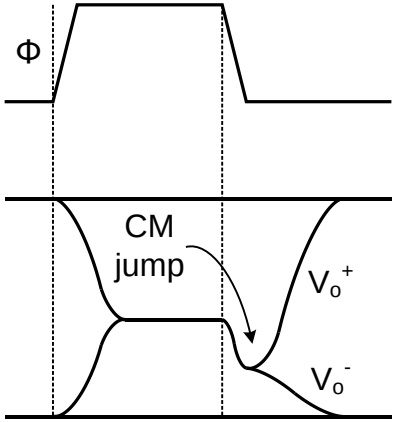
$$BER = \frac{\Delta}{1LSB}$$

$$V_o(t) = V_i(0) \cdot A_{V1}A_{V2} \cdot \exp(t \cdot g_m/C_L)$$

- Cascade pre-amp stages for larger gain
- Pipelined multi-stage latches (with increased latency)
  - pre-amp can be pipelined too

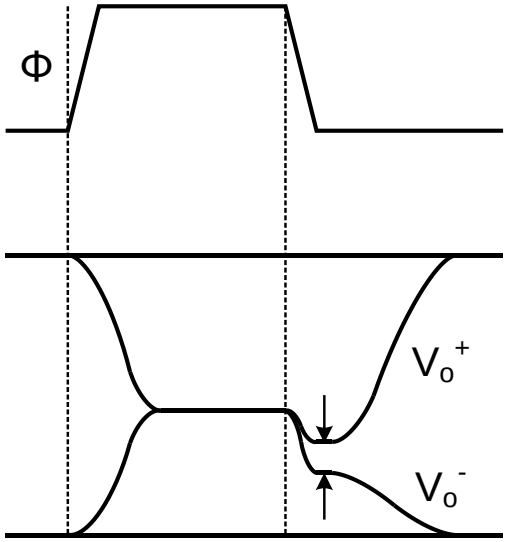
CHARGE-INJECTION AND CLOCK-FEEDTHROUGH IN LATCH





- In the above latch, regeneration starts when Φ goes low
  - Charge injection (CI) and clock-feedthrough (CF) introduce common-mode jump into V_o^+ and V_o^-
  - Mismatch/imbalance in CI and/or CF induces dynamic offset in the latch

DYNAMIC AND STATIC OFFSETS IN A LATCH



Dynamic offset induced due to:

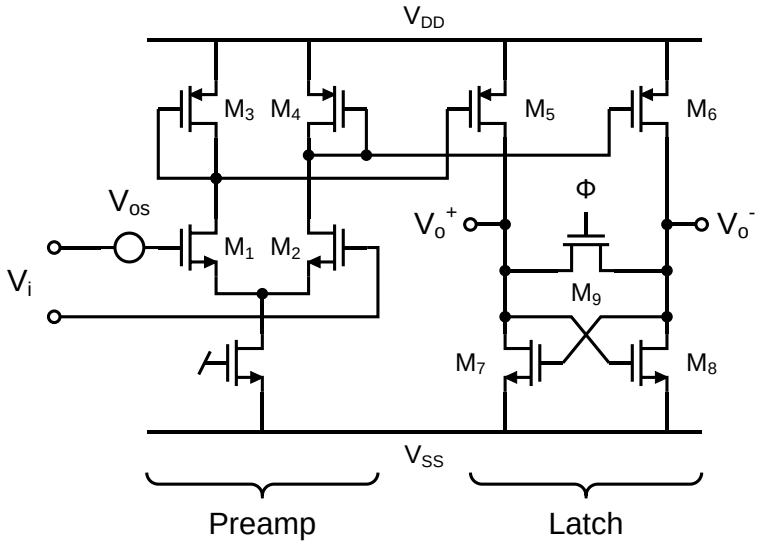
- Imbalanced CI and CF
- Imbalanced load capacitance

$$\left.\begin{array}{l}\text{0.5V CM jump}\\ \text{10\% imbalance}\end{array}\right\} \Rightarrow \text{50mV offset}$$

Static offset induced due to:

- Mismatch in the cross-coupled pairs
- Mismatch in the signal input circuitry

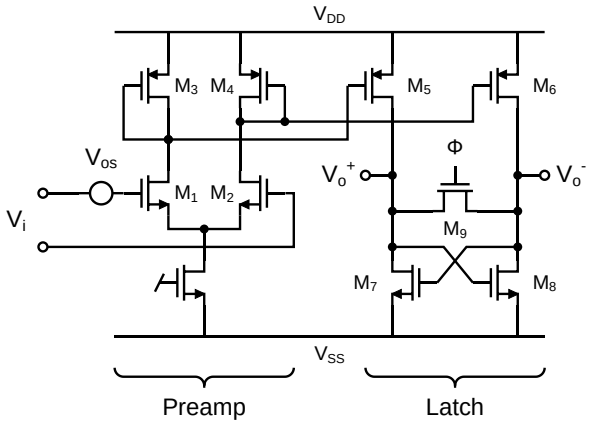
CMOS COMPARATOR



- Input-referred latch offset gets divided by the gain of the preamp
- Preamp introduces its own offset (mostly static due to V_{th}, W, and L mismatches)
- Preamp also reduces kickback noise

- Rapidly varying regeneration nodes couple kickback noise to the input
- Kickback noise disturbs reference voltages, must settle before next sample

COMPARATOR OFFSET



Differential pair mismatch:

$$V_{os}^{\ 2} = (\Delta V_{th})^2 + \frac{1}{4} V_{ov}^{\ 2} \left(\frac{\Delta \frac{W}{L}}{\frac{W}{L}} \right)^2$$

$$|A_{V1}| = \frac{g_{m1}}{g_{m3}} \qquad |A_{V2}| = \frac{g_{m5} R_9}{2 - g_{m7} R_9}$$

Total input-referred comparator offset:

$$V_{os}^{\ 2} = V_{os,12}^{\ 2} + \frac{V_{os,34}^{\ 2} + V_{os,56}^{\ 2}}{A_{V1}^{\ 2}} + \frac{V_{os,78}^{\ 2}}{A_{V1}^{\ 2} A_{V2}^{\ 2}} + \frac{V_{os,dyn}^{\ 2}}{A_{V1}^{\ 2} A_{V2}^{\ 2}}$$

REVIEW: TRANSISTOR MATCHING

Suppose parameter P of two rectangular devices has a mismatch error of ΔP. The variance of parameter ΔP b/t the two devices is

$$\sigma^2(\Delta P) = \frac{A_P^{\,2}}{WL} + S_P^{\,2} D^2,$$

1st term dominates for small devices

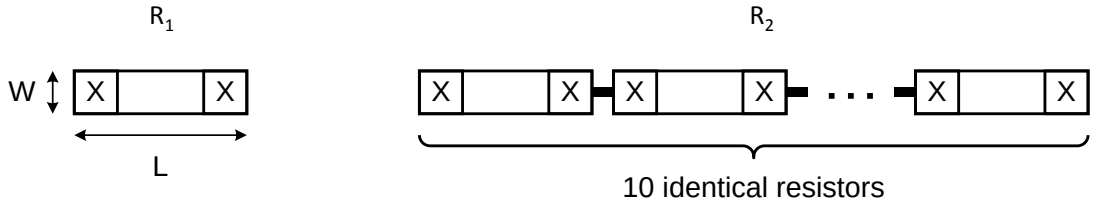
where, W and L are the effective width and length, D is the distance

$$\text{Threshold}: \ \sigma^2(V_{th}) = \frac{A_{Vth}^{\,2}}{WL} + S_{Vth}^{\,2} D^2$$

$$\text{Current factor}: \ \frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^{\,2}}{WL} + S_\beta^{\,2} D^2$$

Ref: M. J. M. Pelgrom, et al., "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 1433-1439, issue 5, 1989.

RECALL: DEVICE SIZING FOR MISMATCH



$$R_1 = R_S \cdot \frac{L}{W} \text{ with std } \sigma_{R1} \qquad R_2 = R_S \cdot 10\left(\frac{L}{W}\right) = 10R_1 \text{ with std } \sigma_{R2},$$

$$\sigma_{R2}^{\,2} = \sum_{j=1}^{10} \sigma_{R_j}^{\,2} = 10\sigma_{R1}^{\,2} \Rightarrow \sigma_{R2} = \sqrt{10}\sigma_{R1}$$

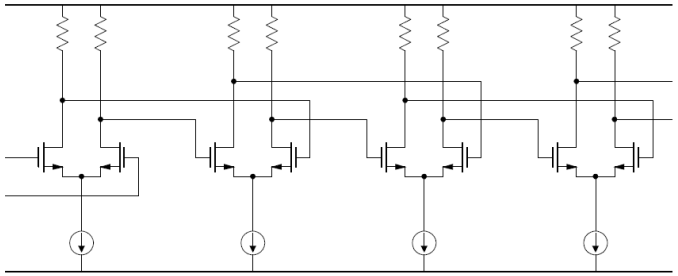
$$\frac{\sigma_{R2}}{R_2} = \frac{\sqrt{10}\sigma_{R1}}{10R_1} = \frac{1}{\sqrt{10}}\left(\frac{\sigma_{R1}}{R_1}\right) \Rightarrow \frac{\sigma_R}{R} \propto \frac{1}{\sqrt{A}} = \frac{1}{\sqrt{WL}}$$

"Spatial averaging"

PRE-AMP DESIGN

A fully-differential gain-stage

- Avoid or use simple CMFB
- Pre-amp gain reduces input referred offset due to the latch
- Autozero techniques for offset storage and reduction



Pre-amp open-loop gain vs tracking bandwidth trade-off

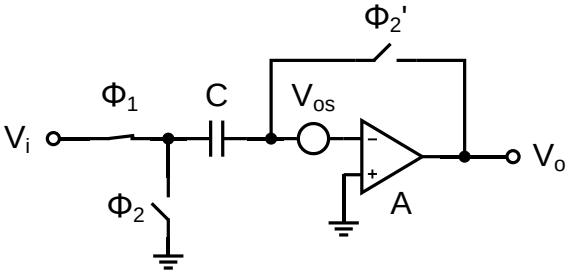
- Multiple stages of pre-amp limit bandwidth
  - Optimum value of stages 2-4

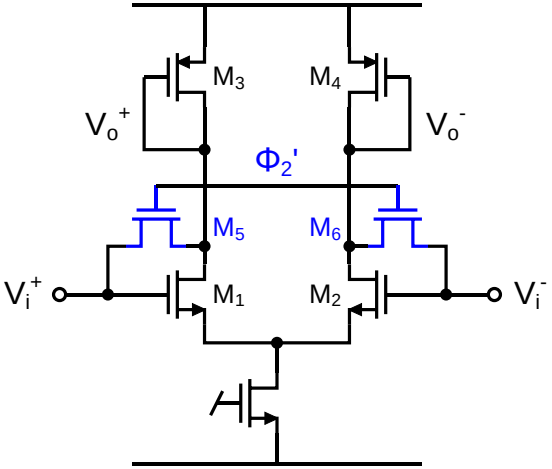
N stages:

$$\left|A_N(\omega)\right| = \left|\left(\frac{A_0}{1+j\cdot\omega/\omega_0}\right)^N\right| = \left(\frac{A_0}{\sqrt{1+(\omega/\omega_0)^2}}\right)^N$$

$$\left|A_N(\omega=\omega_{-3dB})\right| = \frac{A_0^{\,N}}{\sqrt{2}}, \quad \omega_{-3dB} = \omega_0\sqrt{2^{\frac{1}{N}}-1}$$

PRE-AMP (PA) AUTOZERO





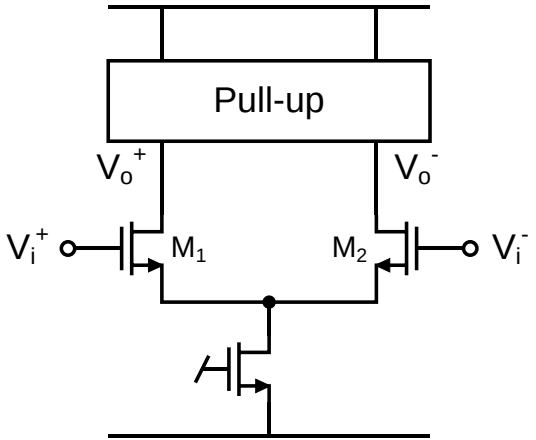
- Finite preamp gain :

$$V_{OS,in} \approx \frac{V_{OS,pre-amp}}{A}$$

- For the overall comparator :

$$\sigma^2_{V_{OS,in}} \approx \frac{\sigma^2_{V_{OS,pre}}}{\left(1+A_{pre}\right)^2} + \frac{\sigma^2_{V_{OS,Latch}}}{A^2_{pre}}$$

PRE-AMP DESIGN: PULL-UP LOAD



- NMOS diode pull-up:

$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{(W/L)_1}{(W/L)_L}}$$

- PMOS diode pull-up:

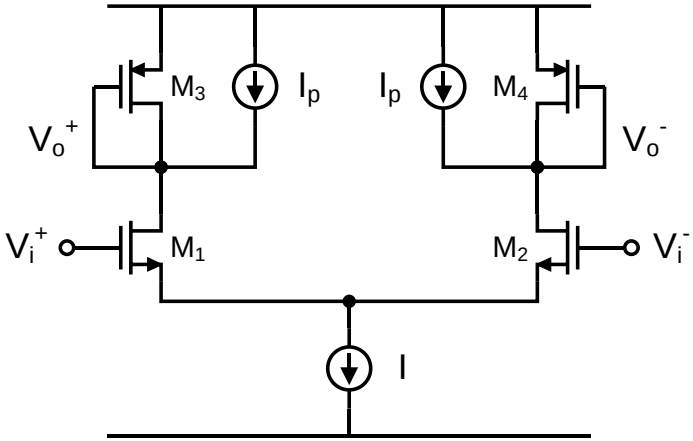
$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{\mu_n}{\mu_p}\frac{(W/L)_1}{(W/L)_L}}$$

- Resistor pull-up:

$$A_V = -g_{m1} \cdot R_L$$

- NMOS pull-up suffers from body-effect, affecting gain accuracy
- PMOS pull-up is free from body-effect, but subject to P/N mismatch
- Gain accuracy is the worst for resistive pull-up as resistors (poly, diffusion, well, etc.) don't track transistors; but it is fast!

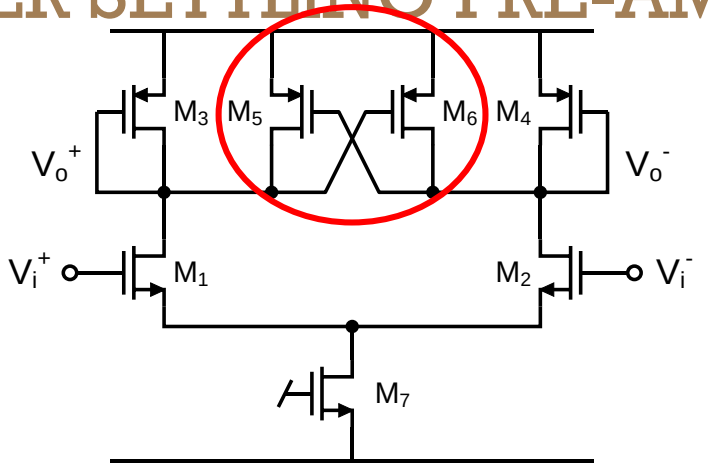
PRE-AMP DESIGN: MORE GAIN

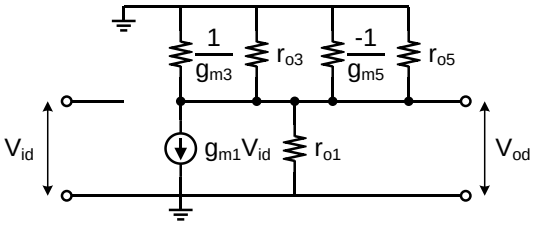


$$A_V = -\frac{g_{m1}}{g_{m3}} \approx -\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{I/2}{I/2 - I_p}\right)\frac{(W/L)_1}{(W/L)_3}}$$

- I_p diverts current away from PMOS diodes (M_3 & M_4), reducing $(W/L)_3$
- Higher gain without CMFB
- Needs biasing for I_p
- M_3 & M_4 may cut off for large V_{in}, resulting in a slow recovery

FASTER SETTLING PRE-AMP



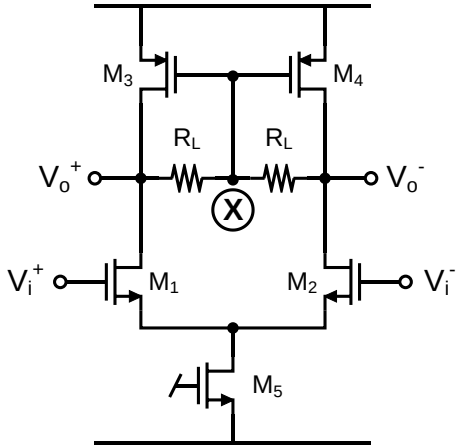


$$\text{DM gain: } A_v^{dm} = -g_{m1}\cdot\left[\frac{1}{g_{m3}}//\left(-\frac{1}{g_{m5}}\right)//r_{o1}//r_{o3}//r_{o5}\right] \approx -\frac{g_{m1}r_{o1}}{3}$$

- NMOS diff-pair loaded with PMOS diodes and a PMOS cross-coupled latch
- High DM gain, low CM gain, good CMRR
- Simple, no CMFB required
- $(W/L)_{34} > (W/L)_{56}$ needs to be ensured for stability

Ref: K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," IEEE *JSSC*, vol. 32, pp. 1887-1895, issue 12, 1997.

PRE-AMP EXAMPLE

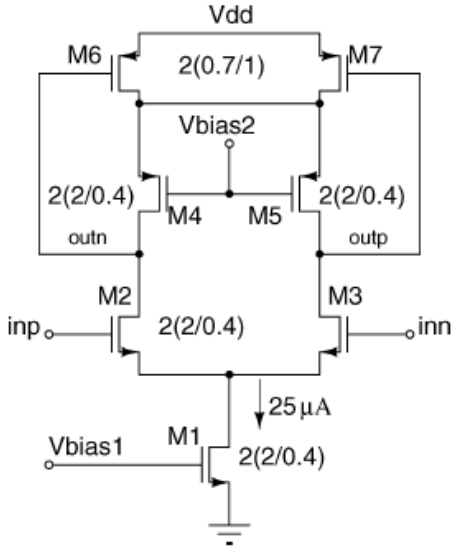


- NMOS diff. pair loaded with PMOS diodes and resistors
- High DM gain, low CM gain, good CMRR
- Simple, no extra CMFB required
- Gain not well-defined

Ref: B.-S. Song et al., “A 1 V 6 b 50 MHz current-interpolating CMOS ADC,” in IEEE *Symp. VLSI Circuits*, 1999, pp. 79-80.

PRE-AMP EXAMPLE

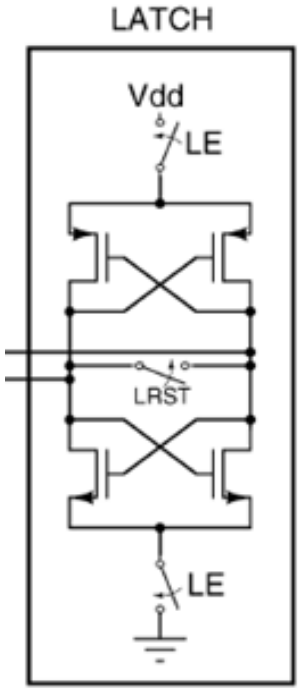
- NMOS diff. pair loaded with PMOS Current mirror
  - Simple CMFB circuit using triode PMOS
- Large DM gain, small CM gain



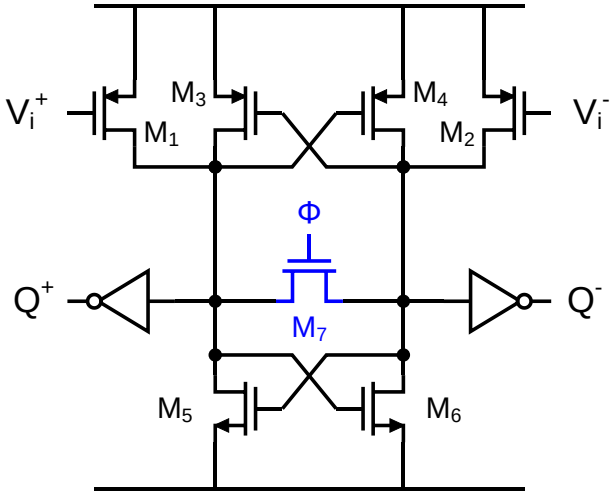
Ref: V. Srinivas, S. Pavan, A. Lachhwani, and N. Sasidhar, “A Distortion Compensating Flash Analog-to-Digital Conversion Technique," IEEE JSSC, vol. 41, no. 9, pp. 1959-1969, Sep. 2006.

LATCH DESIGN

- Regenerative latches for faster settling
  - See lecture notes
- At least one cross-coupled regenerative core
  - Numerous methods for applying the input initial signal for regeneration
  - Latches can have large static and dynamic offsets
- Large Regenerative gain for resolving small inputs
  - Metastability (wrong or incomplete decisions) when latch can't make decision
  - Pre-amp used for larger gain (slower tracking BW)
- One topology doesn't fit all the applications
  - Speed vs power consumption trade-off

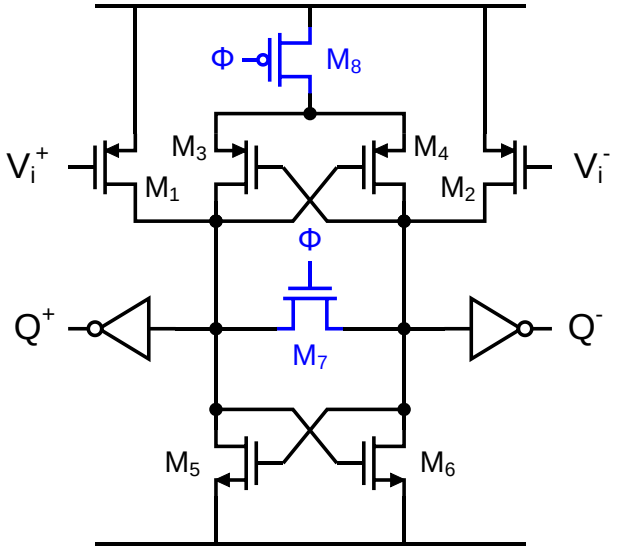


STATIC LATCH EXAMPLE



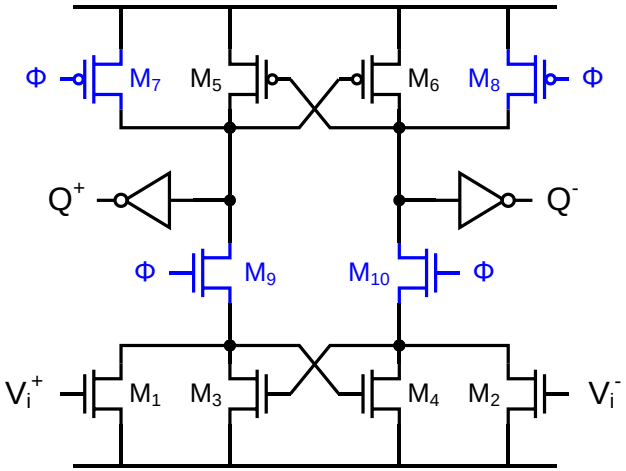
- Active pull-up and pull-down
  - full CMOS logic levels
- Very fast!
- Q^+ and Q^- are not well defined in reset mode ($\Phi = 1$)
- Large short-circuit current in reset mode
- Zero DC current after full regeneration
- Supply is very noisy

SEMI-DYNAMIC LATCH EXAMPLE



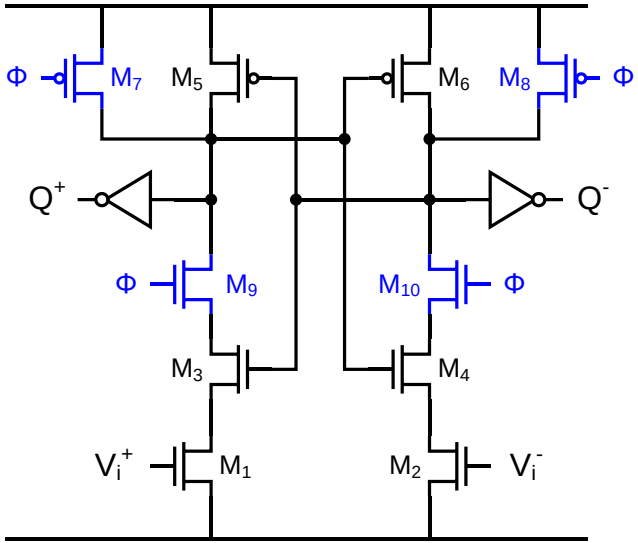
- Latch is disabled in reset mode
  - less static current
- Pull-up not as fast
- Q^+ and Q^- are still not well defined in reset mode ($\Phi = 1$)
- Zero DC current after full regeneration
- Supply still very noisy

DYNAMIC LATCH EXAMPLE



- Zero DC current in reset mode
- Q^+ and Q^- are both reset to “0”
- Full logic level after regeneration
- Slow

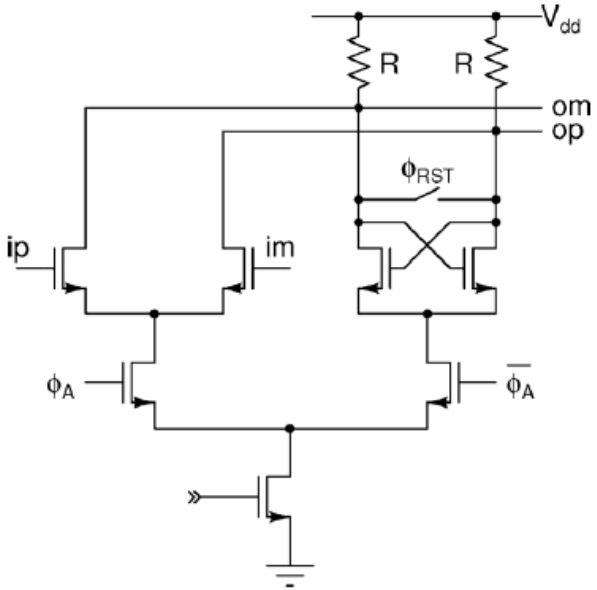
DYNAMIC LATCH EXAMPLE 2



- Zero DC current in reset mode
- Q^+ and Q^- are both reset to “0”
- Full logic level after regeneration
- Slow

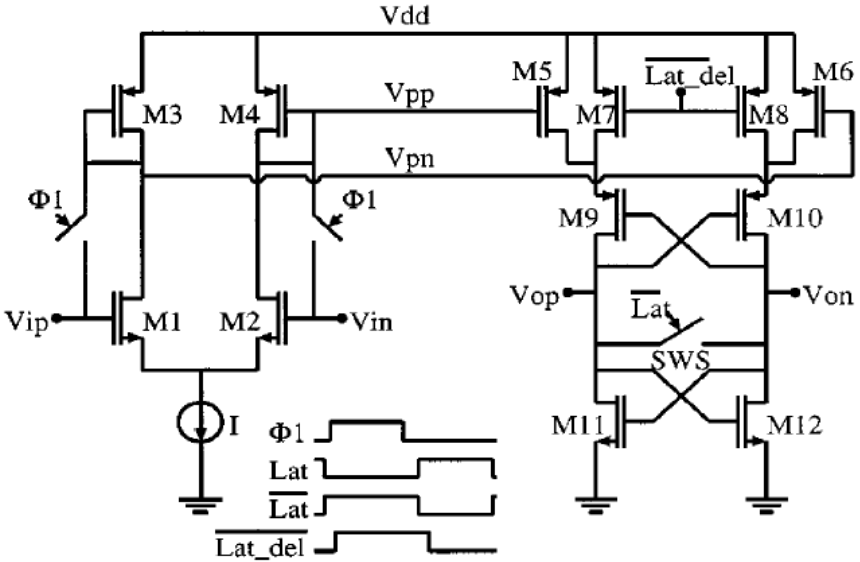
Ref: T. B. Cho and P. R. Gray, “A 10 b, 20 Msample/s, 35 mW pipeline A/D converter,” *JSSC*, vol. 30, pp. 166-172, issue 3, 1995.

CURRENT-STEERING/CML LATCH



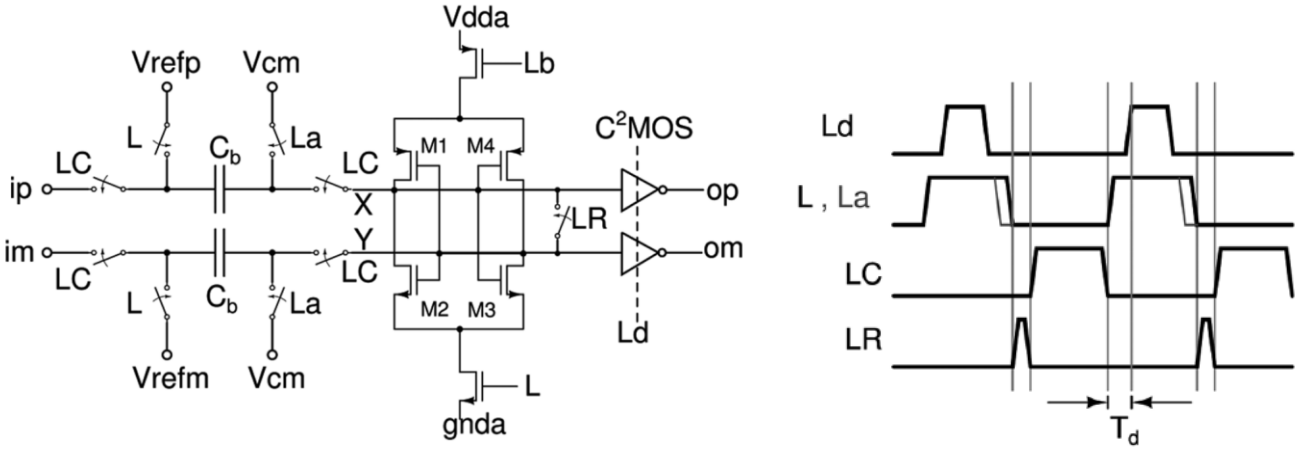
- Current mode logic (CML) latch
- Constant bias current
  - supply very quite
- Higher gain in tracking mode
- Cannot produce full logic levels
- Fast
  - Popular for high-speed designs

COMPARATOR WITH PA AUTOZERO



I. Mehr and L. Singer, “A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC,” IEEE JSSC March 2000, pp. 318-25.

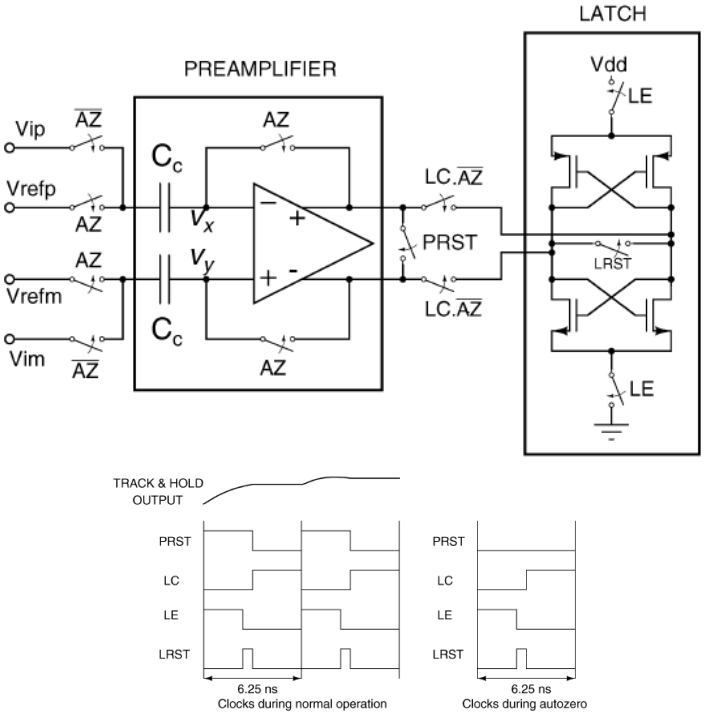
LOW-POWER LATCH WITH REFERENCE SUBTRACTION

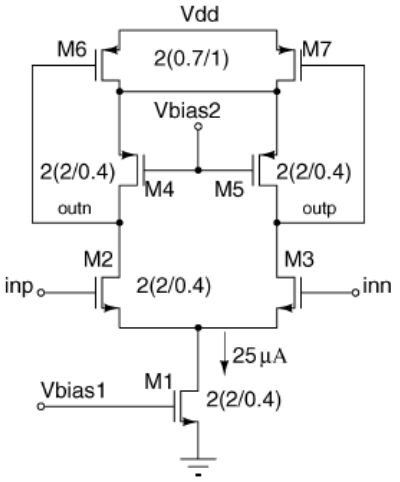


- Energy efficient comparator for medium speed data converters
- Large number of clock phases
  - Driving and routing at higher clock rates leads to more power consumption

S. Pavan, N. Krishnapura, R. Pandarinathan, P. Sankar, "A Power Optimized Continuous-time Delta-Sigma Modulator for Audio Applications," IEEE JSSC, vol. 43, no. 2, pp. 351-360, Feb. 2008.

AUTOZERO AND REFERENCE SUBTRACTION

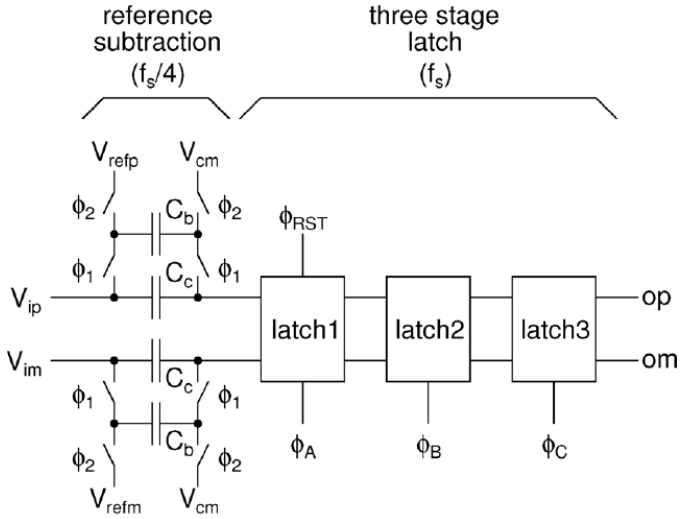


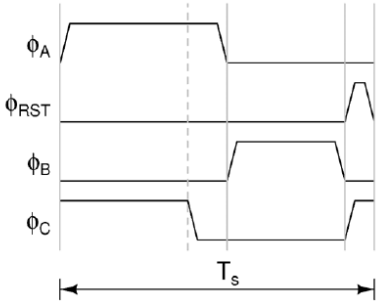


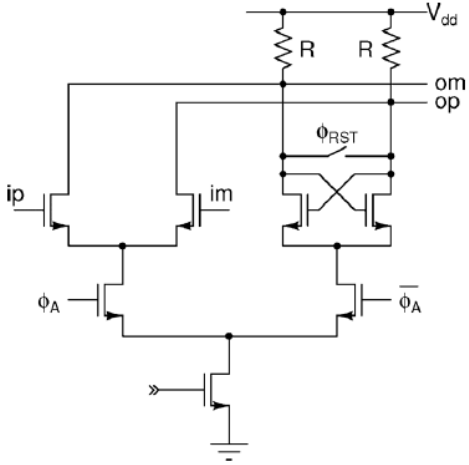
Pre-amp

V. Srinivas, S. Pavan, A. Lachhwani, and N. Sasidhar, "A Distortion Compensating FlashAnalog-to-Digital Conversion Technique," IEEE JSSC, vol. 41, no. 9, pp. 1959-1969, Sep. 2006.

CML BASED COMPARATOR







CML-Latch

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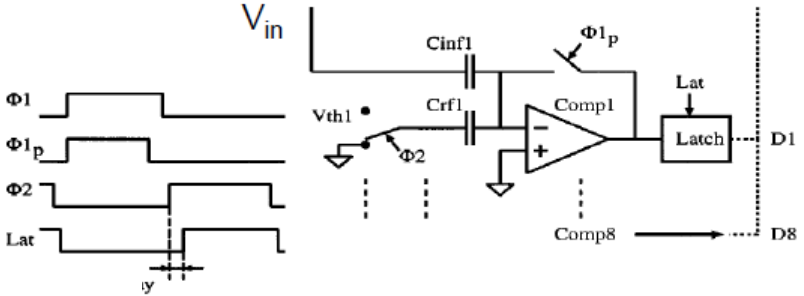
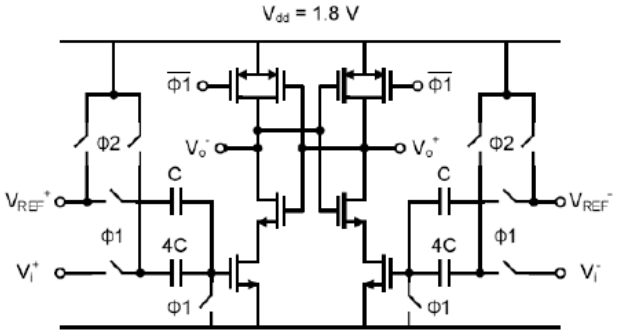
COMPARATORS FOR PIPELINED ADCS

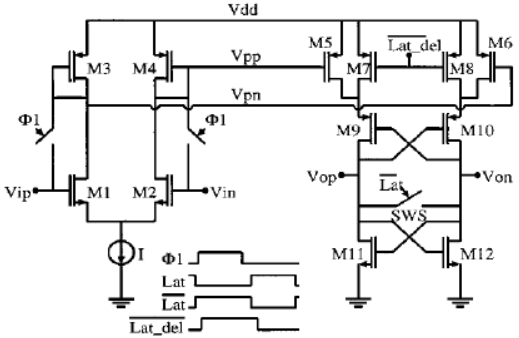
- Pipelined ADCs employ at least 0.5 bit/stage redundancy
  - Can tolerate large offsets and large noise with appropriate redundancy
- Should consume negligible power in a good design
  - 50-100 μW or less per comparator
- Lots of implementation options
  - Resistive/capacitive reference generation
  - Different pre-amp/latch topologies

COMPARATORS FOR PIPELINED ADCS



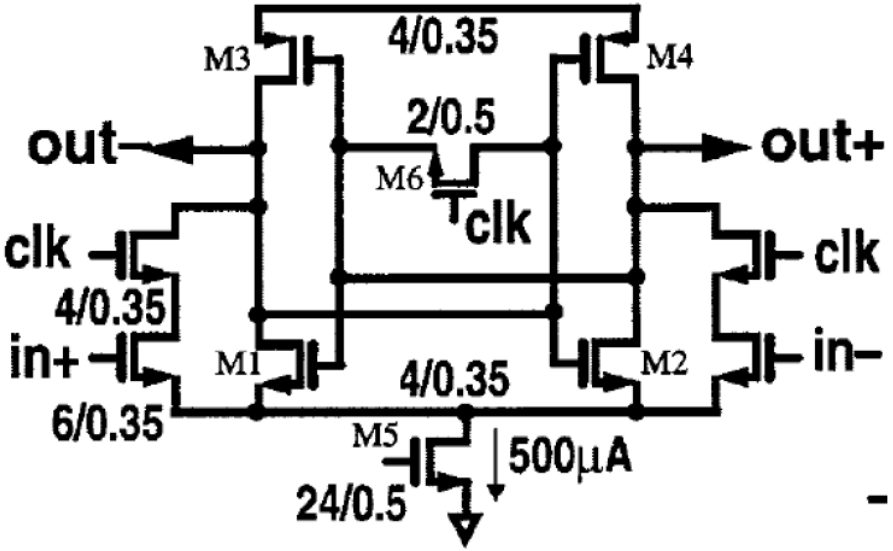
[Chiu 2004]





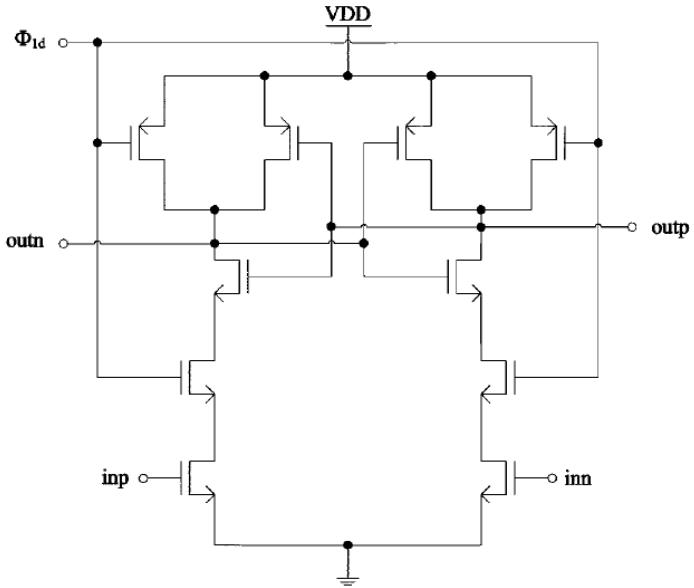
[Mehr 2000]

COMPARATOR EXAMPLE



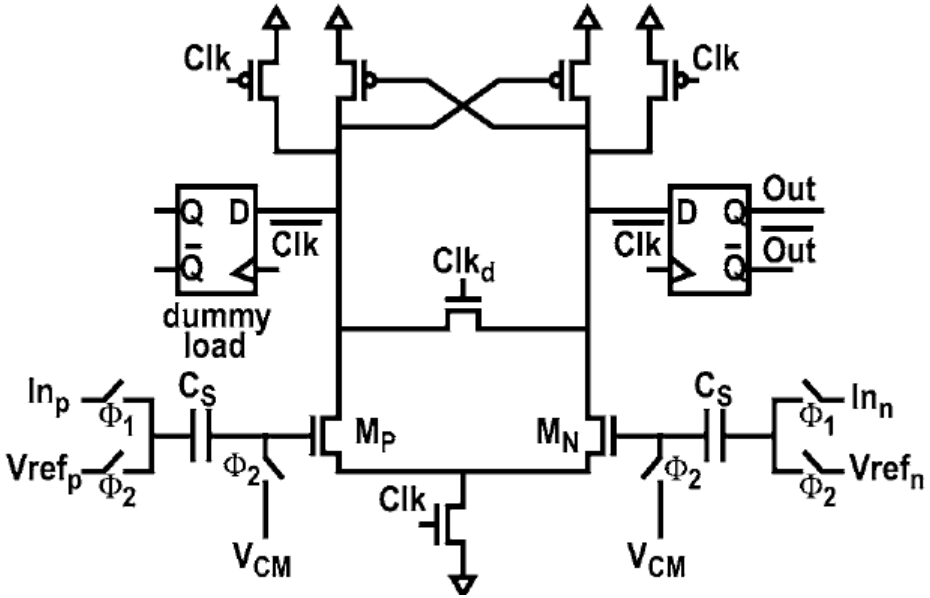
A 6-b 1.3-Gsample/s A/D Converter in 0.35-m CMOS IEEE JSSC, vol. 36, no. 12, Dec 2001.

LATCH EXAMPLE



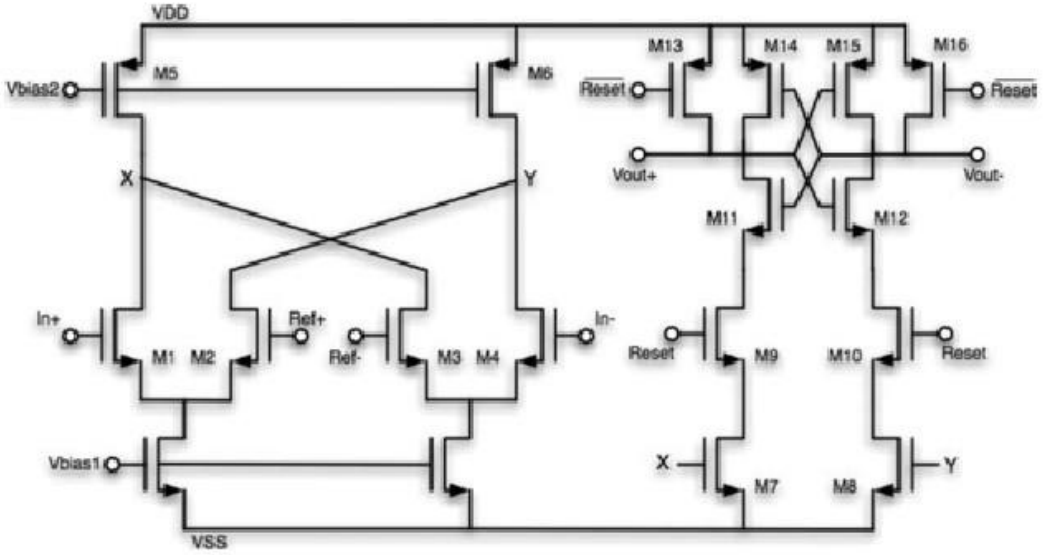
A 0.9-V 60-W 1-Bit Fourth-Order Delta-Sigma Modulator With 83-dB Dynamic Range IEEE JSSC, vol. 43, no. 2, Feb. 2008

COMPARATOR EXAMPLE



A 77-dB Dynamic Range, 7.5-MHz Hybrid Continuous-Time/Discrete-Time Cascaded ΔΣ Modulator, IEEE JSSC, vol. 43, no. 4, Apr 2008

COMPARATOR EXAMPLE



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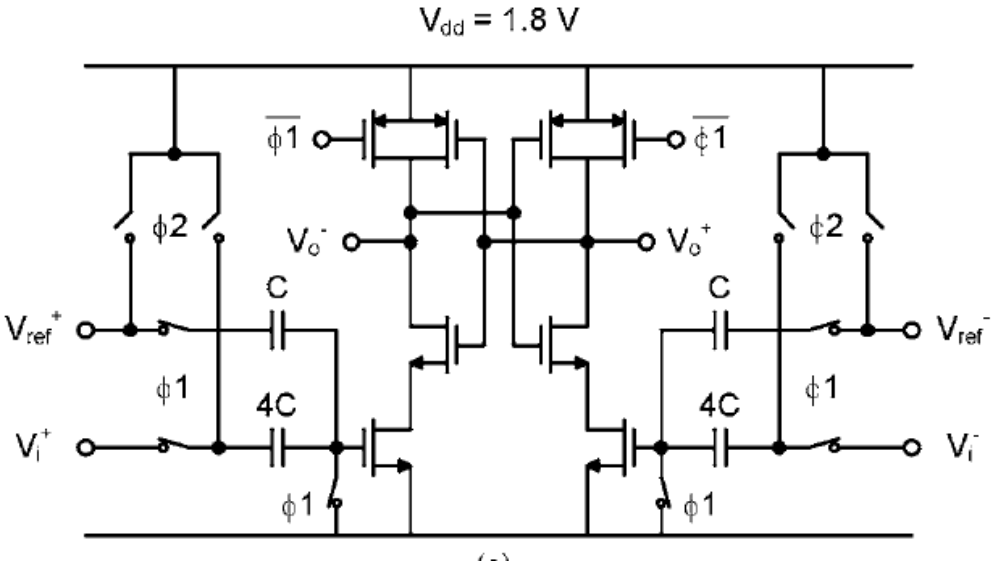
COMPARATOR EXAMPLE



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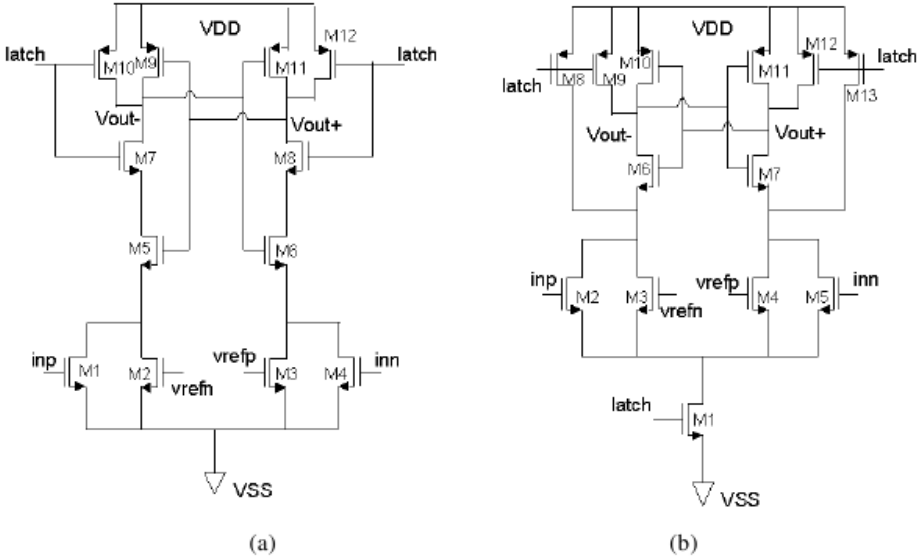
COMPARATOR EXAMPLE



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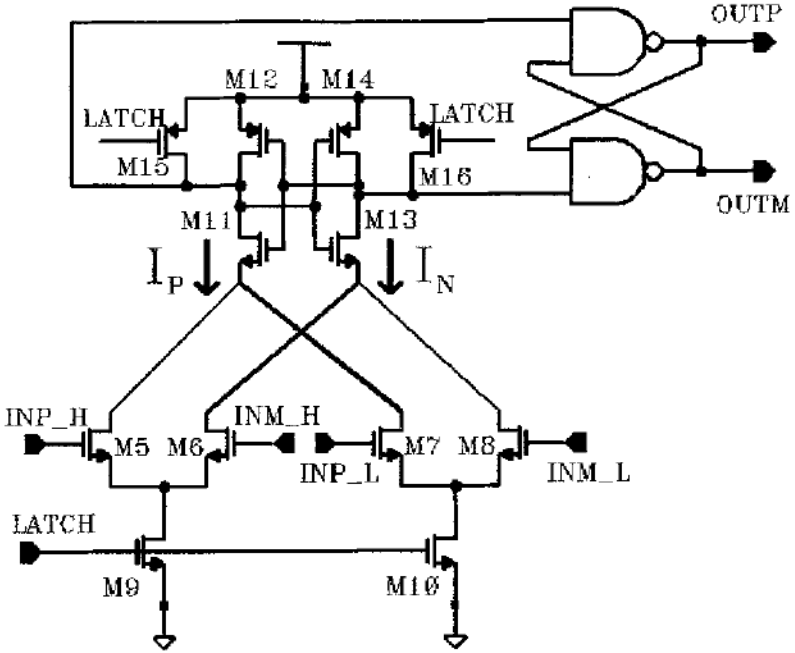
COMPARATOR EXAMPLE



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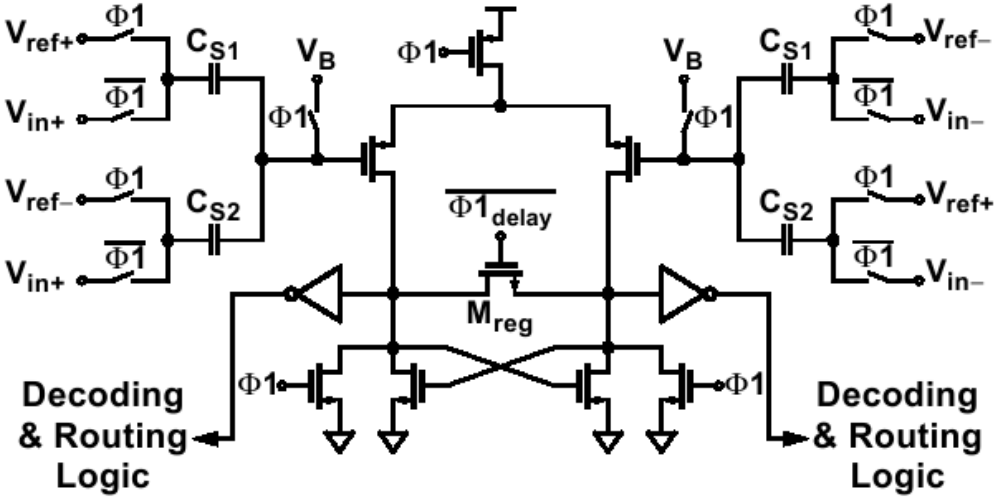
COMPARATOR EXAMPLE



S . Limotyrakis, S. D. Kulchycki, D. Su, and B. A. Wooley, "A 150MS/s 8b 71mW time-interleaved ADC in 0.18µm CMOS," proc. IEEE ISSCC, pp. 258 - 259, Feb 2004.

EXERCISE

Compare the latches with respect to

- Static power dissipation
- Dynamic and Static Offsets
- Kickback noise at the input
- Number of clock phases
- Maximum achievable clock speed

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