## CADENCE SIMULATION SETUP FOR 180NM CMOS DESIGNS





- Create a new library (Test180n in this example)
- Since we do not have a PDK for the 180n CMOS process, attach "cdsDeftechLib" as the techlib.







- Create a new schematic view
- You will be prompted to set the Mosfet minimum dimensions
- Enter 0.18 for all values (180n process)





- Create NMOS instance with desired W and L.
- Make sure you set the model name to cmosn or cmosp
- Use setting of model type=user for changing this parameter







• Create your schematic as shown above. Note the model name and dimensions (absolute values are used)





- Model location on engr-410 server is at
- /home/vsaxena/analog\_design/models





 Set the model location: model card tsmc018.scs located at /home/vsaxena/analog\_design/models



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|   |  | Enabled 🗹 Detions  |   |

• Set up your desired analysis (VGS DC sweep in this example)





- Run simulation
- Contact instructor/TA is you have difficulty in getting to this point.

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