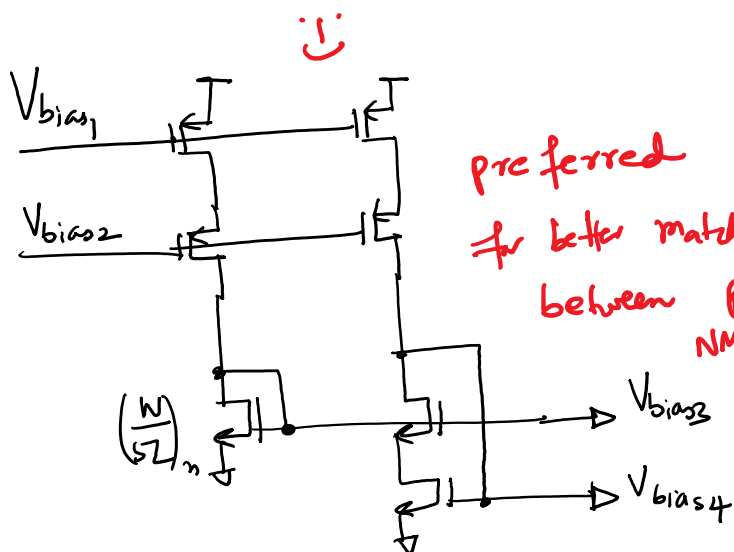
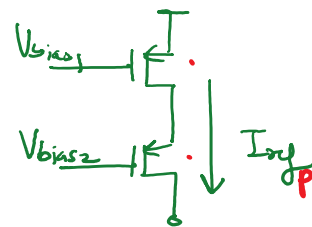
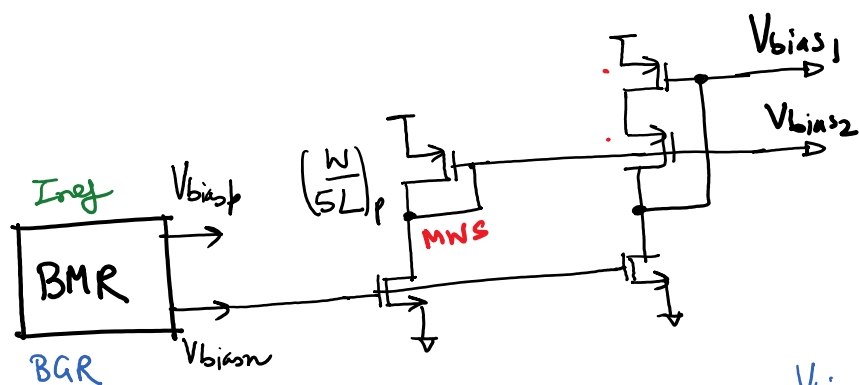
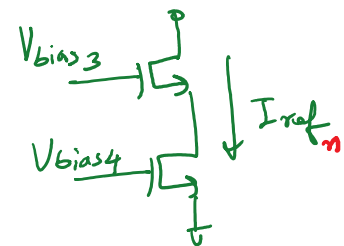
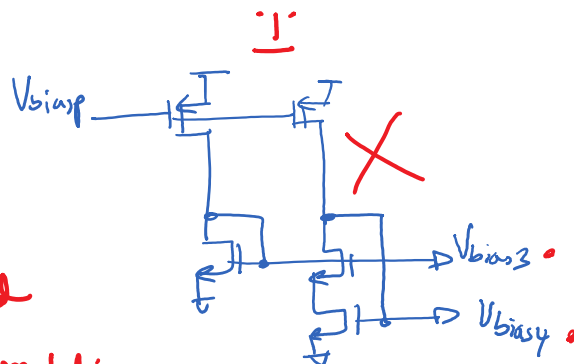


ECE 515- Lecture 9

Thursday, September 20, 2018 11:03 AM

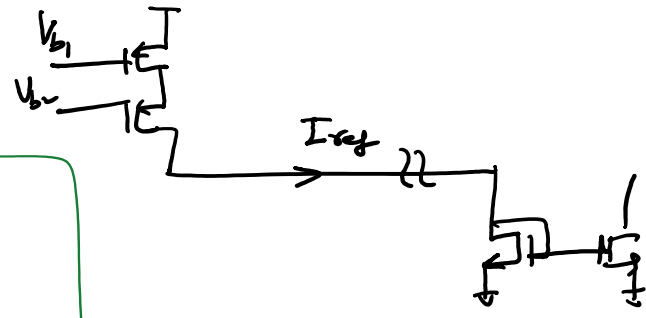
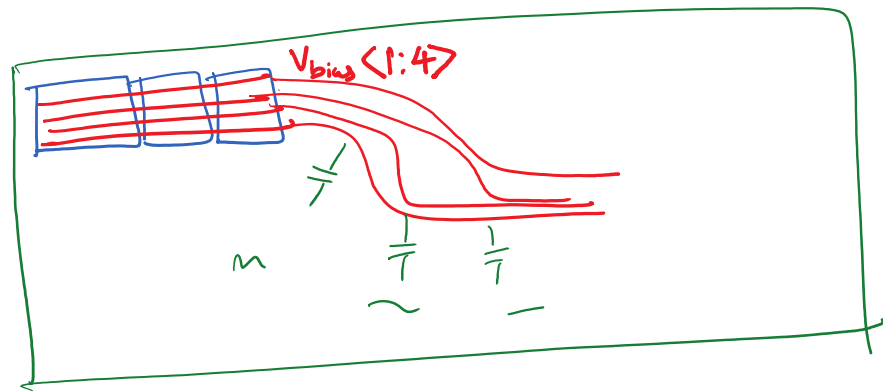
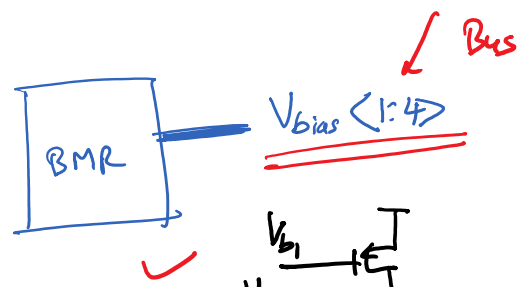
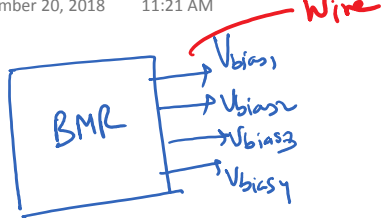


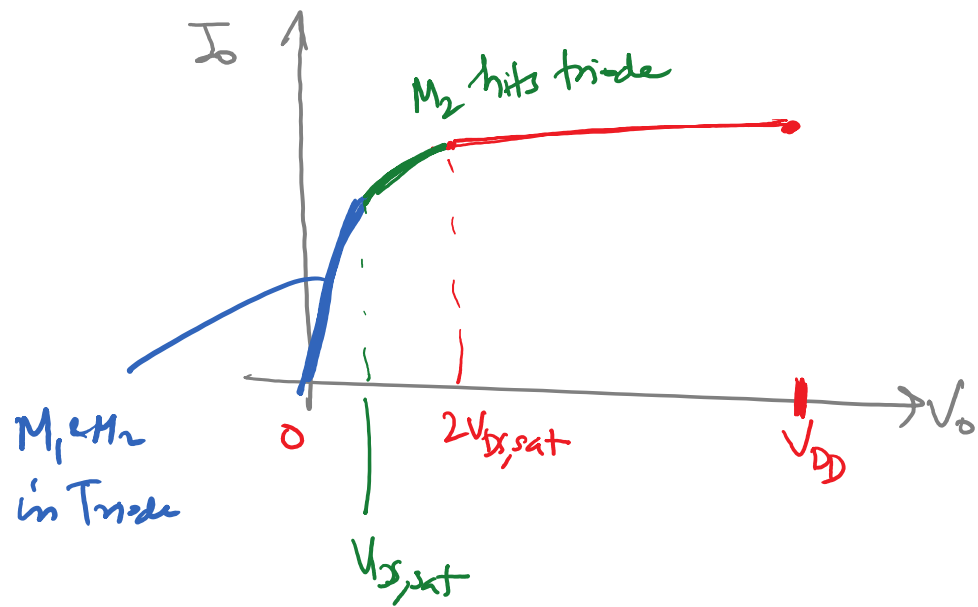
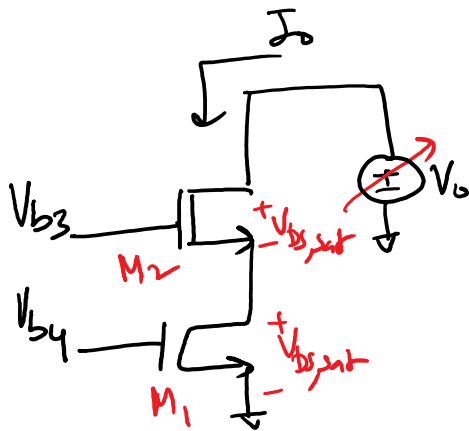
preferred
for better matching
between PMOS &
NMOS current
mirrors



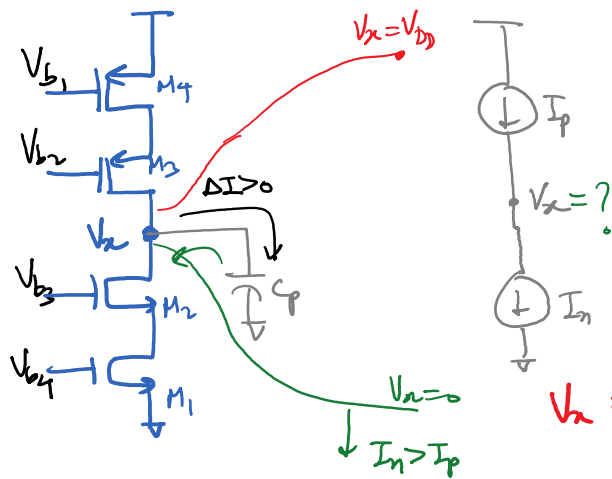
for short channel design use longer L in MWS transistor

Hierarchical





I_p & I_n refer to I_{ref}



$V_x = ?$

$I_p \neq I_n$

V_x is not well-defined.

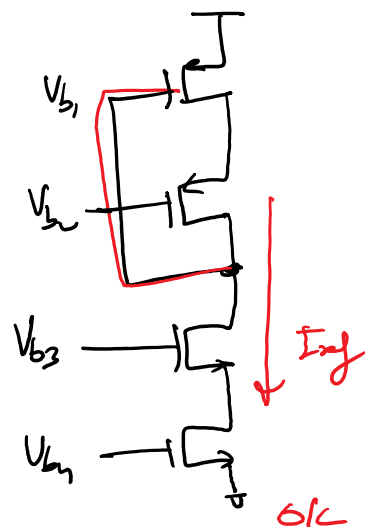
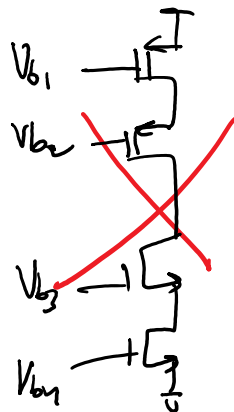
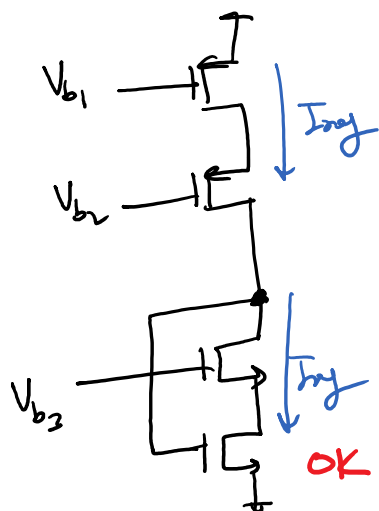
* Can never have two independent current source "fight" with each other.

$$I_p > I_n$$

$$\Delta I = I_p - I_n$$

* small current mismatch

* Always make one source dependent on the other.



Short-channel

transition frequency
at which the
current gain is 1
 $\Rightarrow f_T \propto \frac{V_{ov}}{L}$

gain x BW tradeoff in a
transistor

Maximum
gain extract from
a transistor
 $\Rightarrow g_m r_o \propto \frac{L}{V_{ov}}$

$V_{ov} \uparrow \Rightarrow f_T \uparrow \Rightarrow g_m r_o \downarrow \rightarrow$ cascoding to increase gain
 \rightarrow lower swing

Typically $L = 2-5 \times L_{min}$

Long-channel CMOS

$$\frac{f_{Tp}}{f_{Tn}} = \frac{\mu_p}{\mu_n} \approx \frac{1}{3} \quad \text{in Silicon}$$

PMOS are ^{3x} slower than NMOS

Short-channel CMOS

$$\frac{f_{Tp}}{f_{Tn}} \approx \frac{V_{satp}}{V_{satn}} \approx \frac{1}{2}$$

PMOS are 2x slower than NMOS

* Really need to check the datasheet/sims for 40nm or below

→ FinFET (<14nm)

$V_{ov} \Rightarrow$ sets the "speed" → BW of the design

good speed $V_{ov} \approx 5\%$ of V_{DD}

$$g_m = \frac{2I_D}{V_{ov}}$$

$$\Rightarrow \left(\frac{g_m}{I_D} \right) = \left(\frac{2}{V_{ov}} \right)$$

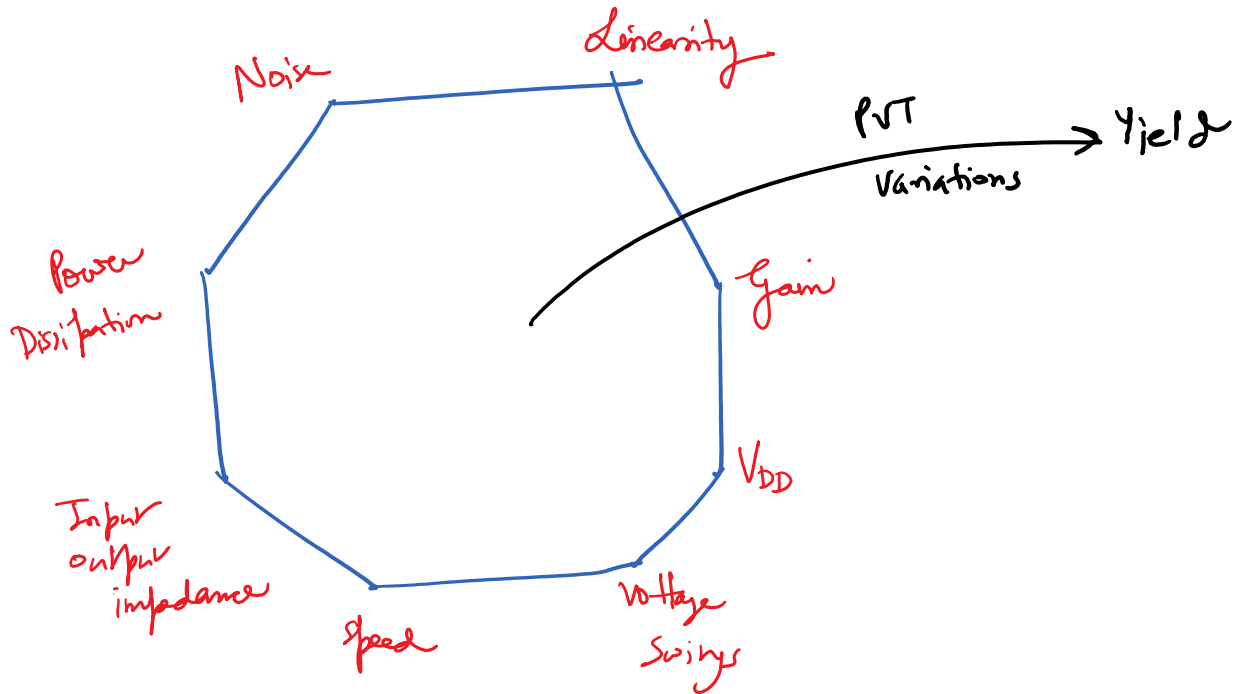
$\frac{g_m}{I_D}$ design methodology.

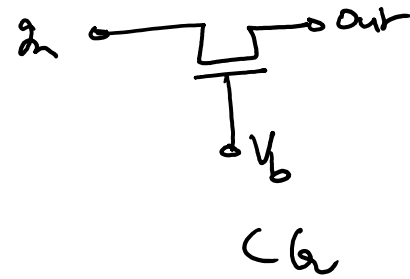
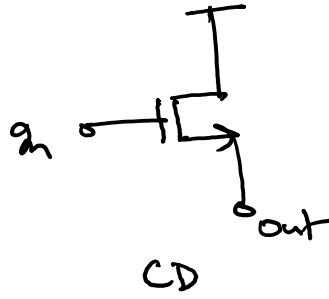
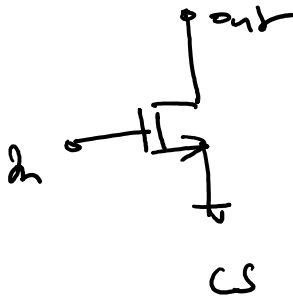
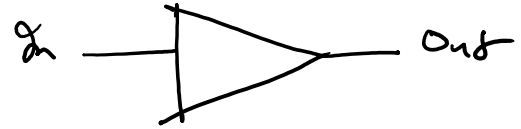
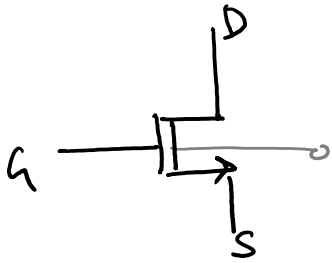
Either fix V_{ov} for a design
or fix $\left(\frac{g_m}{I_D} \right)$

Single-Stage Amplifiers :

Thursday, September 20, 2018 10:57 AM

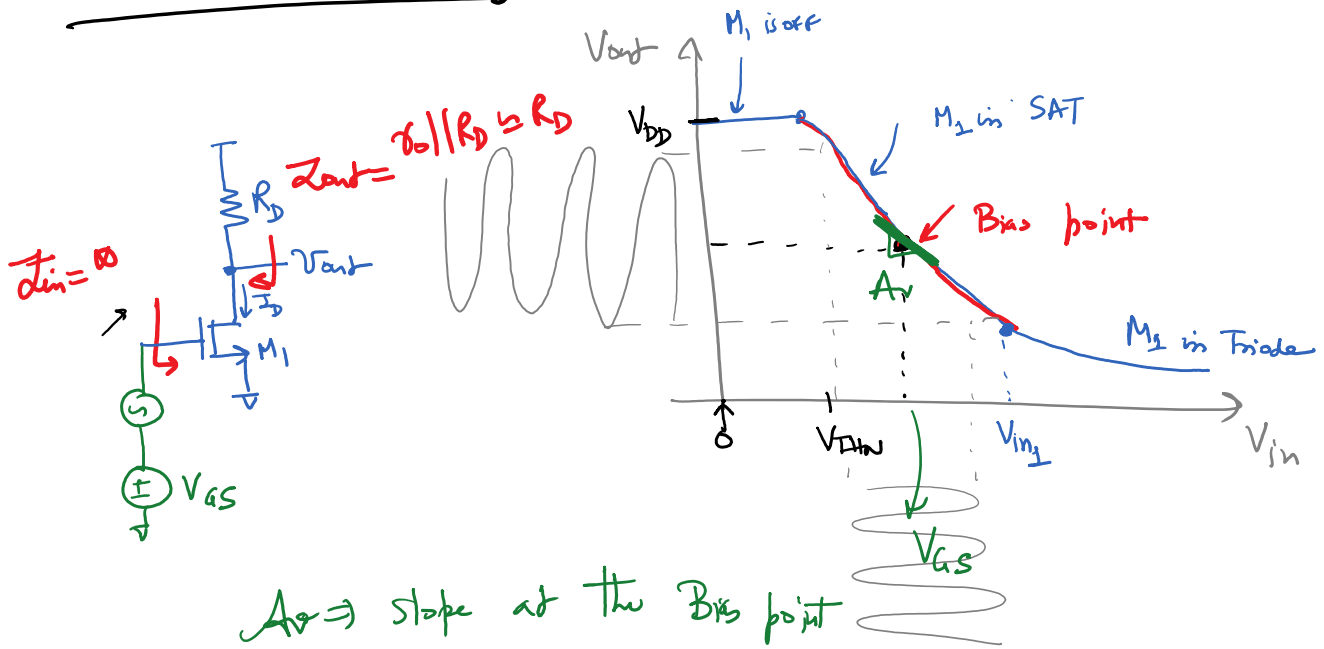
Analog Design Objective \Rightarrow multidimensional trade-off





Common Source Stage :

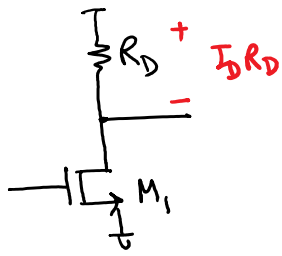
Large Signal Characteristics



$A_v \Rightarrow$ slope at the Bias point

$$A_v = -g_m(r_o \parallel R_D) \approx -g_m R_D$$

$$R_D \ll r_o$$



$$A_v = g_m R_D$$

$$A_v \Rightarrow$$

$$R_D \uparrow$$

$$g_m \uparrow \Rightarrow I_D \uparrow$$

Current Mirror Load

