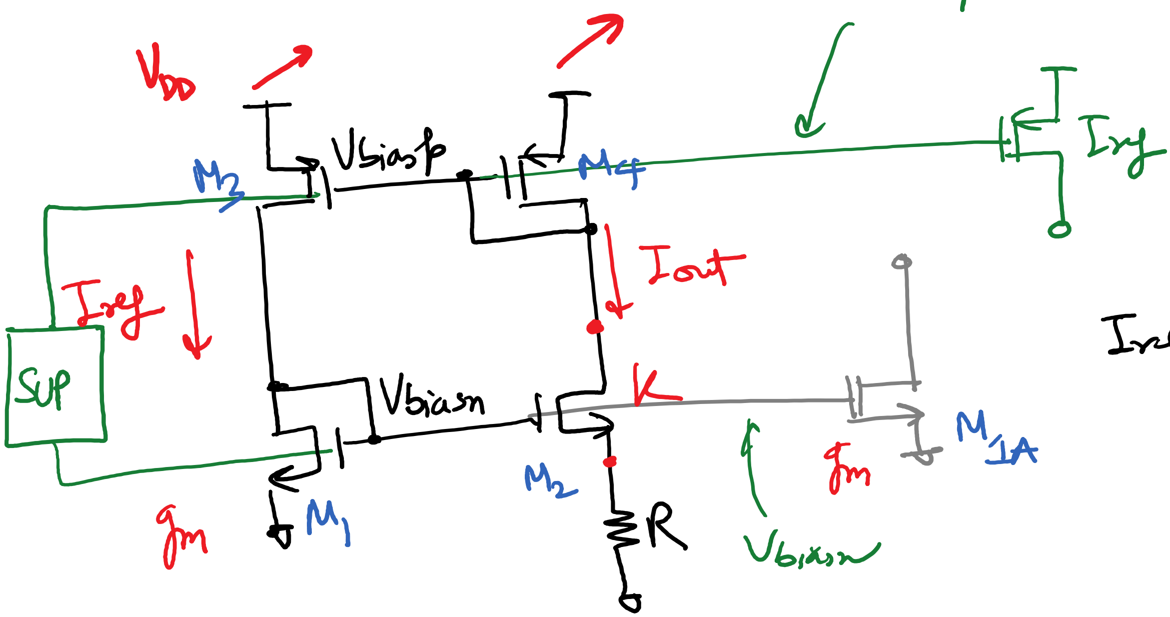
ECE 515 - Lecture 7

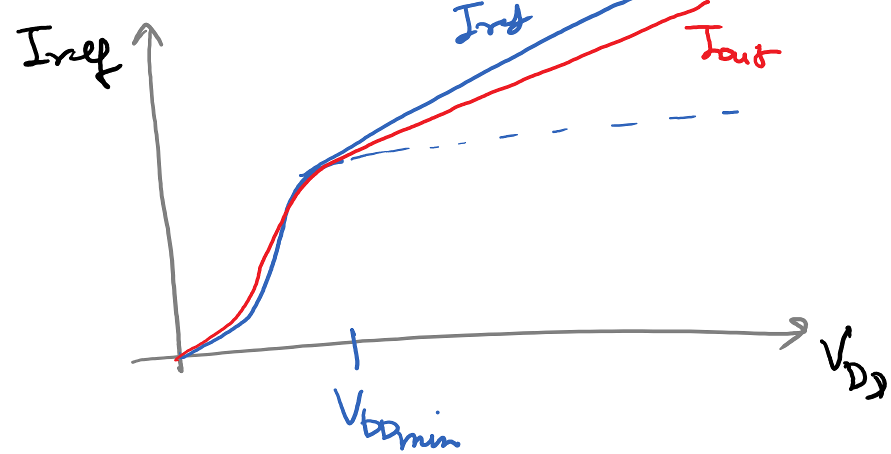
Thursday, September 13, 2018 11:02 AM

BMR.

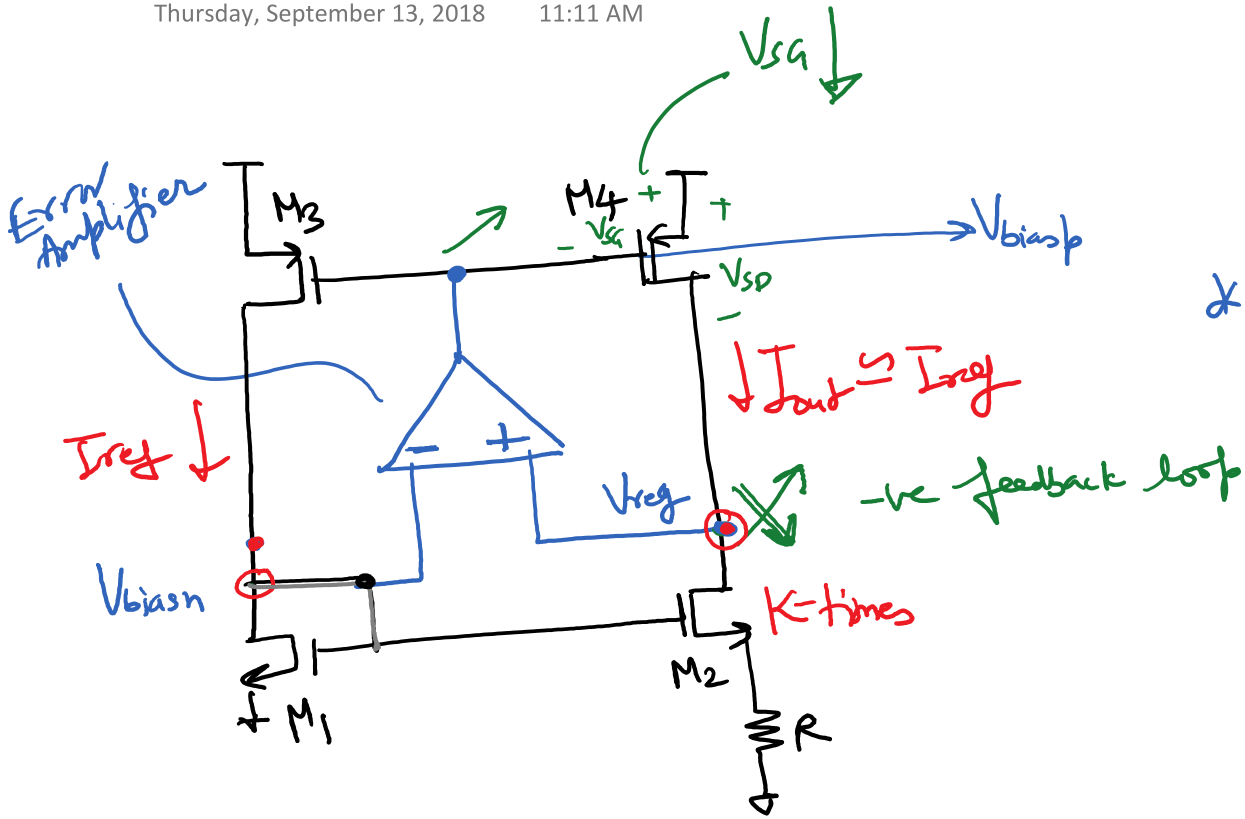


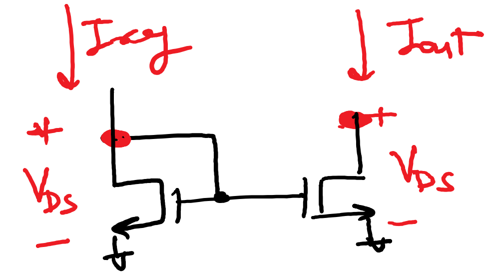
λ=0

in short-channel CMOS



Thursday, September 13, 2018 11:11 AM





* Negative feedback loop keeps Vreg close to Vbiasn

↳ drains of M_3 & M_4 are at the same potential

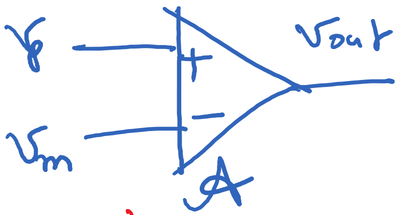
↓

Iout & Iref are held closer

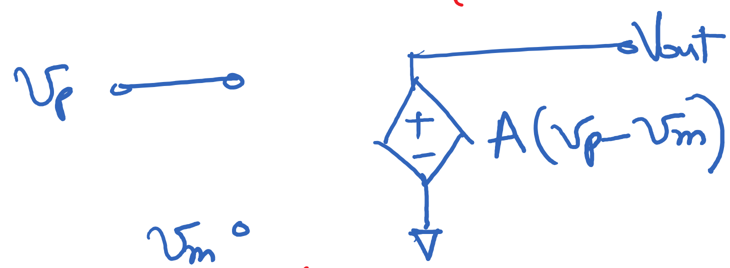
* Effectively increasing the output resistance of the PMOS current current source

Behavioral model

Thursday, September 13, 2018 11:22 AM

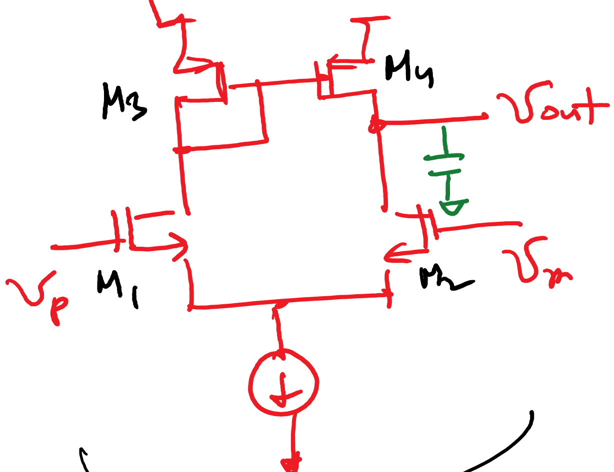


$\Rightarrow$

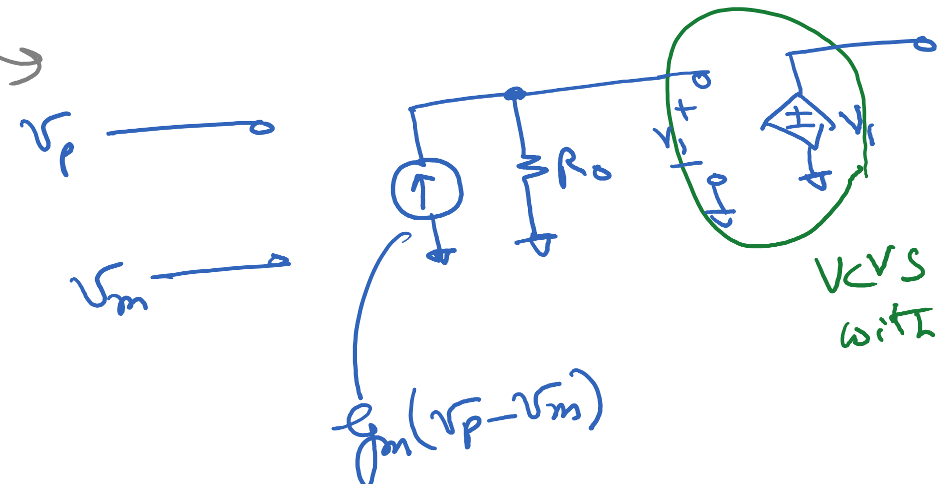


analogLib

large gain → convergence



$$A_v = g_{m_{1,2}} \cdot r_{o2} \| r_{o4}$$

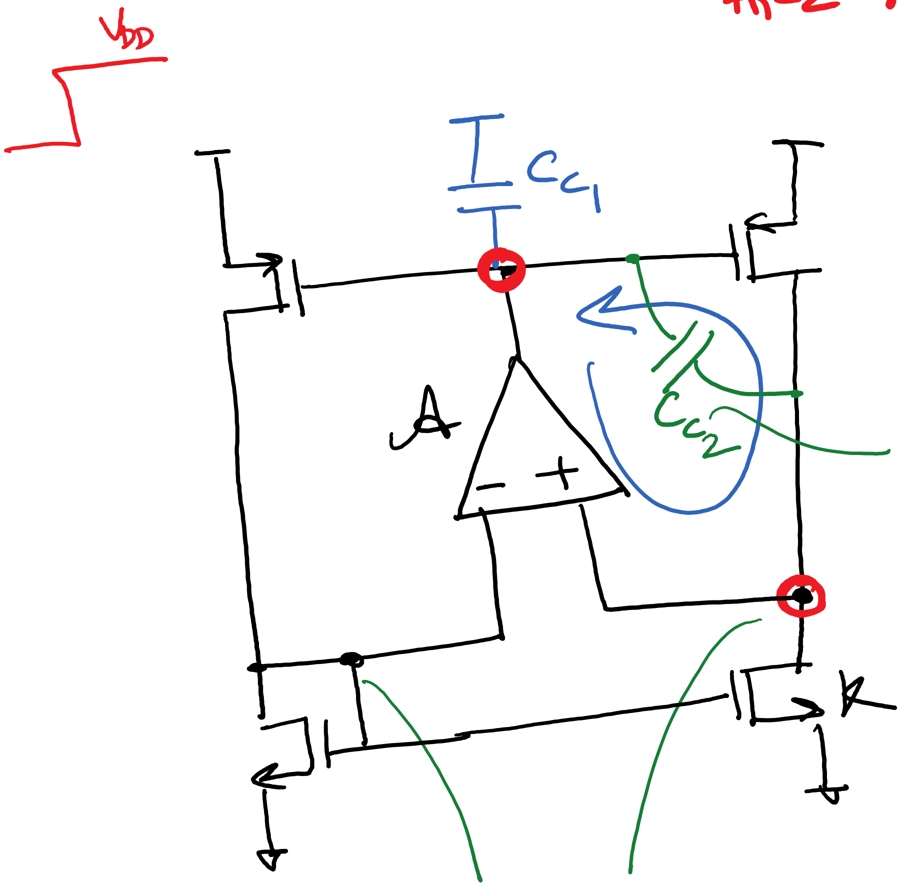


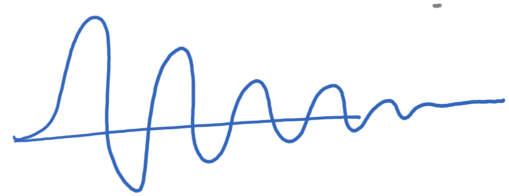
VCVS
with gain = 1

$$A = g_m R_o$$

VerilogA.

Hi-Z nodes

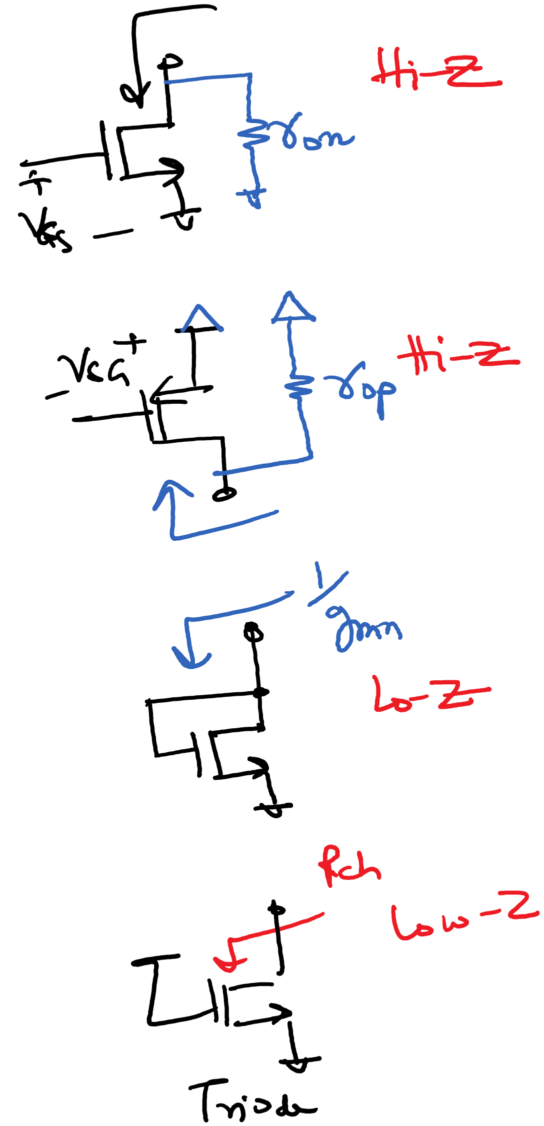




ω_{p1}, ω_{p2}

Miller Compensation Cap

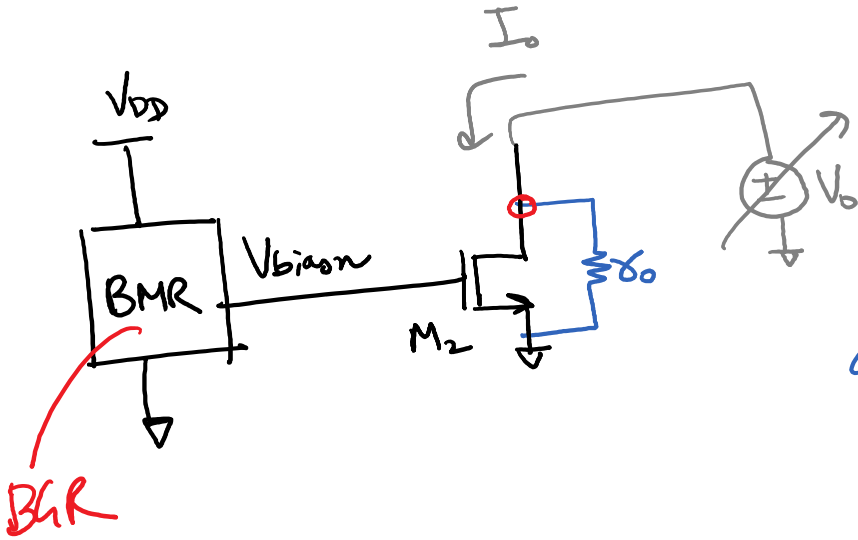
these nodes track each other

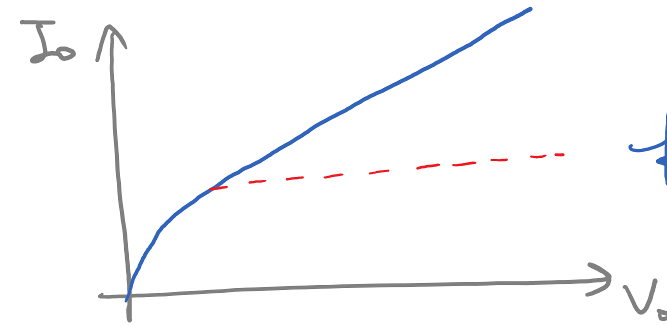


* Compensate this circuit ⇒ make it stable.

Cascoding (Cascode Current Mirrors)

Thursday, September 13, 2018 11:41 AM





CLM

finite r_o

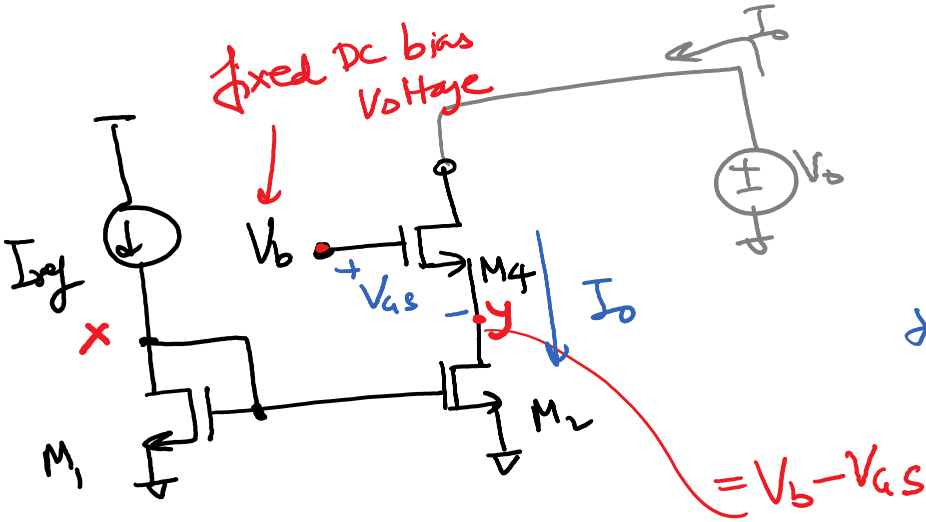
If we hold the drain of M_2 then the current I_o will not vary

↳ V_o should be fixed

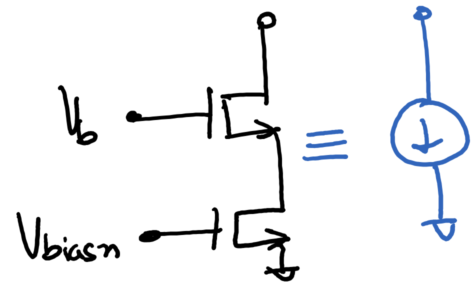
↳ not useful in a circuit !

ECE 515- Lecture 7

Thursday, September 13, 2018 11:46 AM



2 Transistor stack



* Add another device to hold the V_{DS} of the bottom device (M_2)
  ↳ leads to higher output impedance of the current mirror

$V_x = V_{GS}$

$V_y = V_{GS}$

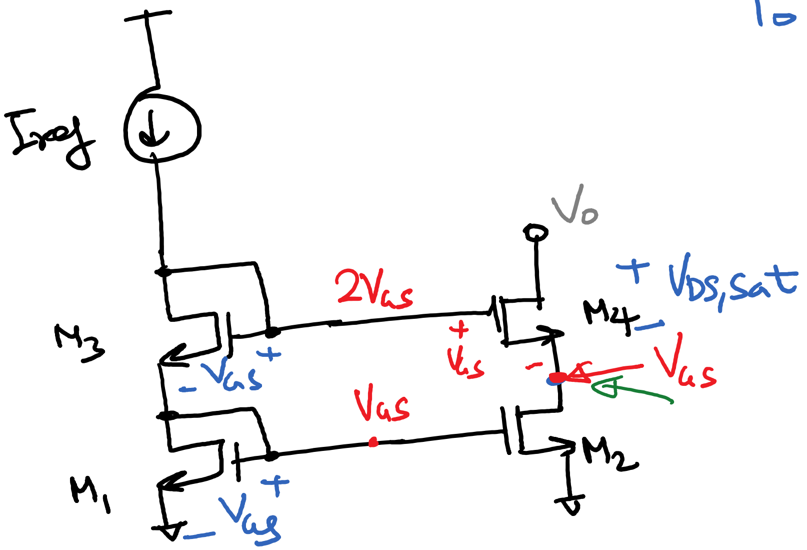
$V_b = 2V_{GS}$ $\Rightarrow$ Generate $V_b = 2V_{GS}$

$\Rightarrow V_x \triangleq V_y$

$\Rightarrow I_o$ tracks I_{ref}

Thursday, September 13, 2018 11:53 AM

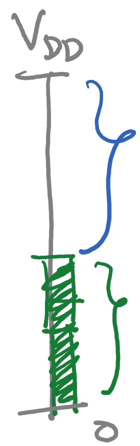
Simple Cascode Current Mirror



To keep M_2 & M_4 in SAT

$$V_o \geq V_{G4} + V_{DS,sat}$$
$$= (V_{DS,sat} + V_{THN}) + V_{DS,sat}$$
$$= 2V_{DS,sat} + V_{THN}$$

We are wasting one 'V_{THN}' of voltage swing

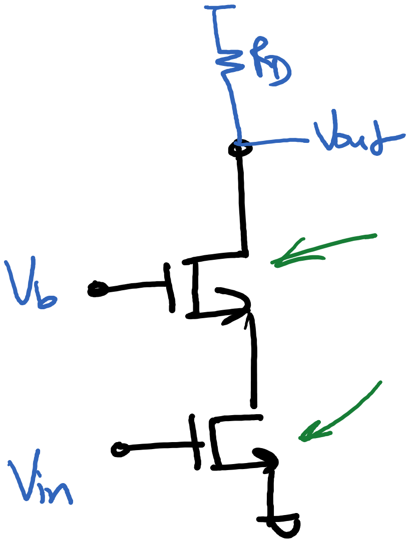


Useful voltage swing

$V_{THN} + 2V_{DS,sat}$

* We will optimize this current mirror later for wide swing biasing

Thursday, September 13, 2018 12:02 PM



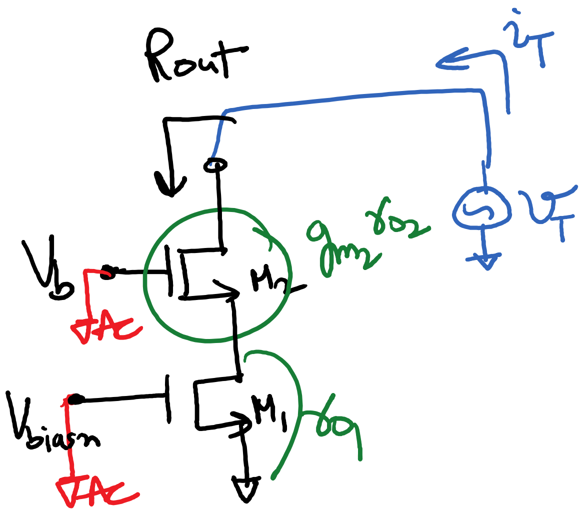
Common Gate amplifier
Grid

Common Source amplifier
Cathode

Cascode ⇒ Cascade of Common Cathode and common Grid amplifier

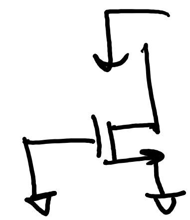
from the vacuum tube days.

Thursday, September 13, 2018 12:06 PM



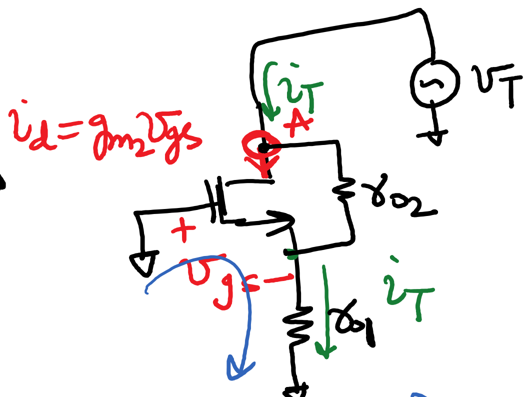
$R_{out} \triangleq \frac{v_T}{i_T}$

$R_{out} = r_o$



KVL: $v_{gs} + i_T r_{o1} = 0 \Rightarrow v_{gs} = -i_T r_{o1} \longrightarrow (1)$

KCL @ (A): $i_T - g_{m2} v_{gs} - \frac{(v_T - i_T r_{o1})}{r_{o2}} = 0 \longrightarrow (2)$



$$i_T + g_{m2} r_{o1} i_T - \frac{(v_T - i_T r_{o1})}{r_{o2}} = 0$$

$$i_T r_{o2} + g_{m2} r_{o1} r_{o2} i_T + i_T r_{o1} = v_T$$

$\Rightarrow$

$$\Rightarrow \frac{v_T}{i_T} = R_{out} = g_{m2} r_{o2} r_{o1} + r_{o1} + r_{o2}$$

$$R_{out} = (g_{m2} r_{o2}) r_{o1} + r_{o1} + r_{o2}$$

$$\simeq g_{m2} r_{o2} r_{o1} \simeq g_m r_o^2$$

$r_o \Rightarrow g_m r_o^2$

r_o $g_m r_o$

1kΩ $\longrightarrow$ 100kΩ

for $g_m r_o = 100$

$\simeq g_{m_2} r_{o_2} r_{o_1} \simeq g_m r_o$