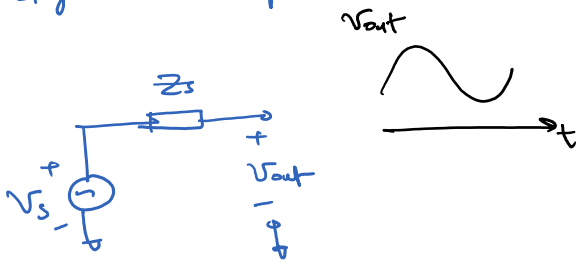
ECE 515 – Lecture 19

Tuesday, October 30, 2018 11:02 AM

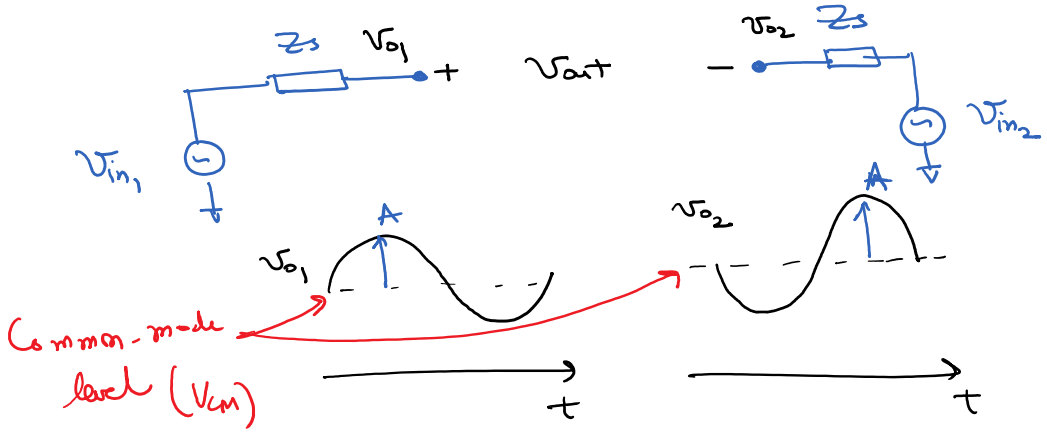
Differential Amplifiers

* Single-ended input



* Differential input

$v_{out} = v_{o1} - v_{o2}$

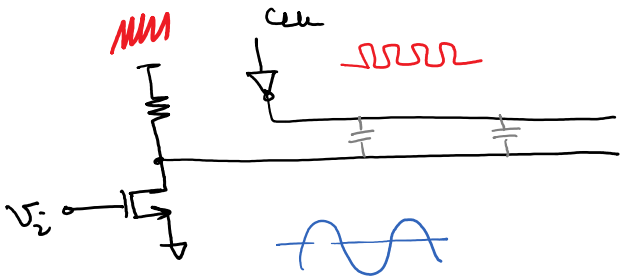


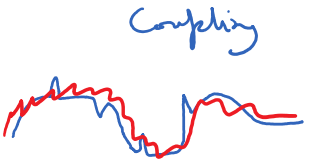
$V_{CM} = \frac{v_{o1} + v_{o2}}{2}$

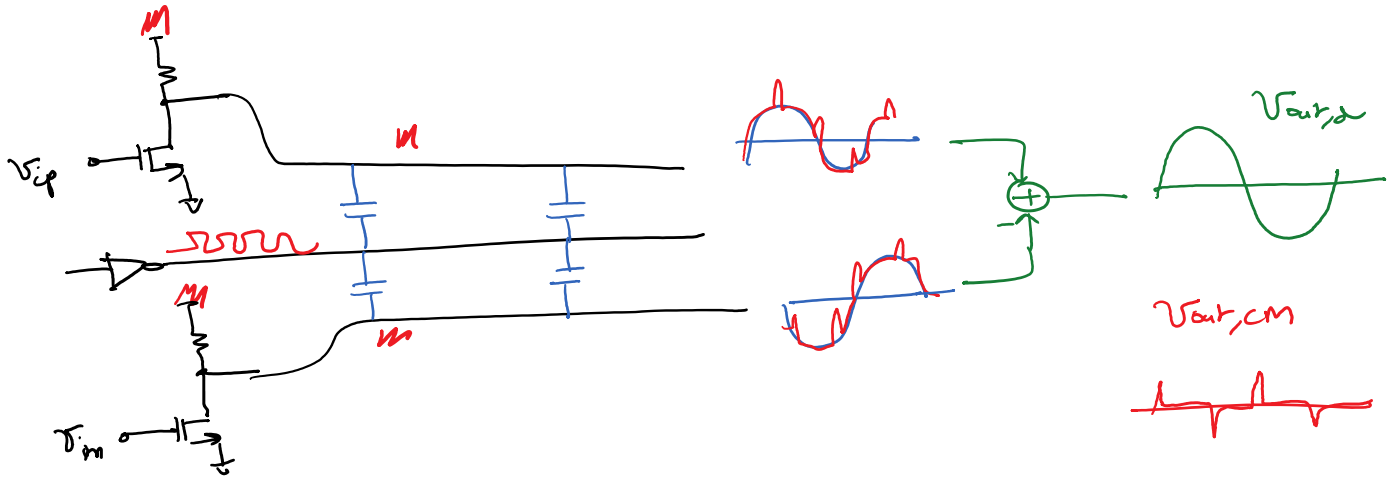
Differential signal, $v_d = (v_{s1} - v_{o2})$

* v_{o1} & v_{o2} (ideally) are equal and opposite (phase different of π)

Advantages of Differential Signaling:



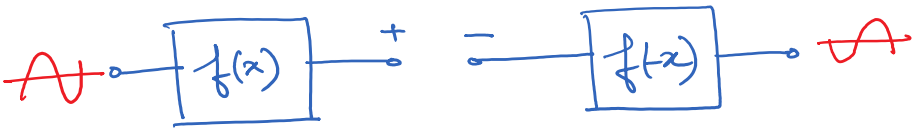




* Rejects any common-mode disturbance

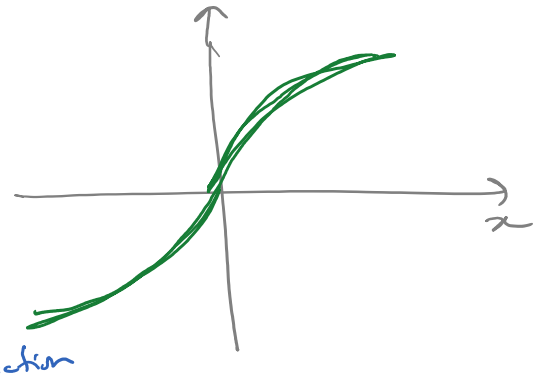
* Also improves linearity by (ideally) cancelling all even-order distortion

$x = v_{in}$



$$f_{odd}(x) = \frac{f(x) - f(-x)}{2}$$

↳ odd symmetry



$Sin(x)$ ⇒ odd function

$$f_{even}(x) = \frac{f(x) + f(-x)}{2}$$ ⇐ even symmetry

e.g. $\cos(x)$

$$f(x) = \alpha_0 + \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + \cdots$$

$$\frac{f(x) - f(-x)}{2} = \alpha_1 x + \alpha_3 x^3 + \alpha_5 x^5 + \cdots$$

* even-order distortion terms are eliminated

⇒ higher linearity.

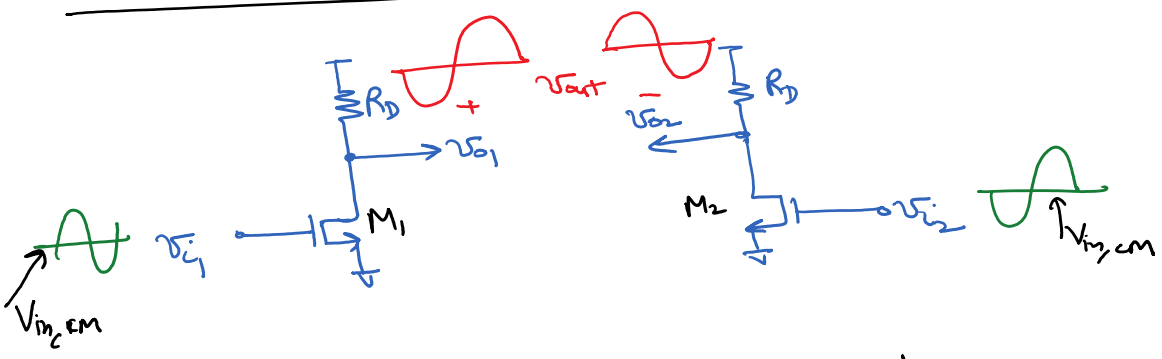
Signal level ⇒ 2X

noise P ⇒ $\sqrt{2}$X

⇒ SNR improvement $\sqrt{2}$X ⇒ 3dB

↳ 0.5 bit resolution in ADC

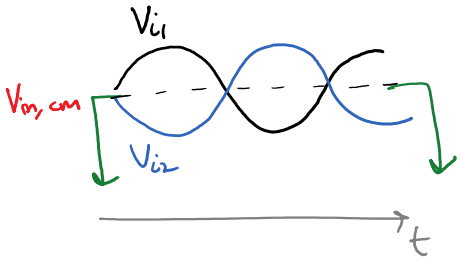
Basic Diff Pair :

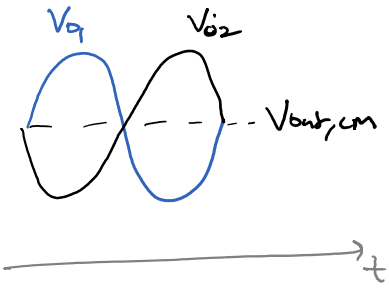


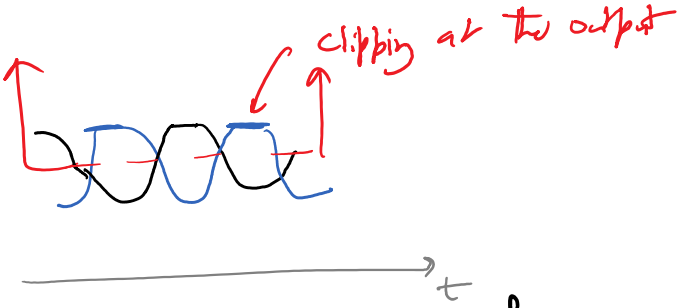
$v_{out} = v_{o1} - v_{o2}$

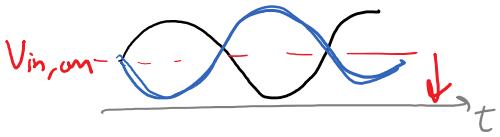
$v_{in} = v_{i1} - v_{i2}$

* What if the input CM-level changes

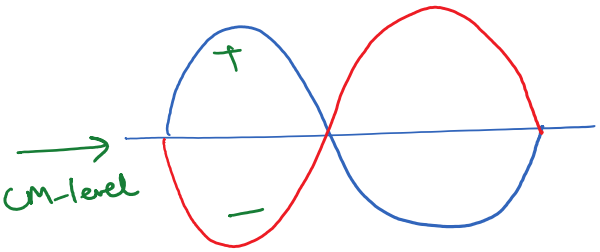


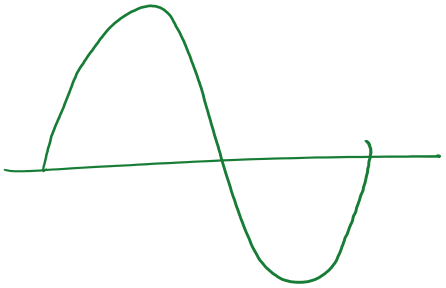


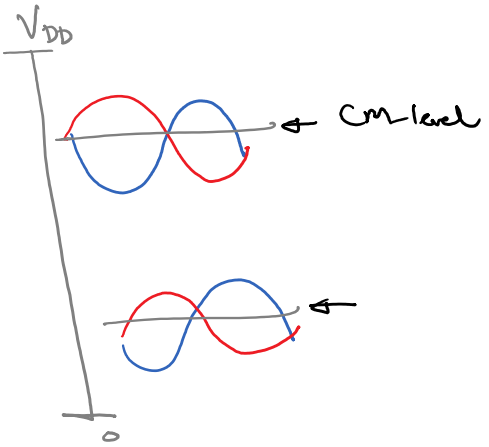




* Its important that the biasing of the transistors have a minimal dependance on the input CM-level.



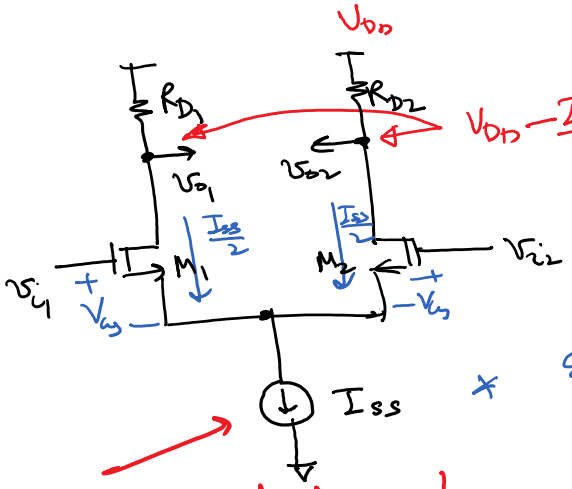




* Input CM-level is also important

Solution :

DC picture.



$V_{GS} = \sqrt{\frac{2 I_{D}}{\beta}} + V_{THN}$ ($I_D = I_{SS}/2$)

* Employs a current source to enforce $I_{SS} = I_{D1} + I_{D2}$
↳ this is independent of input CM-level

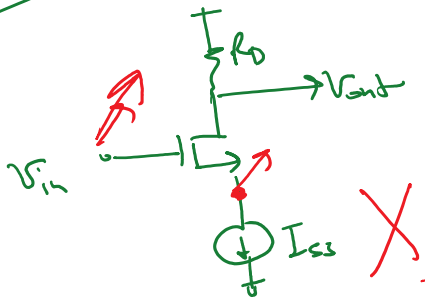
Biasing is performed by setting Iss

Dont need R_{big} & C_{big} to bias $M_{1/2}$

If $V_{i1} = V_{i2} \Rightarrow$ the bias current $I_{D1} = I_{D2} = \frac{I_{SS}}{2}$

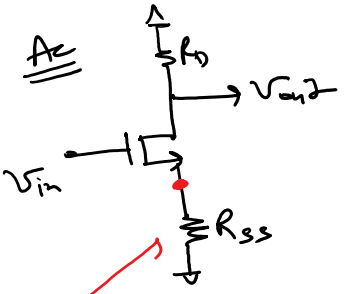
& output CM-level $\Rightarrow V_{DD} - \frac{I_{SS}}{2} \cdot R_D$ is well-defined

Question



$\Rightarrow$

Ac



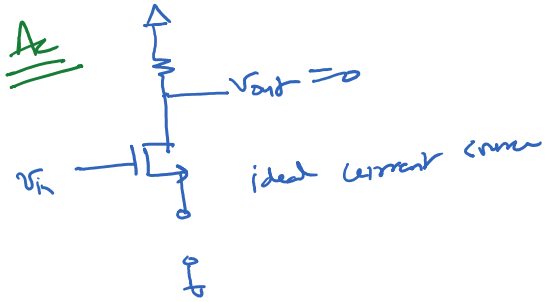
$A_v = -\frac{g_m}{1 + g_m R_{SS}} \cdot R_D$

output resistance of ISS.

$R_{SS} \to \infty$

$A_v = 0$

Ac



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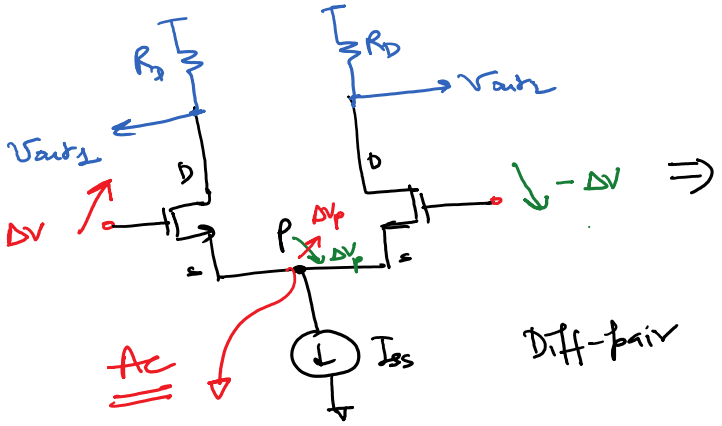
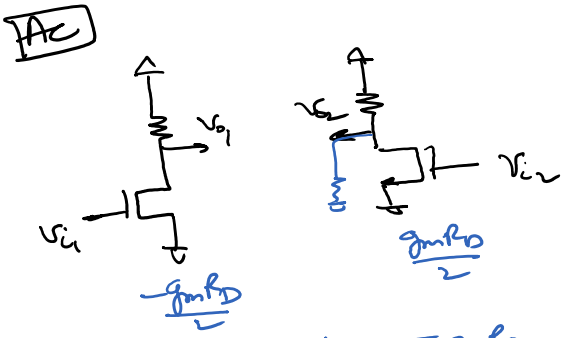


Diff-pair

P ⇒ Source-coupled node



$A_v = -g_mR_D$

Differential Half-pairs.

Common mode behavior of the Circuit:

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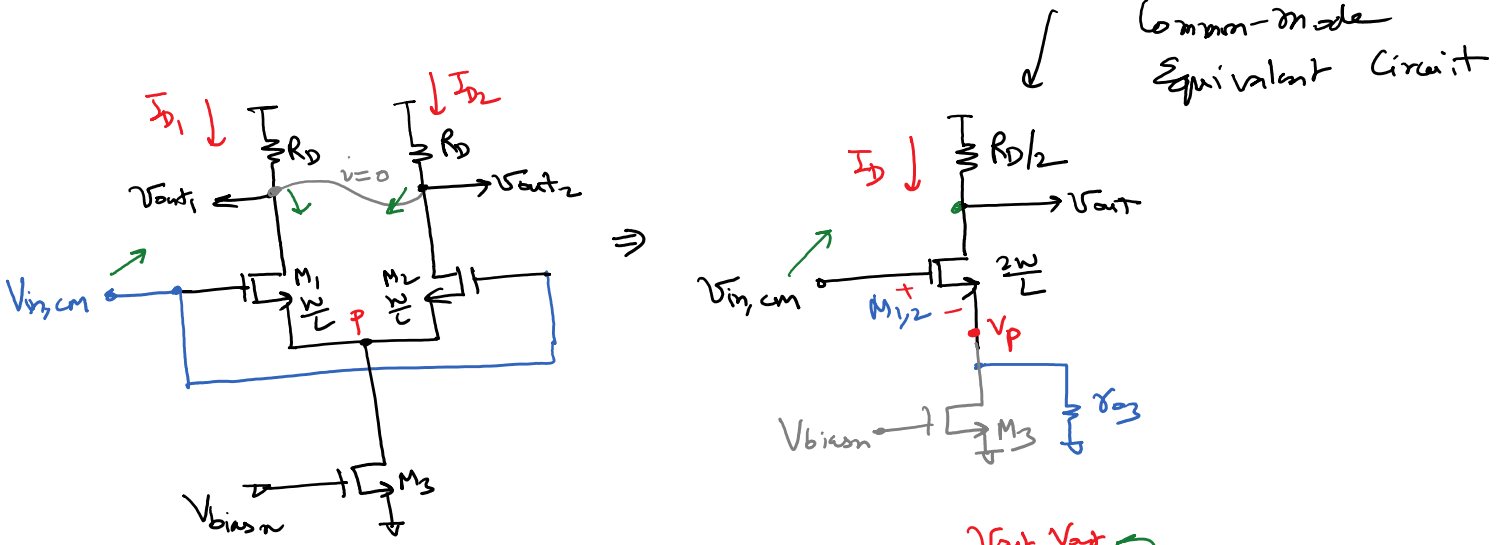

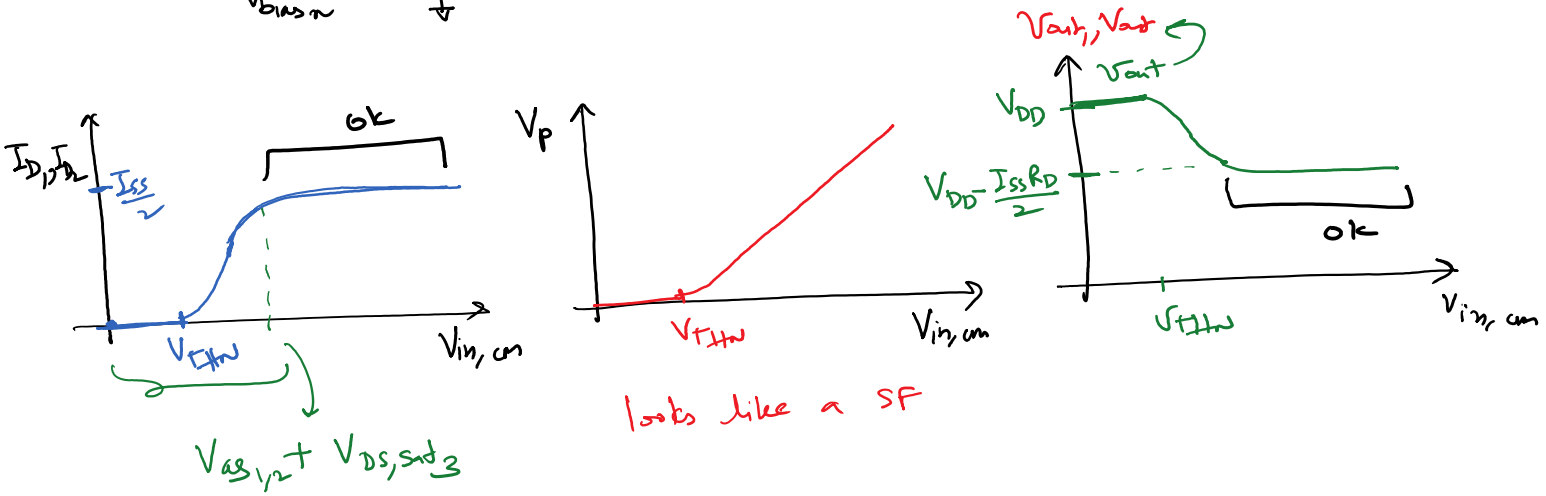

Input common-mode range (ICMR)

$$V_{in,cm} \geq V_{GS1,2} + V_{DS,sat3}$$

In general

$$V_{in,cm} \geq V_{GS1,2} + V_{SS}$$

V_{SS} → voltage needed to keep current source in Saturation

* Lets check for M_1 & M_2 entering Triode

$$V_{in,cm} \geq V_{out} + V_{THN}$$

$\because V_{DS} < V_{GS} - V_{THN}$

$\rightarrow V_D < V_G - V_{THN}$

$\rightarrow V_G > V_D + V_{THN}$

To keep $M_{1,2}$ in SAT

$$V_{in,cm} < V_{DD} - \frac{I_{SS}}{2}R_D + V_{THN}$$

$$V_{GS1,2} + V_{SS} \leq V_{in,cm} \leq \min\left\{V_{DD} - \frac{I_{SS}}{2}R_D + V_{THN},\ V_{DD}\right\}$$

V_1 — ICMR — V_2