ECE 415/515 –ANALOG INTEGRATED CIRCUIT DESIGN

SHORT CHANNEL BIASING

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LONG-CHANNEL CMOS, L_{MIN}=1UM

Table 9.1 Typical parameters for analog design using the *long-channel* CMOS process discussed in this book. Note that the parameters may change with temperature or drain-to-source voltage (e.g., Fig. 9.24).

Long-channel MOSFET parameters for general analog design *VDD* = 5 V and a scale factor of **1 μm** (*scale* = 1e–6)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	20 μA	20 μA	Approximate
W/L	10/2	30/2	Selected based on I_D and $V_{DS,sat}$
$V_{DS,sat}$ and $V_{SD,sat}$	250 mV	250 mV	For sizes listed
V_{GS} and V_{SG}	1.05 V	1.15 V	No body effect
V_{THN} and V_{THP}	800 mV	900 mV	Typical
$\partial V_{THN,P}/\partial T$	−1 mV/C°	−1.4 mV/C°	Change with temperature
KP_n and KP_p	120 μA/V^2	40 μA/V^2	t_{ox} = 200 Å
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	1.75 fF/μm^2	1.75 fF/μm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	35 fF	105 fF	PMOS is three times wider
C_{gsn} and C_{sgp}	23.3 fF	70 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	2 fF	6 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 μA/V	150 μA/V	At I_D = 20 μA
r_{on} and r_{op}	5 MΩ	4 MΩ	Approximate at I_D = 20 μA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	750 V/V	600 V/V	Open circuit gain
λ_n and λ_p	0.01 V^{-1}	0.0125 V^{-1}	At L = 2
f_{Tn} and f_{Tp}	900 MHz	300 MHz	For L =2, f_T goes up if L = 1

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SHORT-CHANNEL CMOS, L_{MIN}=50NM

Table 9.2 Typical parameters for analog design using the *short-channel* CMOS process discussed in this book. These parameters are valid only for the device sizes and currents listed.

Short-channel MOSFET parameters for general analog design *VDD* = 1 V and a scale factor of **50 nm** (*scale* = 50e–9)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	10 µA	10 µA	Approximate, see Fig. 9.31
W/L	50/2	100/2	Selected based on I_D and V_{ov}
Actual W/L	2.5µm/100nm	5µm/100nm	L_{min} is 50 nm
$V_{DS,sat}$ and $V_{SD,sat}$ V_{ovn} and V_{ovp}	50 mV 70 mV	50 mV 70 mV	However, see Fig. 9.32 and the associated discussion
V_{GS} and V_{SG}	350 mV	350 mV	No body effect
V_{THN} and V_{THP}	280 mV	280 mV	Typical
$\partial V_{THN,P}/\partial T$	– 0.6 mV/C°	– 0.6 mV/C°	Change with temperature
v_{satn} and v_{satp}	110 x 10^3 m/s	90 x 10^3 m/s	From the BSIM4 model
t_{ox}	14 Å	14 Å	Tunnel gate current, 5 A/cm^2
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	25 fF/µm^2	25 fF/µm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	6.25 fF	12.5 fF	PMOS is two times wider
C_{sgn} and C_{sgp}	4.17 fF	8.34 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	1.56 fF	3.7 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 µA/V	150 µA/V	At I_D = 10 µA
r_{on} and r_{op}	167 kΩ	333 kΩ	Approximate at I_D = 10 µA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	25 V/V	50 V/V	!!Open circuit gain!!
λ_n and λ_p	0.6 V^{-1}	0.3 V^{-1}	L = 2
f_{Tn} and f_{Tp}	6000 MHz	3000 MHz	Approximate at L = 2

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BMR CIRCUIT IN 1UM CMOS

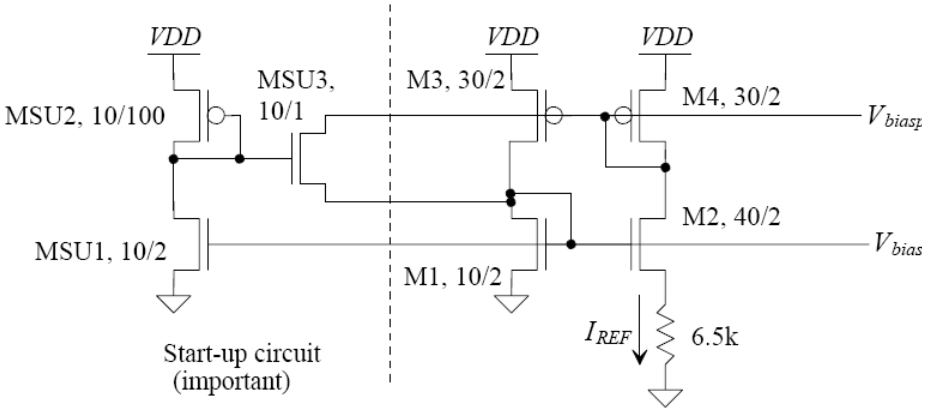

Figure 20.15 Beta-multiplier reference for biasing in the long-channel process described in Table 9.1.

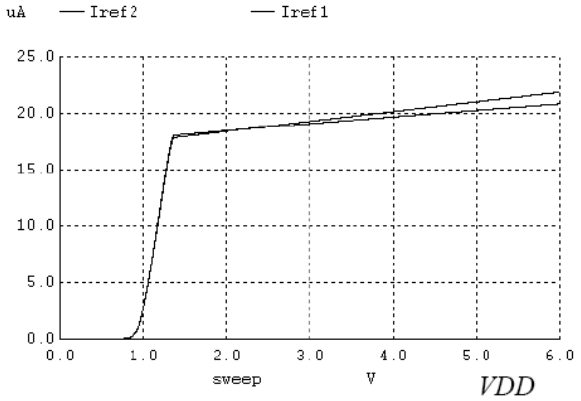

Figure 20.16 The reference currents through M1 and M2 in the Beta-multiplier.

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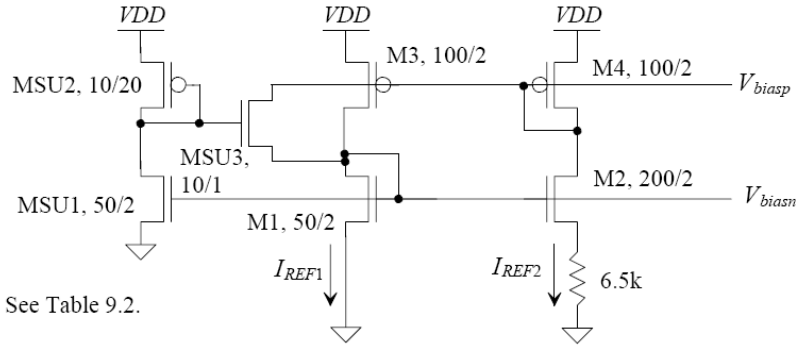
50NM BMR CIRCUIT



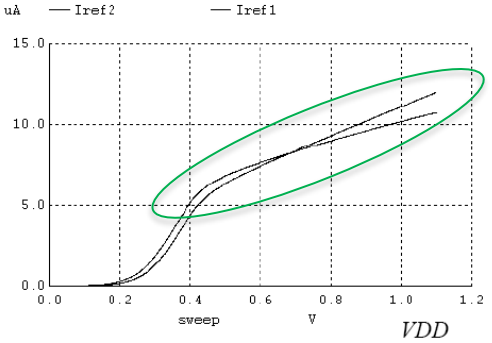


Figure 20.18 Beta-multiplier reference for short-channel design (see Table 9.2).

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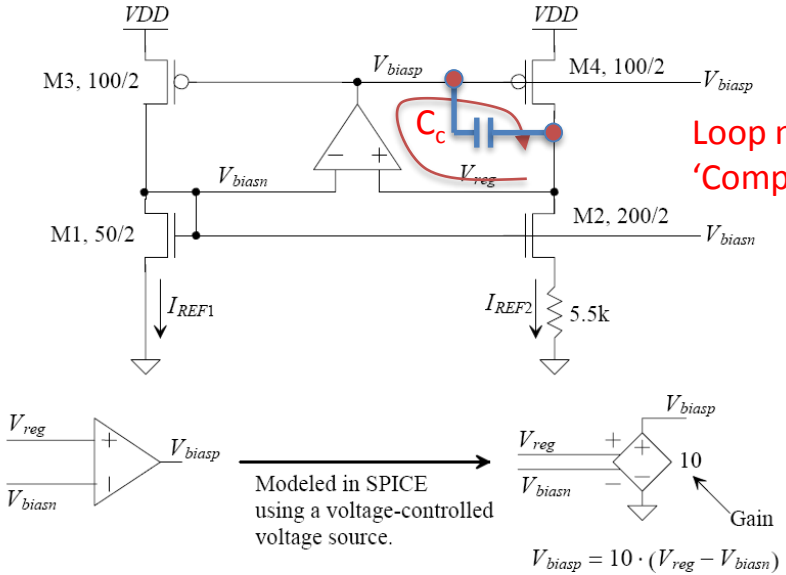
SHORT-CHANNEL BMR CIRCUIT



Loop needs to be 'Compensated'

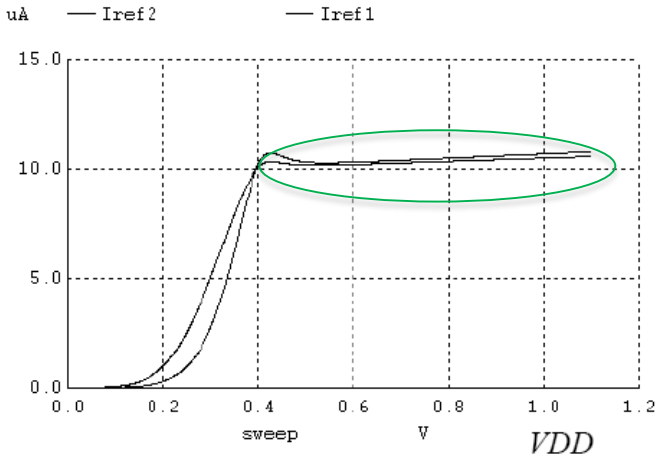


Figure 20.19 Increasing the output resistance of short-channel MOSFETs using feedback. The result, for the Beta-multiplier circuit, is better power supply sensitivity.

Figure 20.20 Improvement with the added amplifier.

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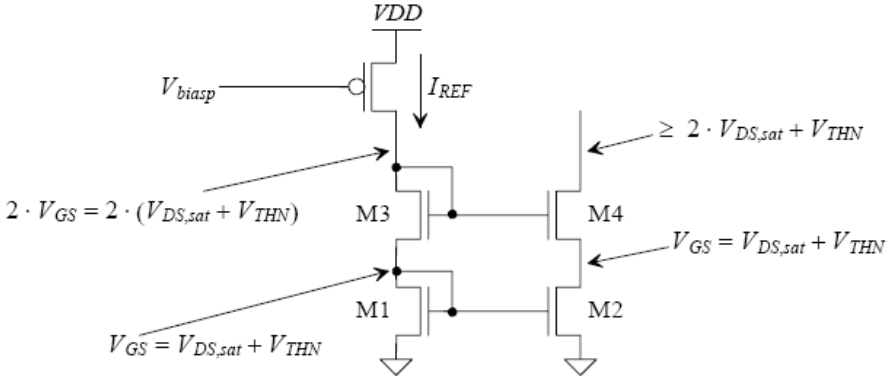
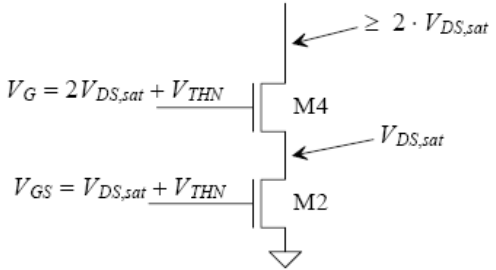
CASCODE CURRENT SOURCES



(a) Regular cascode structure



(b) Low-voltage (aka wide-swing) structure

Figure 20.31 DC voltages in (a) a cascode current mirror and in (b) a low-voltage cascode.

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WIDE-SWING CASCODE CURRENT SOURCES

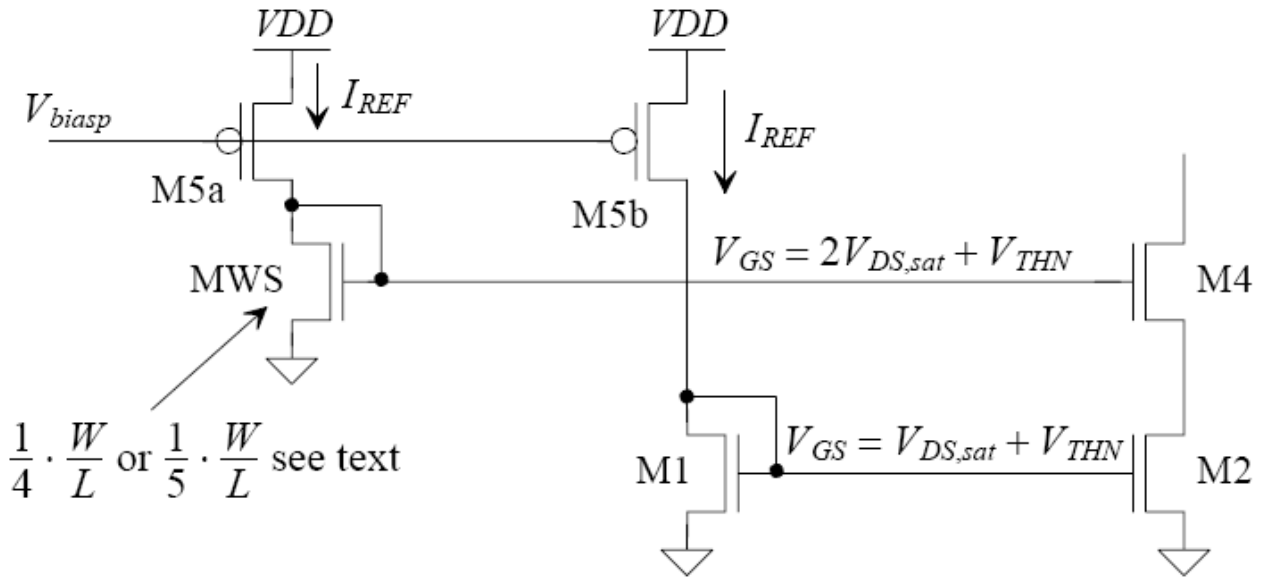

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Figure 20.32 Generating a bias voltage for M4.

WIDE-SWING CASCODE CURRENT SOURCES

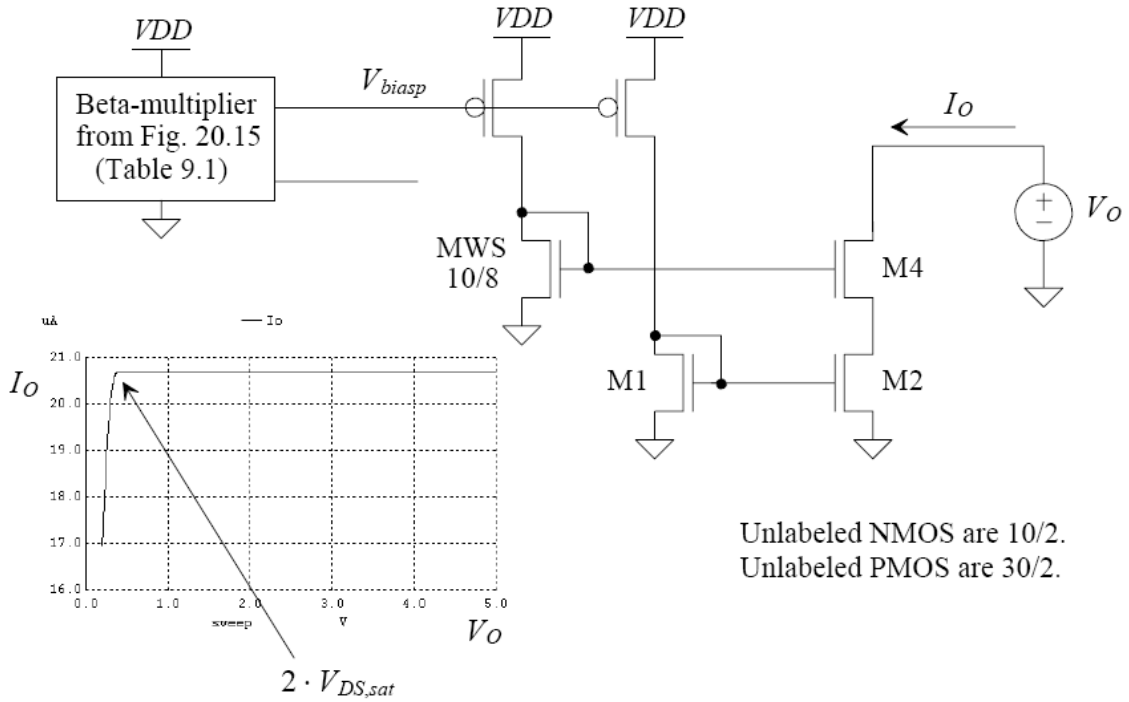

Figure 20.33 Wide-swing cascode current source in the long-channel process.

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LONG-CHANNEL BIAS CIRCUITS

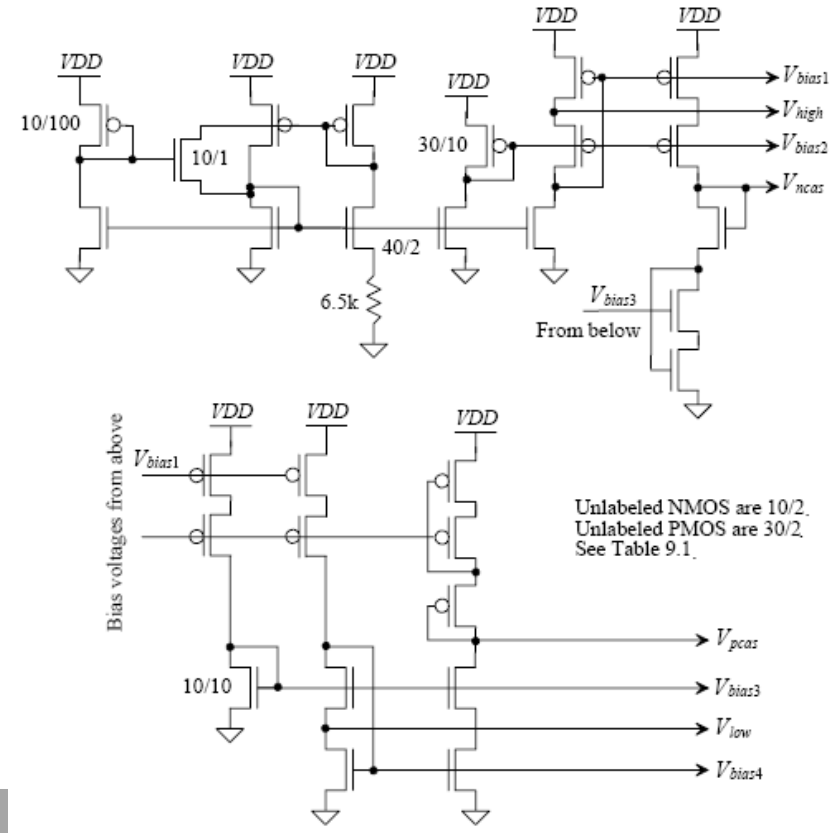

Figure 20.43 General biasing circuit for long-channel CMOS design using the data in Table 9.1

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SHORT-CHANNEL BIAS CIRCUITS

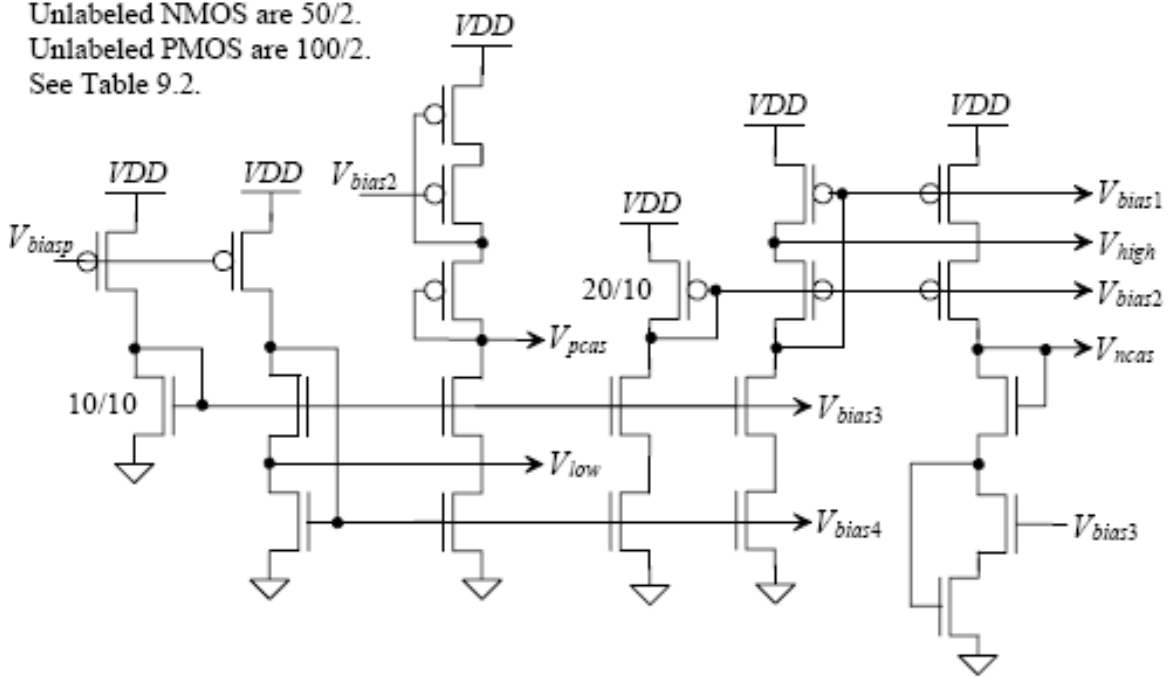

Figure 20.47 General biasing circuit for short-channel design using the data in Table 9.2.

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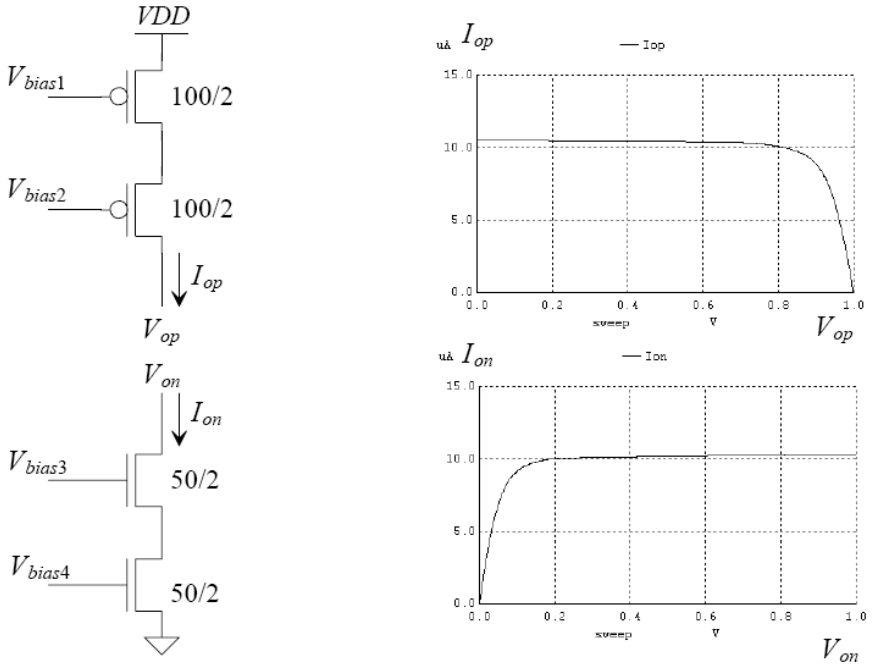
USING BIAS REFERENCES



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2).

Figure 20.48 Cascode current sources operating in a short-channel process.

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