# ECE 5/415 Analog Integrated Circuit Design
## Sample Midterm 1
## Oct 10, 2017

**Name:** Key

| |
|---|
| Closed Book, Closed Notes, Closed Computer.<br>Show your steps clearly to get credit.<br>State clearly any assumptions made.<br>This exam has 6 questions, for a total of 100 points. |

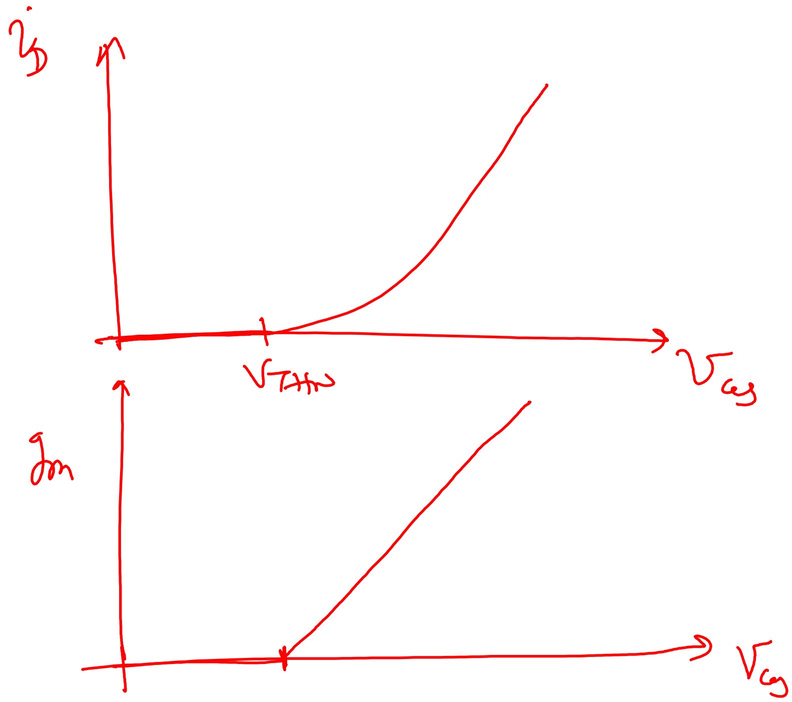
Use the following transistor parameters for problems in this exam. $V_{DD} = 5$V and scale factor of $1\mu m$.

| Parameter | NMOS | PMOS |
|---|---|---|
| $V_{THN,P}$ | 0.8 V | 0.9 V |
| $KP_{n,p}$ | 120 $\frac{\mu A}{V^2}$ | 40 $\frac{\mu A}{V^2}$ |
| $\lambda_{n,p}$ | 0.01 $V^{-1}$ | 0.0125 $V^{-1}$ |

1. Answer the following parts:

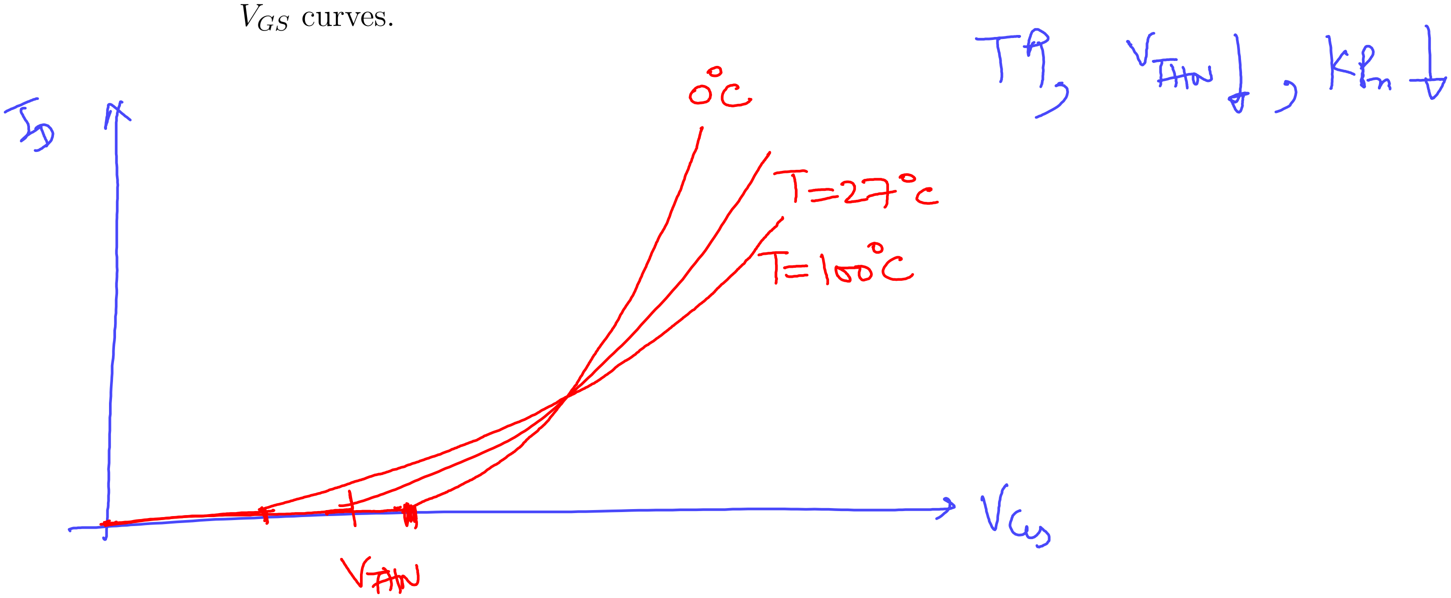
   (a) (5 points) For an NMOS, sketch $g_m$ vs $V_{GS}$ plot. On this plot, label the $g_m$ correspoding to a fixed gate overdrive voltage $V_{ov}$.

$$g_m = \frac{\partial i_D}{\partial v_{GS}}$$

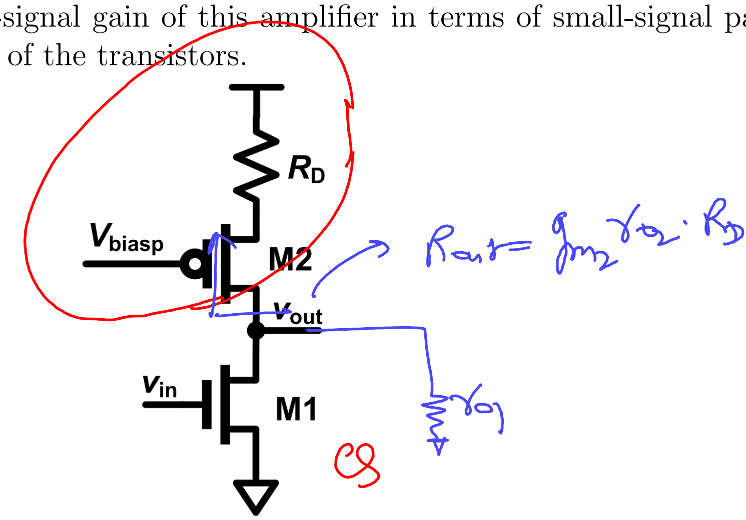



   (b) (5 points) Sketch $g_m$ as a function of current ($I_D$) when the $W/L$ ratio is constant.

(c) (5 points) Explain the temperature behavior of an NMOS transistor using $I_D$ vs $V_{GS}$ curves.

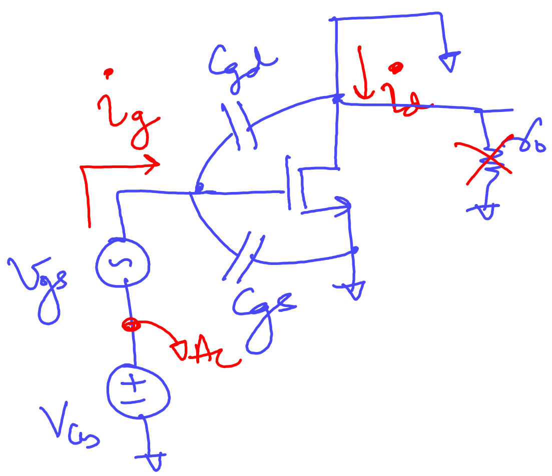



(d) (5 points) Find the small-signal gain of this amplifier in terms of small-signal parameters $g_{m1}$, $r_{o1}$, $g_{m2}$, $r_{o2}$ of the transistors.




$$A_v = -g_{m1}\left[r_{o1} \,\|\, (g_{m2} r_{o2} R_D)\right]$$

2. (10 points) Define the transition frequency ($f_T$) for an NMOS and derive an expression for $f_T$. How does $f_T$ depends on the channel length ($L$) and the gate overdrive voltage ($V_{ov}$)?




$$@\ f = f_T \qquad \left|\frac{i_d}{i_g}\right| = 1$$

$$i_g = \frac{v_{gs}}{\frac{1}{s(C_{gd}+C_{gs})}} = s(C_{gd}+C_{gs})v_{gs} \rightarrow (1)$$

$$i_d = g_m v_{gs} \rightarrow (2)$$

$$\frac{i_d}{i_g} = \frac{g_m v_{gs}}{s(C_{gd}+C_{gs})v_{gs}}$$

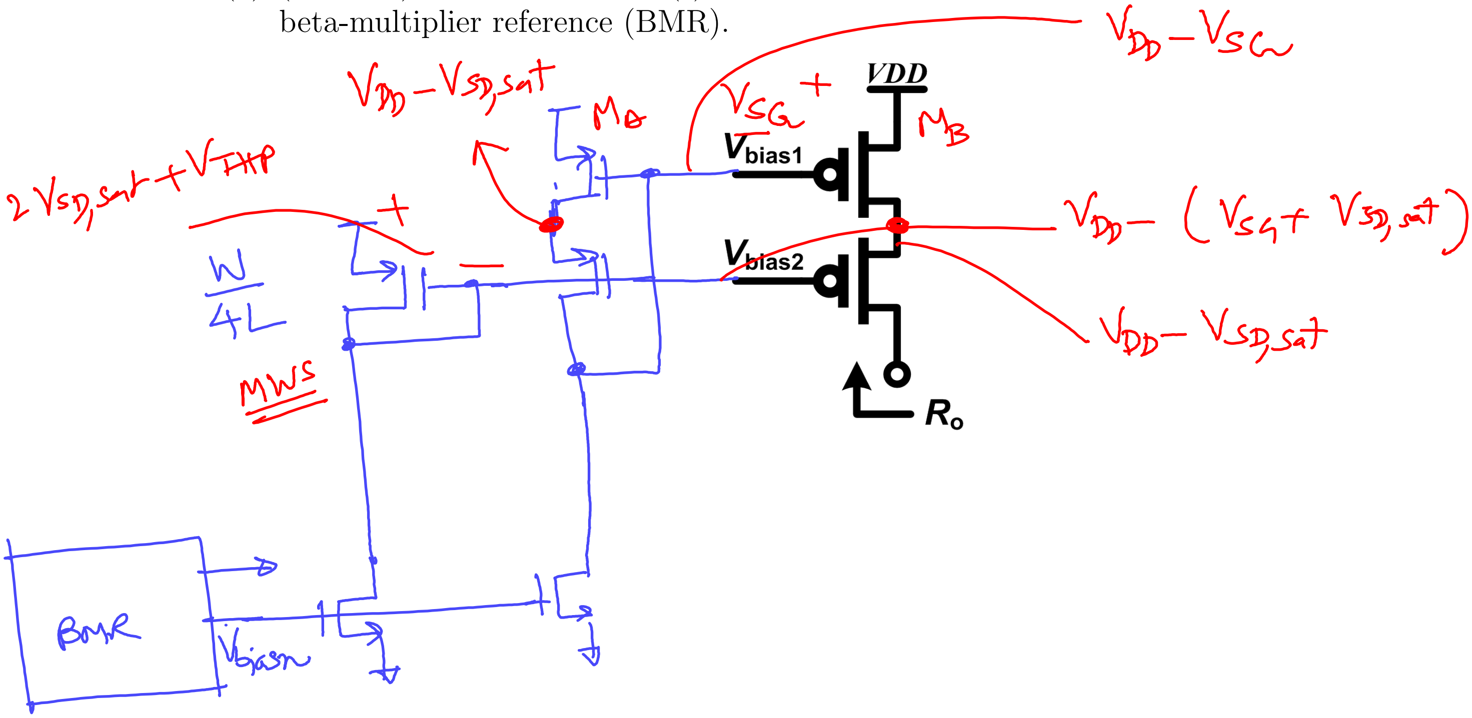
$$\left|\frac{i_d}{i_g}\right| = 1 \Rightarrow \frac{g_m}{2\pi f_T (C_{gs}+C_{gd})} = 1$$

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \simeq \frac{g_m}{2\pi C_{gs}}$$

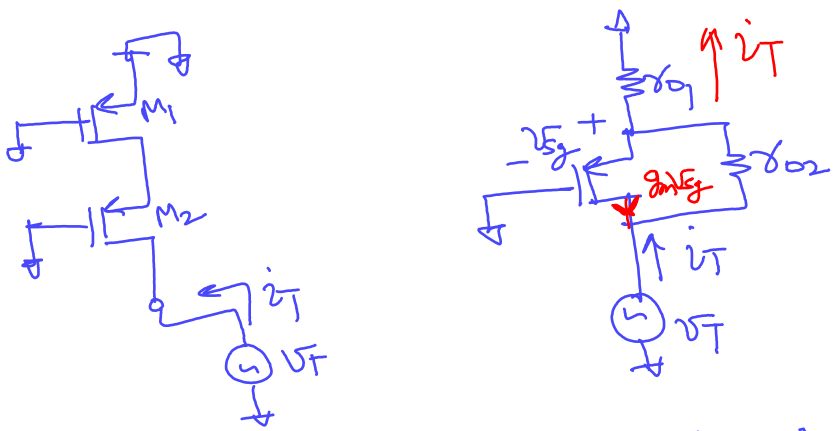
$$f_T \propto \frac{V_{ov}}{L^2} \quad \text{for long-channel}$$

$$\propto \frac{V_{ov}}{L} \quad \text{for short-channel}$$

3. (a) (5 points) Sketch the circuit(s) used to generate references $V_{bias1}$ and $V_{bias2}$ from a beta-multiplier reference (BMR).




(b) (5 points) Derive an exact expression for the output resistance of the cascode current source seen above.



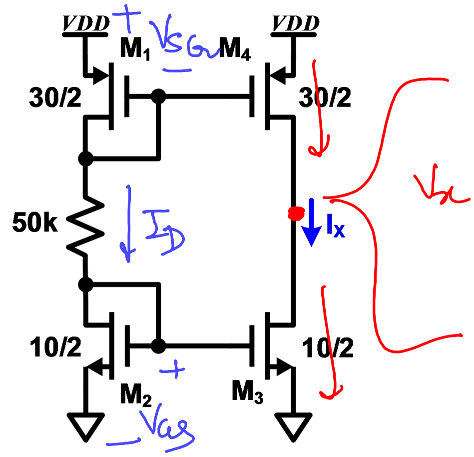

$$v_{sg} = + i_T r_{o1}$$

$$v_T = (i_T + g_{m2} v_{sg}) r_{o2} + i_T r_{o1}$$

$$= i_T [r_{o2} + g_{m2} r_{o2} r_{o1} + r_{o1}] \Rightarrow$$

$$R_{out} = \frac{v_T}{i_T} = g_{m2} r_{o2} r_{o1} + r_{o1} + r_{o2}$$

4. (20 points) Calculate all the DC voltages and currents in the circuit shown below.




$V_x$ & $I_x$ are undefined.

$$V_{DD} = V_{SG} + V_{GS} + I_D R$$

$$= \sqrt{\frac{2I_D}{\beta_p}} + |V_{THP}| + \sqrt{\frac{2I_D}{\beta_n}} + |V_{THN}| + I_D \cdot R$$

$$\Rightarrow \quad I_D \cdot R + \sqrt{I_D}\left(\sqrt{\frac{2}{\beta_p}} + \sqrt{\frac{2}{\beta_n}}\right) - \left(V_{DD} - V_{THN} - |V_{THP}|\right) = 0$$

Let $x = \sqrt{I_D}$

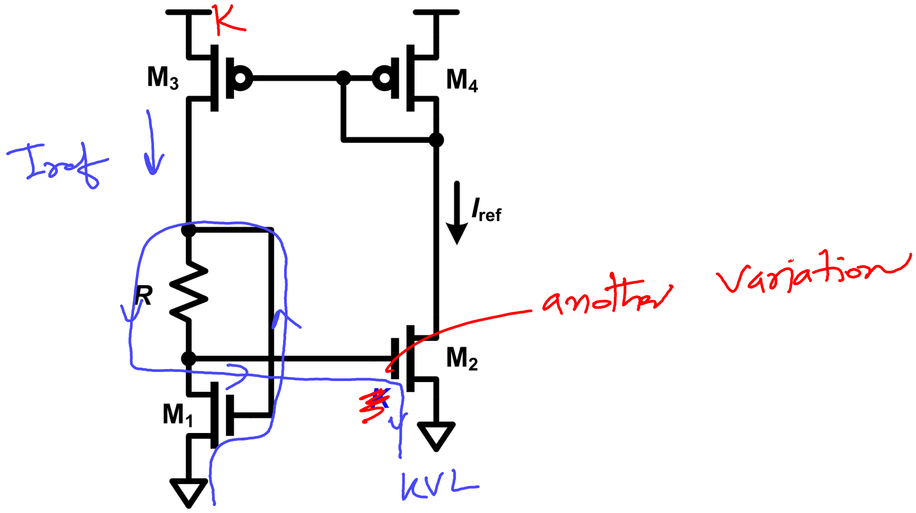
$$x^2 R + x\left(\sqrt{\frac{2}{\beta_p}} + \sqrt{\frac{2}{\beta_n}}\right) - \left(V_{DD} - V_{THN} - |V_{THP}|\right) = 0$$

Solve for $x = ?$

↓

$I_D = ?$

5. Consider the beta multiplier reference (BMR) circuit shown in the figure below.




(a) (10 points) Derive expressions for $I_{ref}$, $V_{GS_1}$ and $g_{m1}$. Note that M2 is $K$ times wider than M1.

(b) (5 points) Draw the schematic for a start-up circuit for this BMR.

(c) (5 points) Modify this circuit to make it suitable for short-channel design.

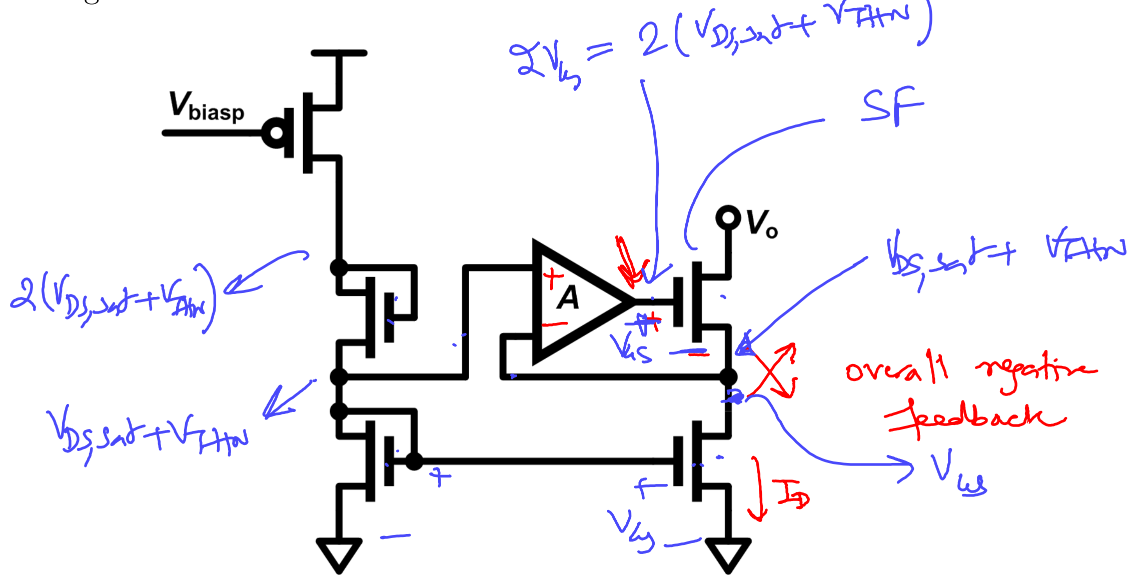
$$V_{GS_1} - I_{ref} R = V_{GS_2}$$

$$\sqrt{\frac{2I_{ref}}{\beta}} - I_{ref} \cdot R = \sqrt{\frac{2I_{ref}}{K\beta}}$$

$$\Rightarrow \sqrt{\frac{2I_{ref}}{\beta}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{ref} R$$

$$\Rightarrow I_{ref} = \begin{cases} 0 \\ \frac{2}{\beta R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \end{cases}$$

6. Consider the regulated drain current mirror shown below.

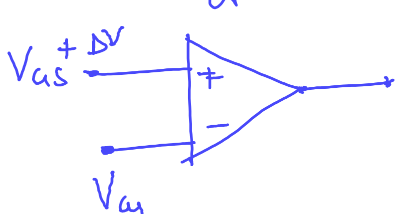



(a) (3 points) Assign the positive and negative terminals on the amplifier to ensure overall negative feedback.

(b) (7 points) Label all the nodes in the circuits in terms of $V_{DS,sat}$ and $V_{THN}$. What is the allowable range for the voltage $V_o$?

(c) (10 points) Derive an expression for the output resistance of this current mirror.

$A \to \infty$

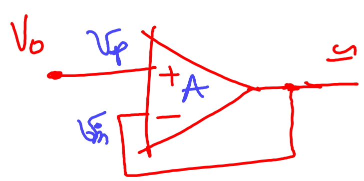



finite voltage $= A \cdot \Delta V \Rightarrow 2V_{GS}$

$\Delta V = \frac{2V_{GS}}{A} \to \epsilon \neq 0$

systematic offset

unity gain




$(V_p - V_m)A = V_{out}$

$(V_o - V_{out})A = V_{out}$

$V_p = V_m \Rightarrow V_o = A(V_p - V_m) \neq 0$

$\Rightarrow V_{out} = V_o \cdot \frac{A}{1+A} \simeq V_o\left(1 - \frac{1}{A}\right)$

(d) (0 points) **Bonus**: Sketch the PMOS and wide-swing version of this circuit.

$R_{out} = g_{m2} r_{o2} A r_{o1} + r_{o1} + r_{o2} \simeq g_m r_o^2 A$