MOSFET Short Channel Effects

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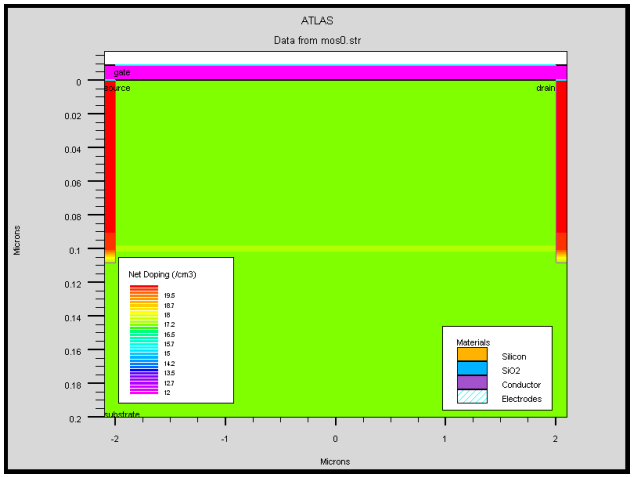
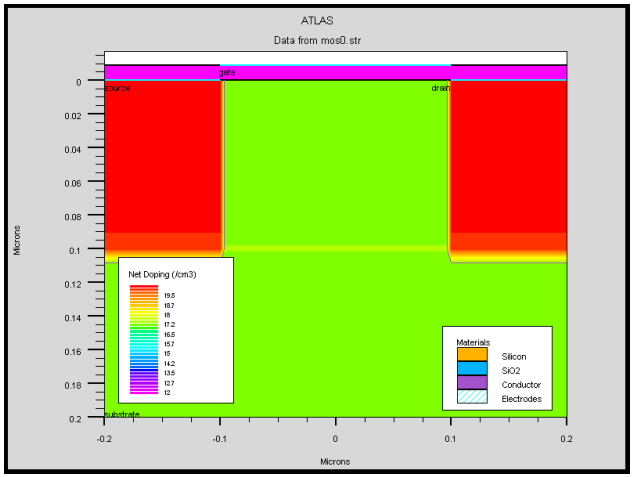
Short Channel MOSFETs

- MOSFETs with channel length (L) of the same order of magnitude as the drain/source region depths.
- Submicron MOSFETs (with $L < 1\,\mu m$) exhibit worsening short channel effects (SCE) as L is scaled down.



A long-channel NMOS (L=4μm)



A short-channel NMOS (L=0.2μm)

SC MOSFET Characteristics

- Due to the high electric fields in the channel region, the carriers in SC MOSFETs are velocity saturated (v_{sat})
- MOSFET current (I_D) in saturation exhibites somewhat linear relation to V_{GS}

$$I_D = W \cdot v_{sat} \cdot C'_{ox}(V_{GS} - V_{THN} - V_{DS,sat})$$

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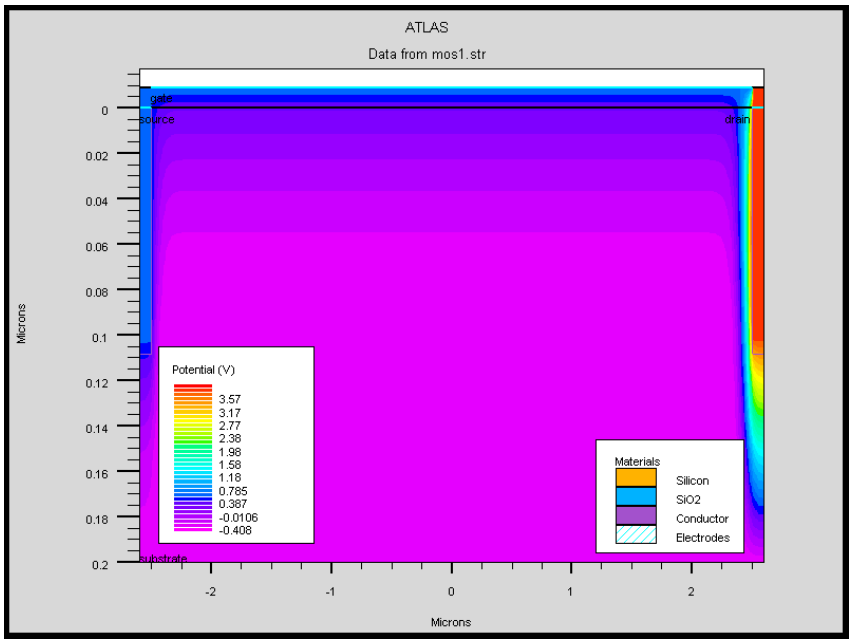
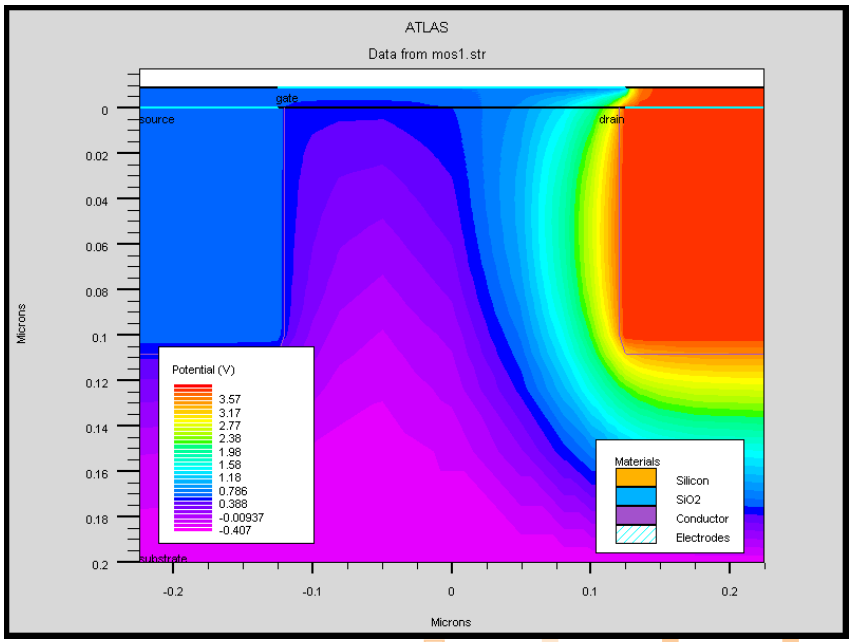
Potential Distribution in Short Channel MOSFETs

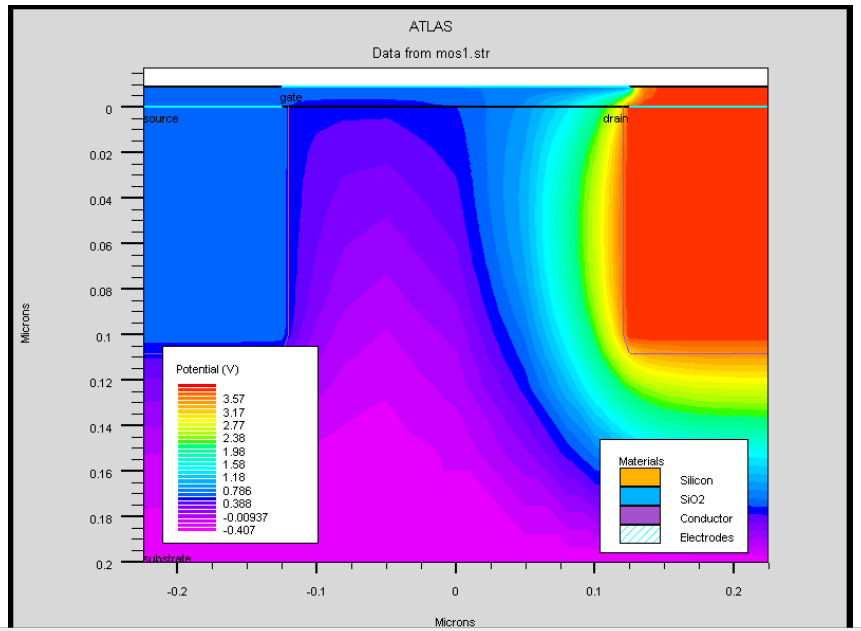
- In the short-channel device, the field and potential contours have a 2D spread while the long-channel device has relatively 1D potential distribution.
- Here, $V_{GS} = 0.1V$ and $V_{DS} = 3.3V$.





Drain Induced Barrier Lowering (DIBL)

- As seen in the constant potential contour plots, there is more surface potential (ψ_s) in the short channel MOSFET
  - more band bending near drain due to the drain field encroaching into the channel region
  - reduces V_{THN} when drain is biased at higher potential
- This is called drain induced barrier lowering (DIBL)



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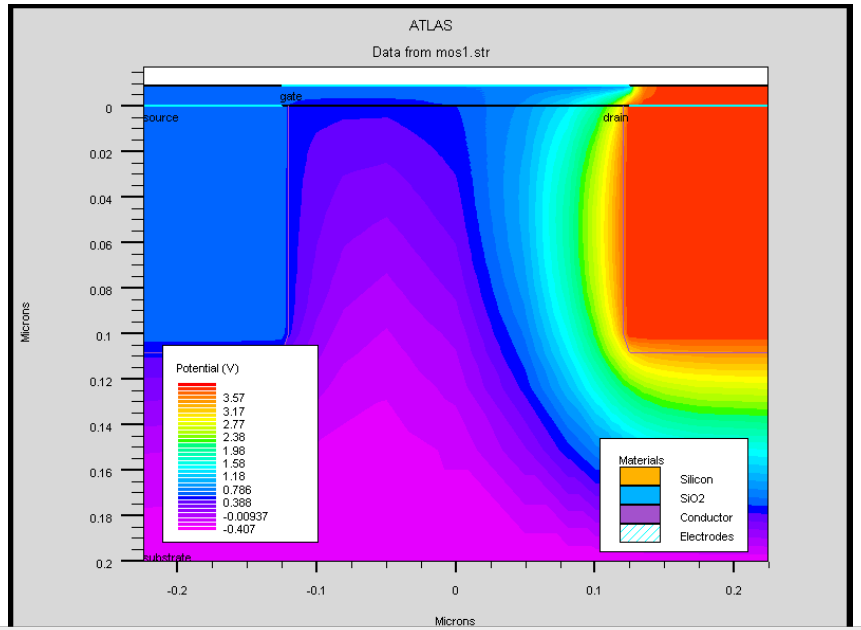
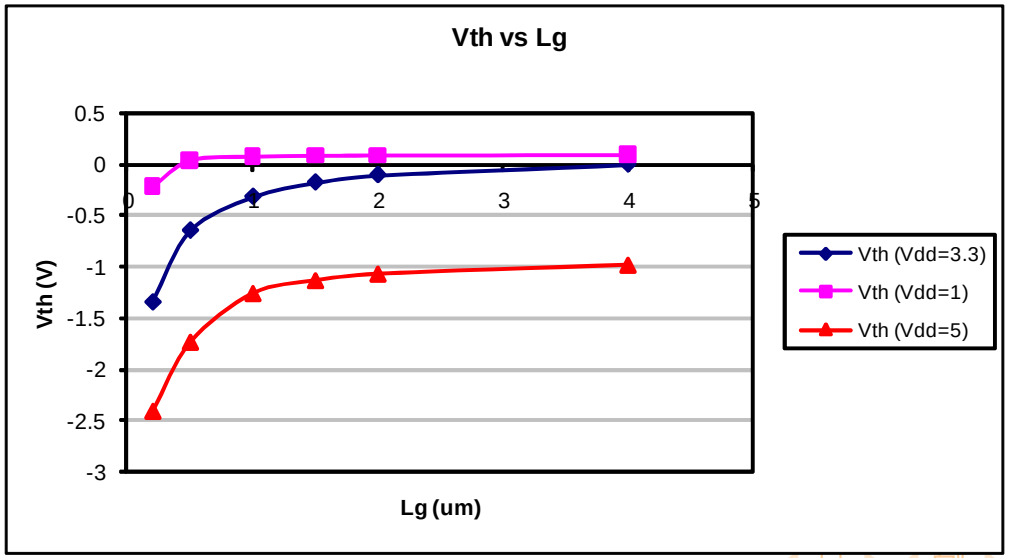


DIBL contd.

- The stronger electric field corresponding to a higher V_{DS}, penetrates deeper into the channel
  - causes more pronounced short channel effects.
- The V_{THN} roll-off slope is higher for a varying L at a higher V_{DS}
  - due to higher 2D electric field in the channel region.



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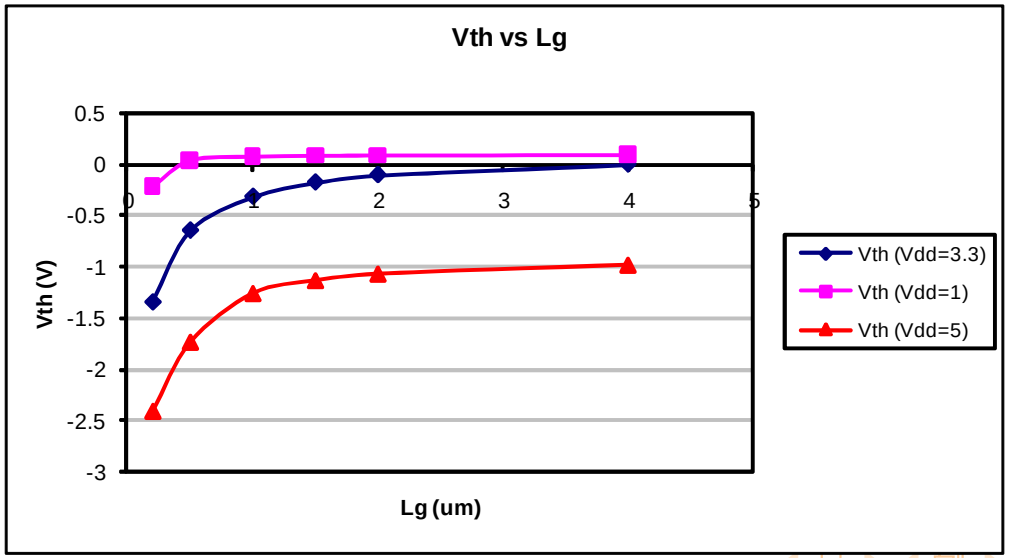

Hot Carrier Generation

- Carriers drifting near the drain can obtain nenergy much higher than the thermal energy of carriers
  - called *hot carriers*
- .The carriers reach velocity saturation (high velocity)
- Hot carriers can tunnel through the gate oxide causing degradation
  - can also cause impact ionization in MOSFETs.
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Lightly-Doped Drain (LDD)

- In CMOS, lightly doped drain (LDD) structure is used to reduce the effect of hot carriers and to reduce short channel effects
  - After Poly patterning an LDD implant is performed in the active regions
  - Afterwards, a nitride spacer is formed by depositing nitride and etching it
  - The nitride spacer acts as a hard mask for the subsequent implants and protects the LDD region
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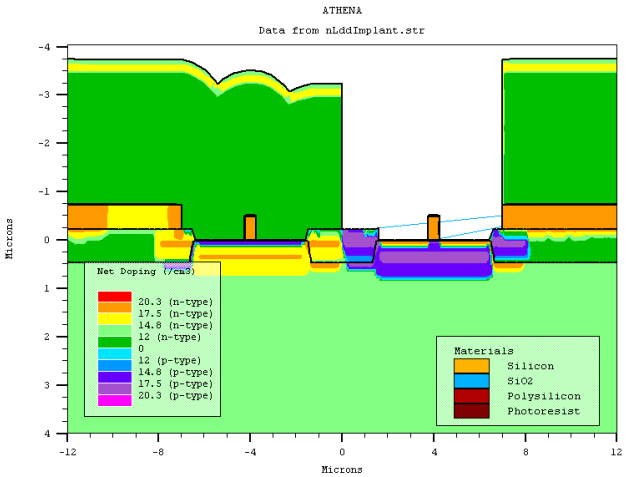
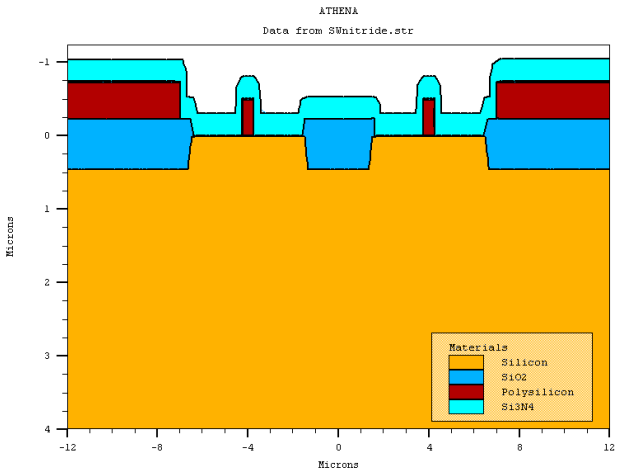
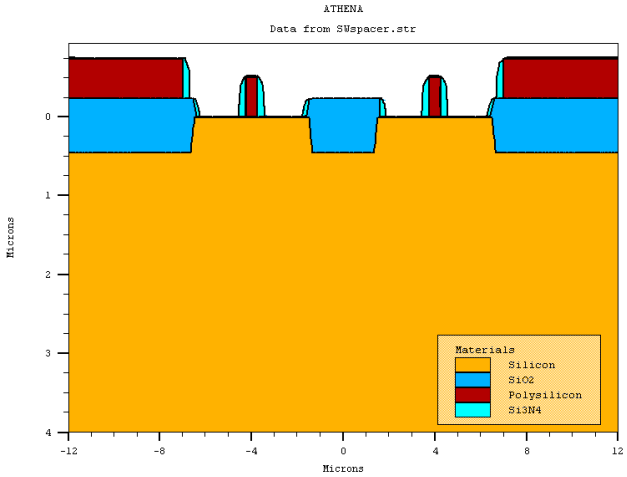


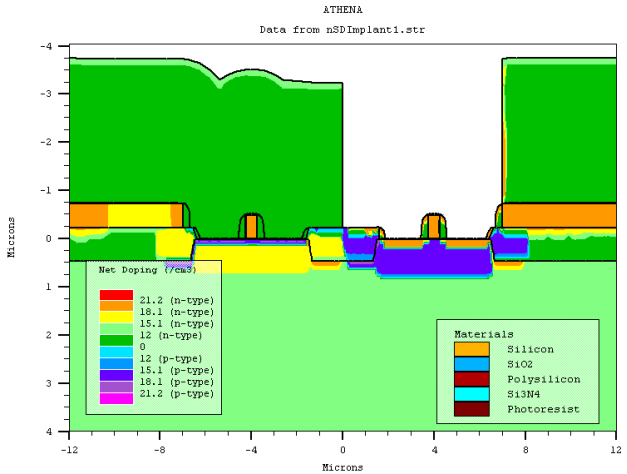
1) NMOS LDD implant



2) Nitride deposition



3) Nitride spacer formation



4) n+ source/drain implant

Oxide Breakdown

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Gate Tunnel Current

- As the oxide thickness (t_{ox}) scales down, the probability of carriers tunneling through the gate oxide increases
  - leads to gate leakage current
- Gate leakage current increases by an order of magnitude with every node scaling
  - major concern in VLSI design
- High dielectric (Hi-K) gate stacks are employed to increase C'_{ox} while keeping t_{ox} constant
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- Hot carriers can cause impact ionization near the drain
  - hole current is generated and flows through the substrate resistance
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Gate Induced Drain Leakage (GIDL)

- Occurs at higher drain biases in the off state of a transistor.
  - example, a DRAM cell with “1” stored on the capacitor and the gate is “0”
- Band-to-band tunnelling occurs at the drain and gate-oxide overlap region.
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