Final Project

ECE 5/415 — Analog IC Design

1 Problem Statement

Opamp Design: Signal processing applications such as Filters and ADCs require opamps with high performance and linearity. In this project students will design a **single-ended** opamp.

The opamps should meet the following specifications using TSMC 180-nm CMOS technology with a VDD=1.8 V supply voltage.

Table 1: Opamp design specifications.

Parameter	**Spec. for ECE 415**	**Spec. for ECE 515**
Technology	TSMC 180n CMOS	
Supply voltage, V_{DD}	1.8V	
Common-mode voltage, V_{CM}	0.9V	
Typical load	$100k\Omega \| \| 1pF$	$10k\Omega \| \| 2pF$
Unit gain frequency (f_{un})	$> 50\,MHz$	$> 50\,MHz$
Open-loop gain (A_{OL})	$> 60\,dB$	$> 60\,dB$
Slew-rate (SR)	$> 100\frac{V}{\mu s}$	
Phase margin (ϕ_M)	60°	
Power consumption	Minimum possible	

2 Opamp Design

In your opamp design consider the following criterion:

1. Explore the opamp design space and select an appropriate topology which will meet the given specifications. Explain your design choices and trade-offs, e.g. Telescopic *vs* Folded-cascode; single-stage *vs* two-stage; choice of compensation scheme, etc. *If you are not able to meet any of the specifications, explain giving justification.* You would want to have a class-AB output buffer to drive the given load with rail-to-rail output swing.

2. Characterize the process and explain the transistor size selection in your design. Clearly show/tabulate all the transistor sizes and the component values. Show the biasing circuits with appropriate simulations.

3. Perform stability (**STB**) analysis in Spectre using the ***iprobe*** and plot the open-loop AC response [1]. Label the PM and GM values and comment on closed-loop stability. This is important!

4. Simulate the single-ended opamp in unity-gain feedback with step input and comment on the transient stability. Characterize the design for small as well as large step inputs. Label your settling times. Do you see any slewing?

5. Characterize your design for all metrics including *rise and fall Slew-rates (SR^+ and SR^-), CMRR, PSRR*, power consumption using appropriate test bench schematics.

6. **PVT Characterization:** Simulate the behavior of your design for process corners (*tt,sf,fs,ss*), V_{DD}variations, and temperature range $0^\circ < T < 100^\circ C$.

3 Final Report

Submit your neatly typed report as a **PDF** file, preferably in IEEE two-column format[3]. Show neatly drawn schematics and block diagrams. You can download the Visio schematic symbols from the course website [2]. Provide relevant references in your report. Show the overall opamp performance in a neatly tabulated manner along with the conclusion.

4 Academic Honesty

You are expected to come up with your original designs. No circuits can be shared or copied from other student(s).

5 Grading Scheme

Design choices and justification 25%

Functionality and performance 30%

Design characterization and presentation of results 25%

PVT Analysis 10%

Report presentation and clarity 10%

References

[1] Loop Stability Analysis [Online].

[2] Visio Schematic Symbols. Available [Online].

[3] IEEE Transactions Templates. Available [Online].