Homework 5

ECE 5/415 – Analog IC Design

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.
2. Unless otherwise stated, use the following MOSFET parameters for hand-calculations. Use the $1\,\mu m$ CMOS models on the servers for corresponding simulations.

Table 1: Long-channel MOSFET parameters.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$1\,\mu m$	
V_{DD}	5 V	
V_{THN} and $\lvert V_{THP}\rvert$	0.8	0.9
KP_n and KP_p	120 $\frac{\mu A}{V^2}$	40 $\frac{\mu A}{V^2}$
Bias Current, I_D	$20\mu A$	$20\mu A$
g_{mn} and g_{mp}	$150\frac{\mu A}{V}$	$150\frac{\mu A}{V}$
$V_{ov} \cong \frac{2I_D}{g_m}$	250mV	250mV
W/L	10/2	30/2
V_{GS} and V_{SG}	1.05V	1.15V
r_{on} and r_{op}	$5M\Omega$	$4M\Omega$
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	1.75 $\frac{fF}{\mu m^2}$	
C_{oxn} and C_{oxp}	35 fF	105 fF
C_{gsn} and C_{sgp}	23.3 fF	70 fF
C_{gdn} and C_{dgp}	2 fF	6 fF
f_{Tn} and f_{Tp}	900 MHz	300 MHz

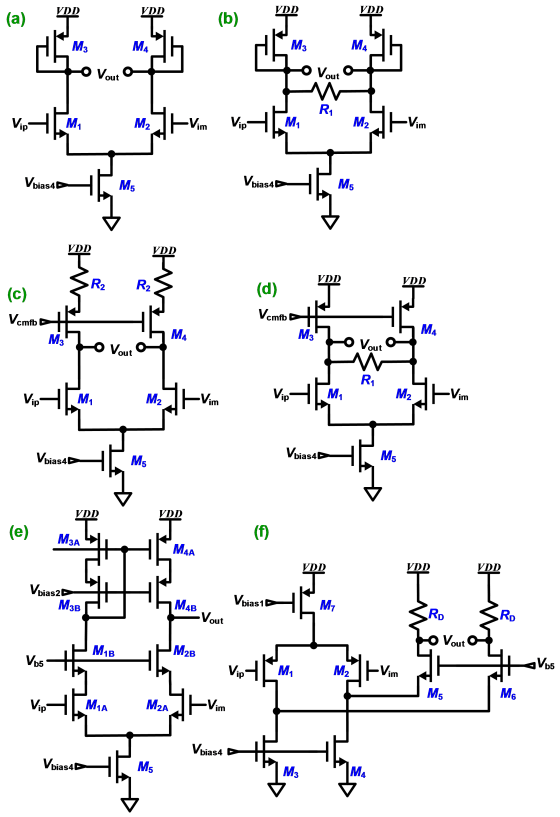

Figure 1

Problem 1: Calculate expressions for small-signal differential voltage gain ($A_{v,DM}$) for each of the circuits shown in Figure 1. Use variables g_{m1}, r_{o1}, g_{m2}, r_{o2}, etc. Here, $\lambda \neq 0$ and$\gamma = 0$. *No simulations are needed.*

Problem 2: Consider the diffential amplifiers (diffamps) shown in Figure 2. For each of these three amplifiers:

(a) Calculate DC voltage at all nodes, and the input common-mode range (ICMR).

(b) Estimate differential gain $A_{v,DM}$ (using *half-circuit analysis* as shown in class), common-mode gain $A_{v,CM}$ (using *common-mode equivalent circuit* analysis) at low-frequencies, and $CMRR$ in dB.

(c) Determine the frequency response $\frac{v_{out}}{v_{in}}(s)$ (perform numerical calculations pole-zero locations, and provide neatly hand-sketched Bode magnitude and phase responses). Find the unity-gain frequency (f_{un}), and phase-margin (Φ_M) for the amplifiers. *Note that* $f_{un} = \frac{\omega_{un}}{2\pi}$.

(d) Create schematics and compare Spectre DC and AC simulation results to hand-calculations for: A_{v0}, frequency response, CMRR.

(e) Plot v_{out} vs v_{in} characteristics by sweeping

the input. Mark ICMR on these plots.

You *need to put some thought into how to organize the test-benches. Create a symbol for your individual circuits and use heirarchical schematics for your simulation test-benches.*

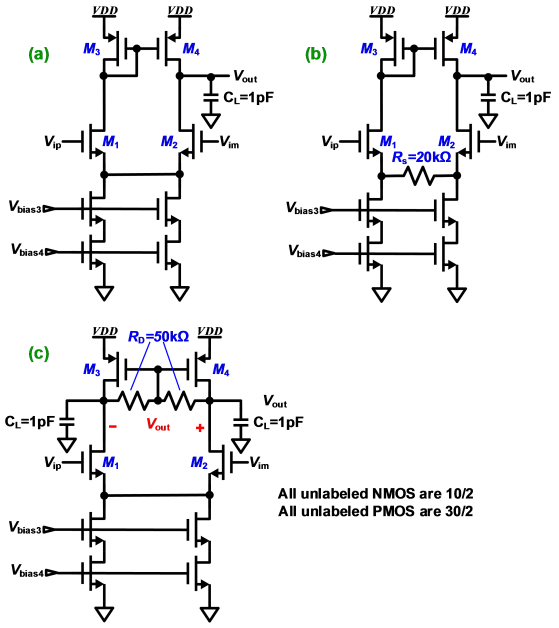

Figure 2