Homework 3

ECE 5/415 – Analog IC Design

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.

Problem 1: Consider the PMOS-version of the regulated drain current mirror shown in Fig 1.

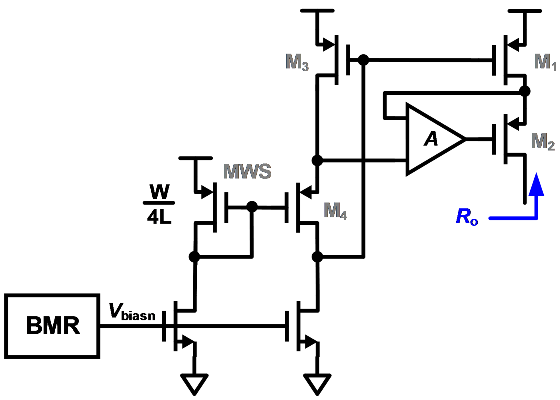

Figure 1

a) Assign the positive and negative input terminals for the error amplifier (A).

b) Find expressions (in terms of V_{THP}, $V_{SD,sat}$ and V_{DD}) for the DC levels all the nodes in the circuit.

c) Find an expression for the small-signal output resistance, R_o, of the current mirror in terms of g_{m1}, g_{m2}, r_{o1} etc.

d) What is the allowed swing across the current mirror to ensure all the transistors are in saturation?

Problem 2: The concept of cascoding can be further extended to realize a *triple-cascode* current mirror as shown in figure 2 below.

a) Assuming all devices to be identical, find an expression for the output resistance of this triple-cascode current mirror in terms of g_m and r_o.

b) What are the trade-offs involved if triple-cascoding is used in designs?

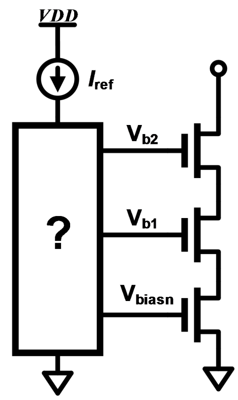

Figure 2

b) Given an ideal reference (I_{ref}) and using long-channel equations, design a wide-swing triple-cascode current mirror such that the minimum allowed output voltage is $3V_{DS,sat}$. Neatly sketch the schematics and the steps for calculating the sizes of the long-length devices used in the design. No need for simulations here.

Problem 3 - Process Characterization: Using the **180n CMOS** models:

a) Generate Table 1 below for an overdrive ($V_{OV} = V_{GS} - V_{THN}$) of 90mV. Use $L = 2 \cdot L_{min}$ and *state your assumptions.*
Show all the relevant simulation plots in a neatly organized manner, and save all your neatly created simulation test-benches for upcoming homeworks and project.

Table 1: Short-channel MOSFET general design parameters.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$0.18\,\mu m$	
V_{DD}	1.8 V	
V_{ov}	90 mV	90 mV
V_{THN} and V_{THP}		
V_{GS} and V_{SG}		
Bias Current, I_D	20 μA	20 μA
W/L		
$V_{DS,sat}$ and $V_{SD,sat}$		
g_{mn} and g_{mp}		
$\frac{g_{mn}}{I_D}$ and $\frac{g_{mp}}{I_D}$		
r_{on} and r_{op}		
$g_{mn} \cdot r_{on}$ and $g_{mp} \cdot r_{op}$		
$C_{gg,n}$ and $C_{gg,p}$		
$C_{gs,n}$ and $C_{sg,p}$		
$C_{gd,n}$ and $C_{dg,p}$		
$f_{T,n}$ and $f_{T,p}$		

b) For the NMOS and PMOS devices in your table, plot f_T, $g_m r_o$, $\frac{g_m}{I_D}$, and $\left(\frac{g_m}{I_D}\right)^{-1}$ as function of overdrive (V_{OV}). Interpret each of these graphs.

Problem 4 - BMR Design: This problem deals with the practical considerations for constant-g_m bias (aka BMR) circuit design. Using the **180 nm CMOS** process and the characterization data from Problem 3:

a) Design and simulate a constant-g_m bias circuit shown in Figure 3 (a), along with a start-up circuit. Plot the currents in the BMR when V_{DD} is swept. Comment on the supply sensitivity of the circuit.

b) In practice, on-chip resistance varies by ±20% and thus an external precision resistance may be used for setting the bias current as shown in Figure 3 (b). However, the bond-pad introduces a parasitic capacitance (say $C_p = 200\,fF$. This necessitates a compensation capacitance C_c to stabilitize the circuit. Modify your circuit from part (a) by including the bond-pad parasitic cap and stabilize the circuit using appropriate value of C_c (using hit-and-trial at this point).

c) Repeat part (a), by using an ideal amplifier model (use controlled-source model) to regulate the drain voltages of the bottom NMOS devices as shown in Figure 3 (c). Note that, later on when using transistor-level amplifier, the loop will need to be compensated.

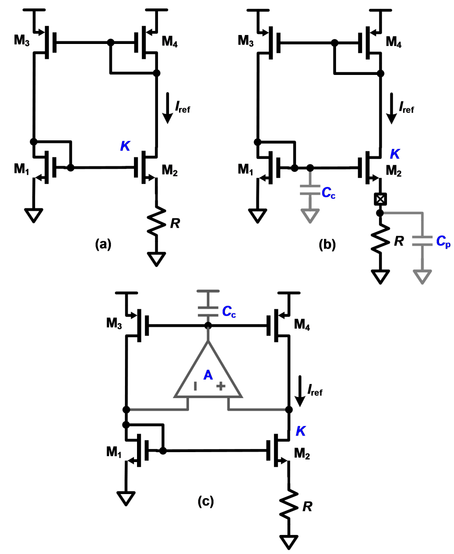

Figure 3