Homework 2

ECE 5/415 — Analog IC Design

Note:

1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.
2. Unless otherwise stated, use the following MOSFET parameters for hand calculations. Use the $1\,\mu m$ CMOS models on the servers for corresponding simulations.

Table 1: Long-channel MOSFET parameters.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$1\,\mu m$	
V_{DD}	5 V	
V_{THN} and V_{THP}	0.8	0.9
KP_n and KP_p	120 $\frac{\mu A}{V^2}$	40 $\frac{\mu A}{V^2}$
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	1.75 $\frac{fF}{\mu m^2}$	

Problem 1:

1. Calculate the currents and voltages in the circuit in Fig. 1 (a). What is the maximum value allowed for R_2 so that M_2 remains operating in the saturation region? Verify results with simulation.

2. Sketch I_x vs V_x for the circuit shown in Fig. 1 (b).

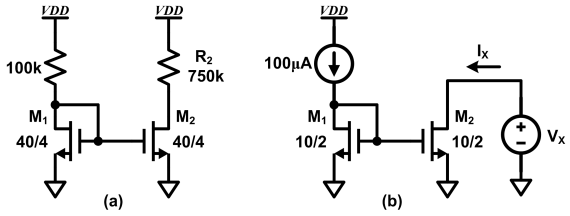

Figure 1

Problem 2: Estimate the current I_X flowing in circuits shown in Fig. 2. Verify results with simulations.

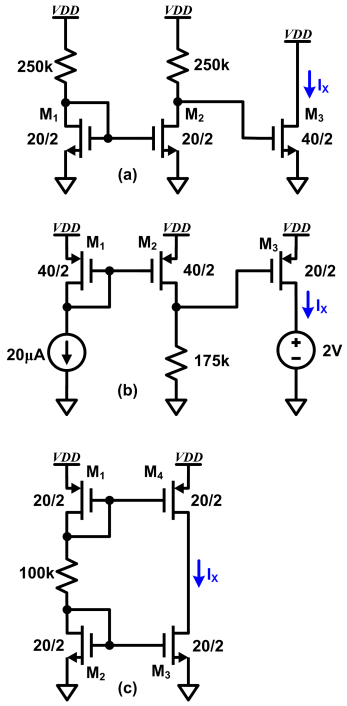

Figure 2

Problem 3: The beta-multiplier references (BMR) are used for constant-g_m biasing, where the goal is to stabilize the transconductance of a transistor. For example, in Fig. 3 (a), the g_m of M1 will be 'copied' to a current mirror device (not shown here).

a) Derive expressions for I_{ref}, V_{GS_1} and g_{m1} in Fig. 3 (a). Note that M3 is K times wider than M4 and M1 and M2 are the same size. Draw the schematic for a start-up circuit for this BMR.

b) Will the circuit shown in Fig. 3 (b) work as a constant-g_m reference? Explain.

c) Fig. 3 (c) shows a fix for the body effect problem in the bottom NMOS in the BMR. Derive an equation for I_{ref} in this circuit. Run a temperature sweep on I_{ref} and compare it with the results from the BMR seen in class. Explain your observations.

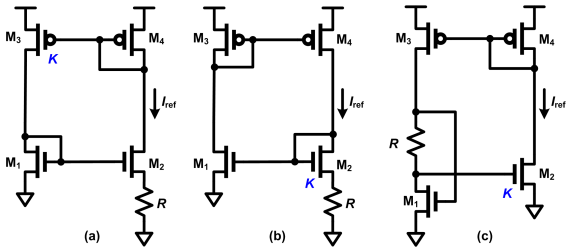

Figure 3