Homework 1

ECE 5/415 — Analog IC Design

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.
2. Unless otherwise stated, use the following MOSFET parameters for hand calculations. Use the $1\,\mu m$ CMOS models on the servers for corresponding simulations.

Table 1: Long-channel MOSFET parameters.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$1\,\mu m$	
V_{DD}	5 V	
V_{THN} and V_{THP}	0.8	0.9
KP_n and KP_p	120 $\frac{\mu A}{V^2}$	40 $\frac{\mu A}{V^2}$
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	1.75 $\frac{fF}{\mu m^2}$	

Problem 1: For the circuit shown in Figure 1, sketch I_x as V_x varies from 0 to $V_{DD} = 5\,V$. Not required, but feel free to verify using simulations.

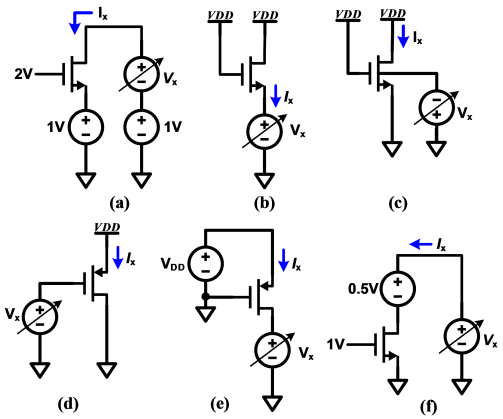

Figure 1

Problem 2: Using square law equations for a MOSFET, determine the DC voltage, V_x, in each of the circuits shown in Figure 2. Verify your calculations with simulations.

Problem 3: Use the **180nm CMOS** Spectre models for this problem. Note that for this process: $L_{min} = 0.18\mu m$ and $V_{DD} = 1.8V$.

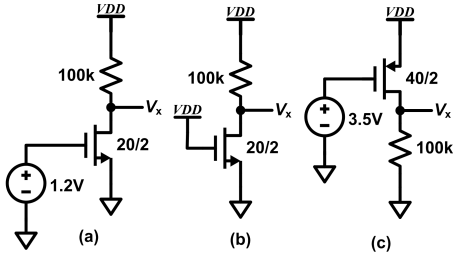

Figure 2

1. Generate all the I-V curves (i.e. I_D vs V_{GS}, V_{DS} and V_{SB}) for a 10/1 NMOS.
2. Generate all the I-V curves (i.e. I_D vs V_{SG}, V_{SD} and V_{BS}) for a 10/1 PMOS.
3. Do you expect long-channel or short-channel behavior from these devices?