ECE 515/415: Analog IC Design
Fall 2017, University of Idaho

Course Site : http://lumerink.com/courses/ece517/s17/ECE517.htm

Instructor	: Vishal Saxena
Meeting Time	: Tue & Thu 11:00 AM - 12:15 PM
Course dates	: Aug 22 - Dec 12, 2017
Location	: JEB 21
Office	: BEL 318
Office hours	: Tue & Thu 12:30 PM-1:30 PM, or by appointment

Course Site: http://lumerink.com/courses/ece515/f17/ECE515.htm

Course content – CMOS transistor models, advanced current mirrors and biasing, review of amplifiers. Opamps: frequency compensation, negative feedback and stability, half circuit analysis. Voltage references (bandgap reference) and regulators. Fully-differential Opamp design and simulation. Noise, mismatch, and distortion in analog circuits. Analog layout considerations.

Prerequisites – ECE 410 or permission.

Expectations – The course will build upon material covered in the prerequisite ECE 410, where CMOS amplifier design and frequency response was covered. Familiarity with schematic capture and Spectre simulation is assumed. Students are encouraged to review Cadence usage using videos tutorials linked from the course site.

Textbook – Design of Analog CMOS Integrated Circuits, B. Razavi, McGraw-Hill, 2002.
Additional Reference – CMOS Circuit Design, Layout and Simulation – R. J. Baker, 3nd Edition, Wiley-IEEE, 2010
For detailed references and handouts see course site.

Workload (Grading)
25% Homeworks
20% Midterm Exam 1
20% Midterm Exam 2
20% Project 1
20% Final Exam

This grading scale is for both ECE415 and ECE515 students. Students are required to write their project reports in provided IEEE Transaction format. Microsoft Word Templates will be available at the class web site for Project report. Using these templates will be mandatory.

Make-Up Policies
Only students presenting medical or official university excuses to the instructor will be allowed to take a make-up exam or other missed assignments. Whenever possible, arrangements should be made with the instructor prior to the regularly scheduled exam or assignment due date.

Making these arrangements is entirely the responsibility of the student. Make up exams or other assignments may differ from those given at the regularly scheduled time, and whether an absence is deemed to be excusable is at the discretion of the instructor.

Academic Honesty

Academic honesty is governed by Article II of the University of Idaho's Student Code of Conduct http://www.webs.uidaho.edu/fsh/2300.html. Cheating on classroom or outside assignments, including examinations is a violation of this code. Incidents of academic dishonesty will be kept on file by the instructor and may be reported to the dean of students. Such instances of academic dishonesty may warrant expulsion from the course and a failing grade. All students should be aware that even one incident of academic dishonesty may also merit expulsion from the University.

Policies

- Homework and exam scores become final one week after they are returned to the class.
- Late submissions of assignments and project reports are not encouraged; however, if you cannot finish in time and submit late before the solutions are available, a 25% per day compounding deduction will be applied on the final grade. (Ex.:100 points assignment submitted 3 days late will be graded on 42 points, 1 day on 75, 2 days 56, 4 days 32, etc.).
- Submission will not be accepted if the solutions are distributed by any means.
- Assignments have to be turned in during class session. I will not accept any assignment dropped in my office mailbox without getting my permission earlier. You may consult with others on assignments, provided you only submit your attempt at the work. Identical assignments will receive a grade of zero and be considered as academic dishonesty case. Assignment is considered one day late if it is not turned in before 12:30 PM on the day it is due.
- Neither the final exam nor final project will be returned at the end of the semester.