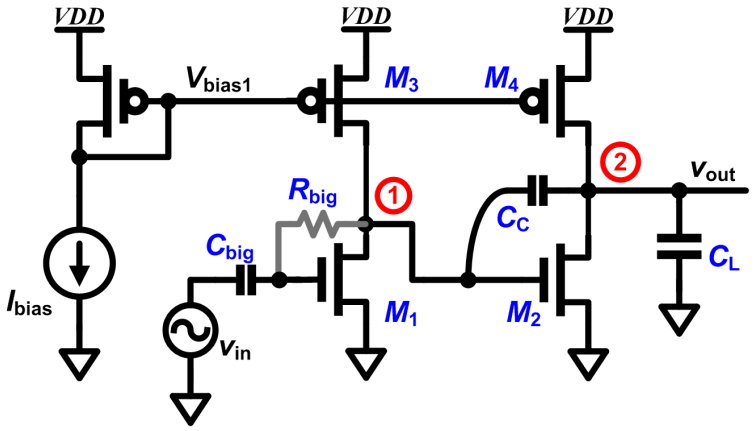
ECE 5415 Analog Integrated Circuit Design
Sample Midterm 2
Nov 16, 2017 **Name:** _____

Closed Book, Closed Notes, Closed Computer.
Show your steps clearly to get credit.
State clearly any assumptions made.
This exam has 5 questions, for a total of 100 points.

1. Consider the Miller-compensated two-stage amplifier shown below,



The pole and zero expressions for the amplifier are given by

$\omega_z = +\frac{g_{m1}}{C_c}$

$\omega_{p_1} \approx \frac{1}{g_{m2}R_2R_1C_c}$

$\omega_{p_2} \approx \frac{g_{m2}C_c}{C_2(C_1+C_C)+C_CC_1} \approx \frac{g_{m2}}{C_2}$

(a) (5 points) Explain pole-splitting in this circuit, showing relevant pole-zero plot.

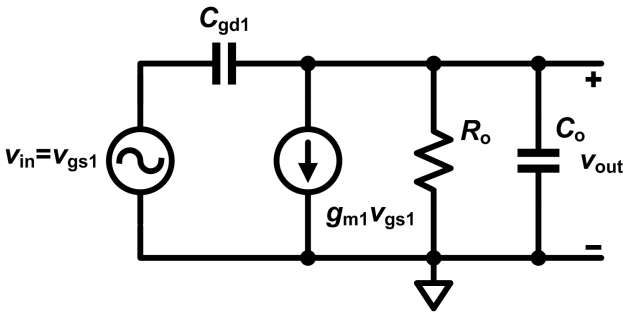
(b) (5 points) Looking at the circuit, qualitatively explain why does a feed-forward (Miller) capacitance lead to an RHP zero in a common-source stage?

(c) (5 points) Qualitatively, why does the second pole (ω_{p_2}) gets pushed to a frequency location roughly given by $\frac{g_{m2}}{C_2}$?

(d) (5 points) Assuming that the amplifier is dominant pole compensated, derive the expression for unity gain frequency (f_{un}).

(e) (0 points) Comment on any slew-rate limitation in this amplifier.

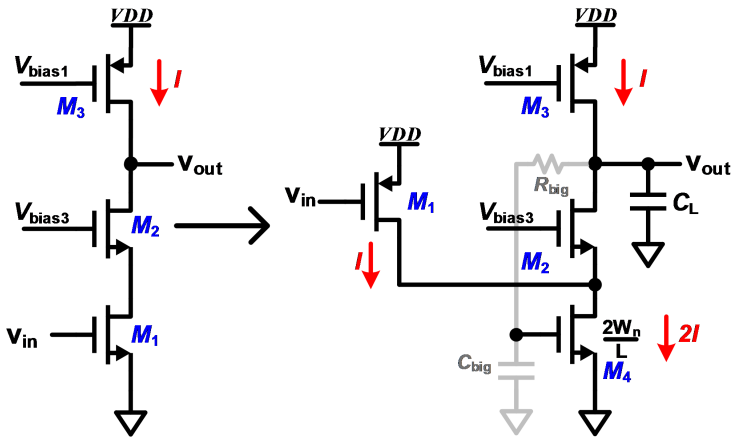
2. (20 points) Solve for $\frac{v_{out}}{v_{in}}(s)$ in the following circuit. Find the locations of the pole (ω_p) and zero (ω_z). Assuming that $C_o \gg C_{gs1}$, sketch rough Bode magnitude and phase plots.



3. (a) (10 points) Derive and explain Miller (capacitance multiplication) Effect in amplifiers with negative gain.

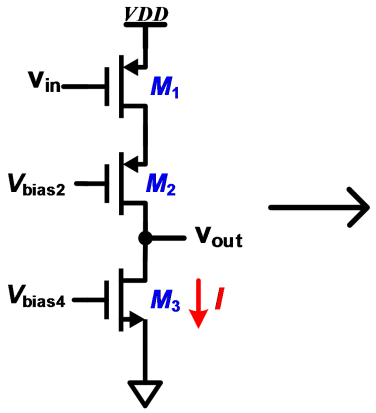
(b) (5 points) Why does a source follower (common-drain) amplifier have a low input capacitance? Use a circuit sketch to illustrate your answer.

4. A cascode amplifier can be converted to its equivalent 'folded-cascode' topology for alleviating voltage swing limitations in the former. The figure below illustrates the translation of a single-ended NMOS *cascode amplifier* to its *folded-cascode* counterpart, where the input device is replaced by its PMOS equivalent.



(a) (10 points) Find the small-signal gain of the folded-cascode amplifier (b) shown above, and compare it with the gain of the cascode amplifier (a).

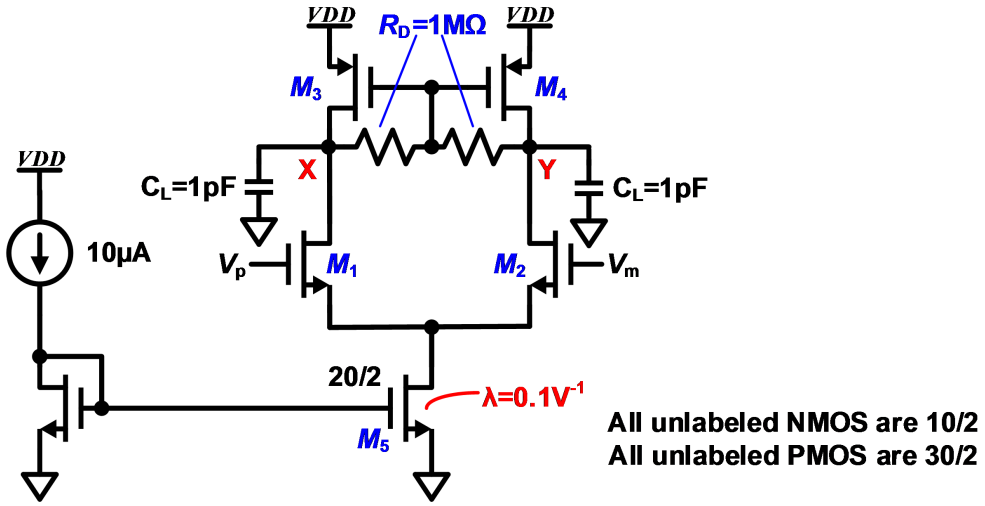
(b) (10 points) Draw the equivalent *folded cascode* amplifier for the PMOS cascode amplifier shown below.



5. Use the MOSFET parameters shown in Table below. Assume $\lambda = 0$ unless specified for a device.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$1\,\mu m$	
V_{DD}	5 V	
V_{THN} and $\lvert V_{THP}\rvert$	0.8	0.9
KP_n and KP_p	120 $\frac{\mu A}{V^2}$	40 $\frac{\mu A}{V^2}$
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	1.75 $\frac{fF}{\mu m^2}$	
C_{oxn} and C_{oxp}	35 fF	105 fF
C_{gsn} and C_{sgp}	23.3 fF	70 fF
C_{gdn} and C_{dgp}	2 fF	6 fF

For the amplifier shown in the figure below:



(a) (5 points) Determine the DC operating point at nodes X and Y.

(b) (5 points) If $v_{in} = v_p - v_m$ and $v_{out} = v_Y - v_X$, determine small-signal differential gain $A_{v,DM}$.

(c) (5 points) Determine small-signal common-mode mode gain $A_{v,CM}$.

(d) (5 points) Find CMRR and input common-mode range (ICMR).

(e) (5 points) Find the locations of pole(s) and zero(s), and small-signal transfer function, $\frac{v_{out}(s)}{v_{in}(s)}$.