ECE 415/515 –ANALOG INTEGRATED CIRCUIT DESIGN

CMOS PROCESS CHARACTERIZATION

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DESIGN PARAMETERS

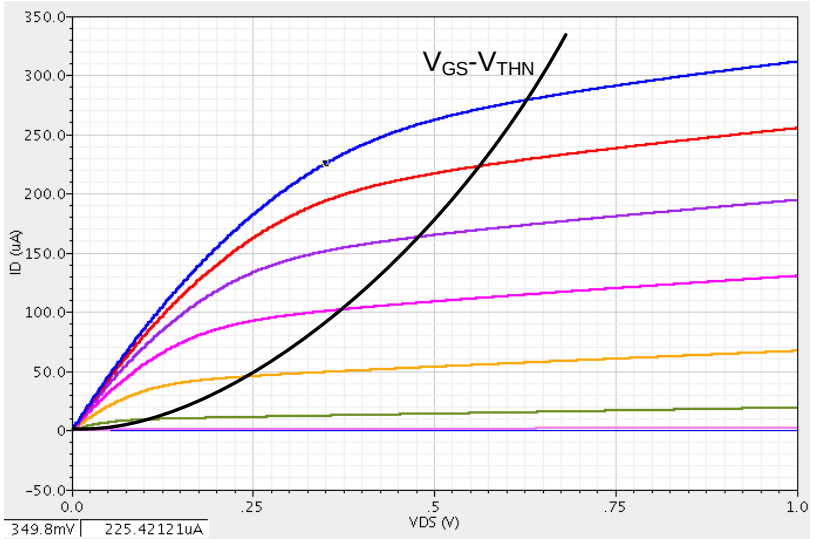
- Analog circuit designers care about:
  - Open-loop Gain: $g_m r_o$
  - Bandwidth (speed): C_{gs}, C_{gd}, f_T, f_{max}, etc.
  - Power: $V_{DD}*I_{DD}$
  - Voltage swing: $V_{DS,sat}$
  - Noise
  - Linearity
  - Mismatch (systematic and random)
- Layout Engineers care about:
  - W/L sizing, layout matching, circuit isolation,….

SHORT CHANNEL CHARACTERISTICS

- Square law equations are no longer valid
  - Intuition derived from classical analysis is still helpful
  - $i_D = v_{sat} W C_{ox} (V_{GS} - V_{THN} - V_{DS,sat})$
    - v_{sat}=saturation velocity
    - C_{ox}=oxide capacitance per unit area
  - Velocity saturation and overshoot effects
- Current analog technology is 14nm, typical designs in 65nm
  - Requires NDA agreements
- CMOS Book uses 50nm process parameters
  - V_{DD}=1V, L_{min}=50nm
  - V_{THN}=V_{THP}=280mV

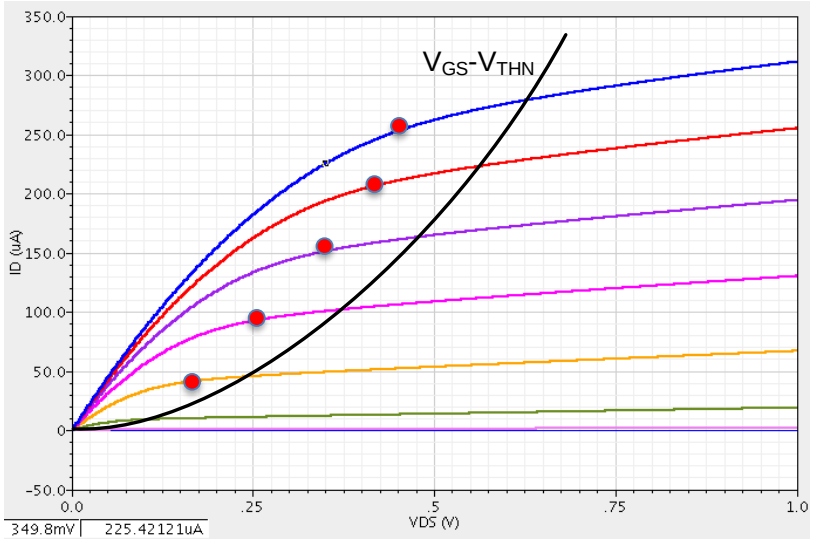
SHORT CHANNEL CHARACTERISTICS (2)

- Short-channel devices appear to enter saturation as a lower voltage than predicted by the equation $V_{DS,sat}=V_{GS}-V_{THN}$
  - $V_{DS,sat} \neq V_{ov}=V_{GS}-V_{THN}$
  - The actual inversion layer charge distribution, $Q'_I(y)$, is a function of V_{DS}, in addition to V_{GS}
  - $Q'_I(y)$ becomes zero at a lower $V_{DS,sat}$



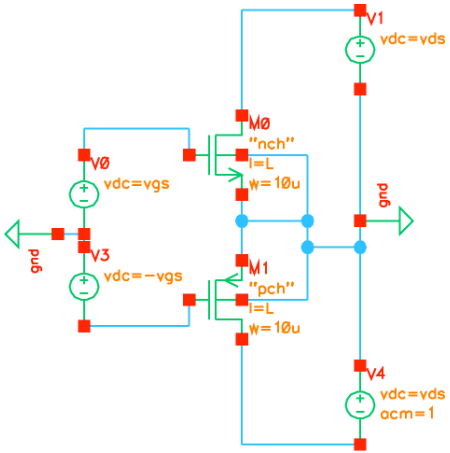
SHORT CHANNEL CHARACTERISTICS (3)

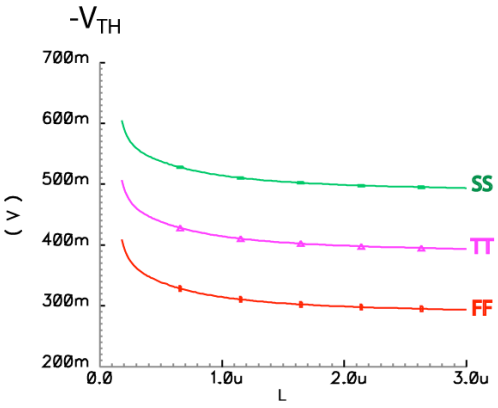
- Is a large range for the saturation region beneficial?
  - We could really use the larger swing!
- Not really, need to look at the region where r_o is large and that occurs when the device is deep into saturation :(

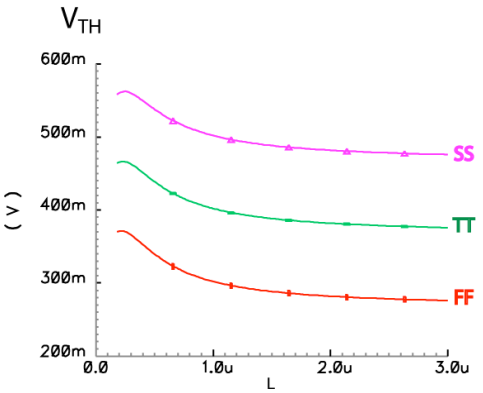


THRESHOLD VOLTAGE

- Strong function of L
  - Use long channel for V_{TH} matching
- Process variations
  - Run-to-run ~100mV
  - Slow/nominal/fast
- Good design should be insensitive to the absolute value of V_{TH}
  - Should only depend upon the mismatch in V_{TH} (~1mV) for good layout and large devices



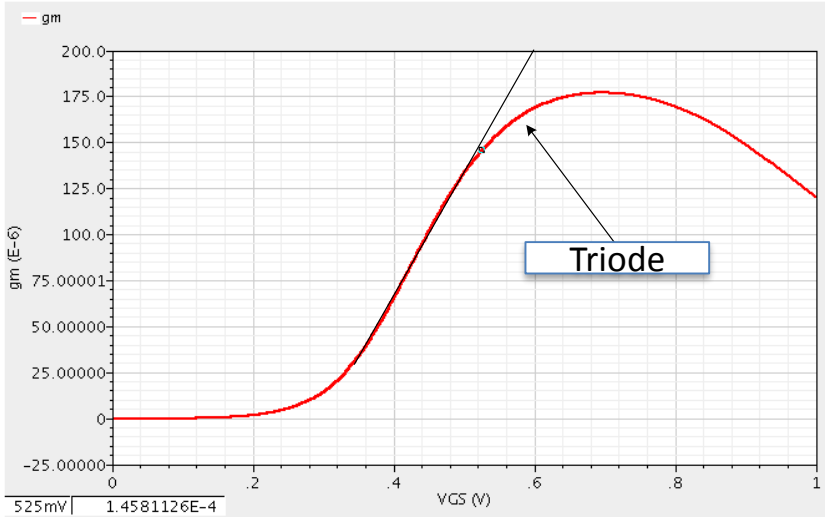




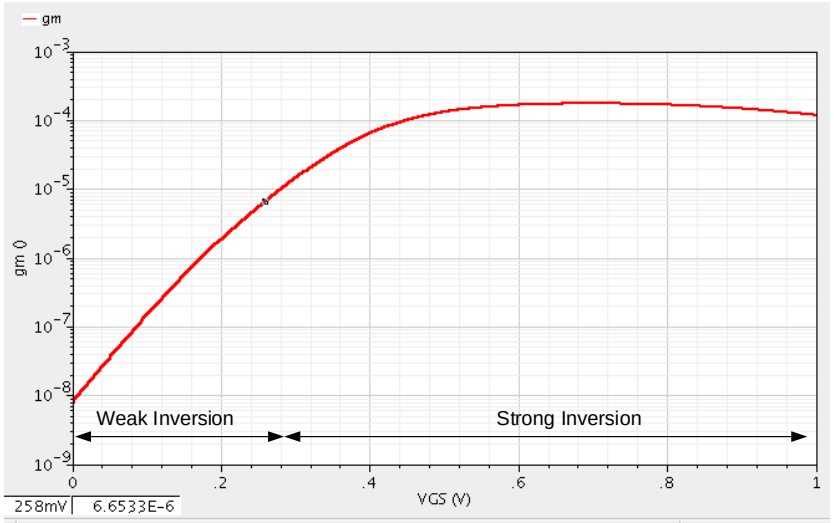
SHORT CHANNEL CHARACTERISTICS

- For short-channel design, the equation $V_{DS,sat}=V_{GS}-V_{THN}$ is meaningless
- From now onwards, we'll talk in terms of the gate overdrive voltage
  - $V_{ov}=V_{GS}-V_{THN} > V_{DS,sat}$
- We can use V_{ov} = 5% of V_{DD} as a starting point for high-speed design (build your intuition)
- Vov = 70mV!
  - VGS = 350mV
- A more robust method is to use constant g_m/I_D and current density (I_D/W) across the design, instead of a constant V_{ov}
  - Refer to the slides “Analog Design Using g_m/I_d and f_t Metrics” by Prof. Boser of UC Berkeley

TRANSCONDUCTANCE



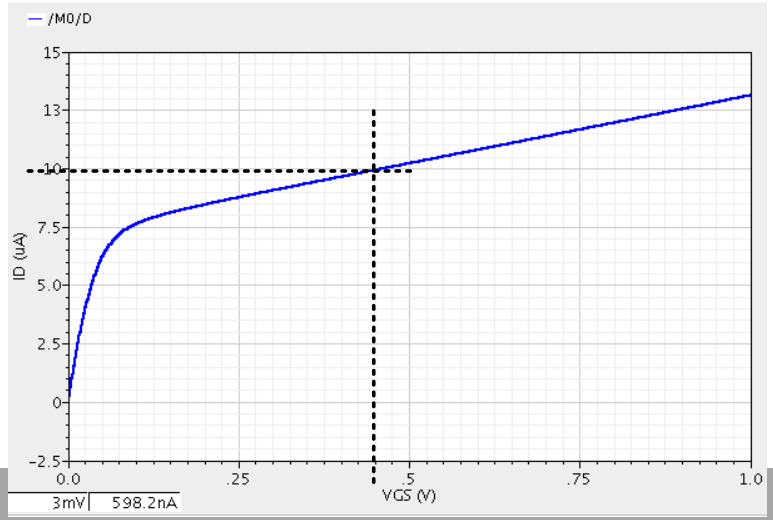
$g_m = (V_{GS} - V_{THN})$

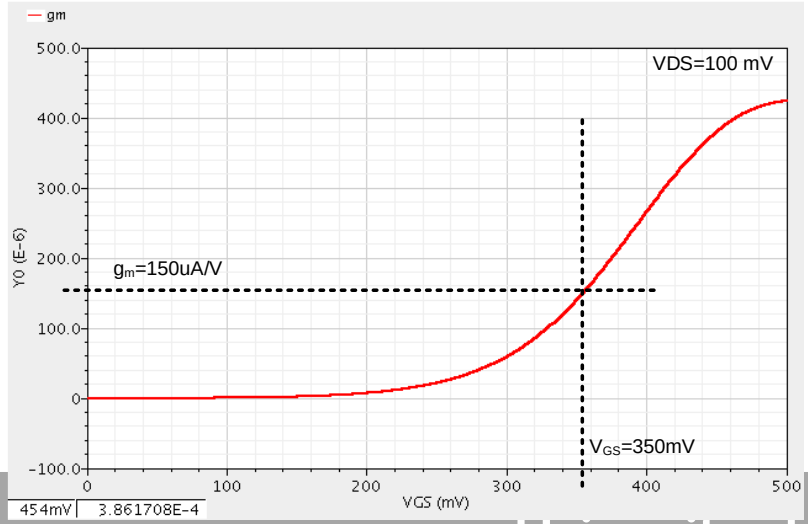


$g_{msub-VT} = I_D/nV_T$

TRANSCONDUCTANCE

- Given $V_{ov}=2I_D/g_m$, and a specified value of g_m
- Pick I_D and W based on
- Here, for a g_m=150uA/V, we pick 10uA for sufficient current drive
- This leads to W=50 for NMOS and W=100 for PMOS

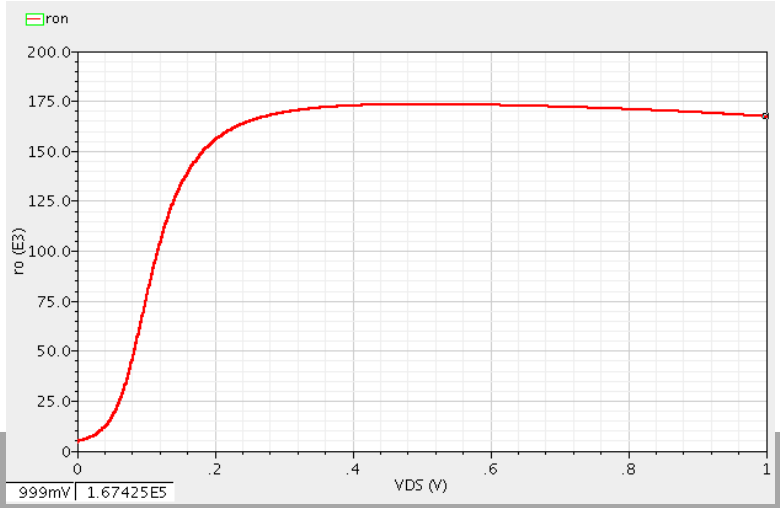


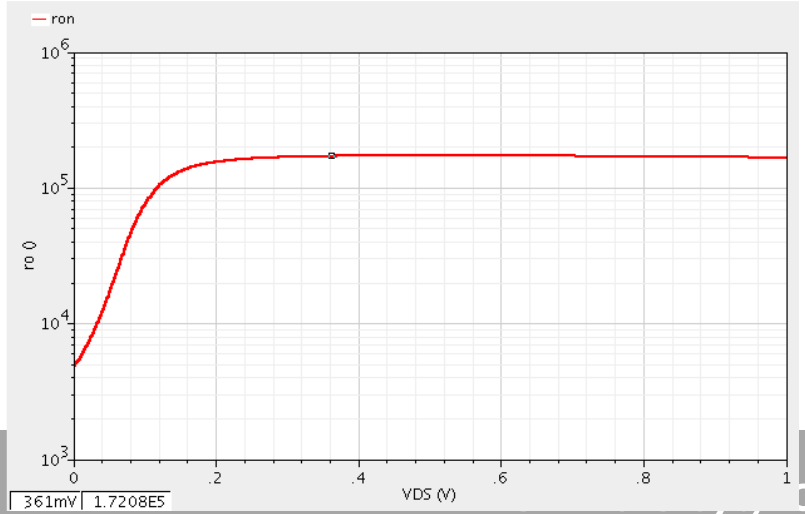


OUTPUT RESISTANCE

- To determine $V_{DS,sat}$, look at the point where the output resistance starts to increase (Here, $V_{DS,sat}$ = 50mV)
- We get considerably higher output resistances at a larger VDS(important!)

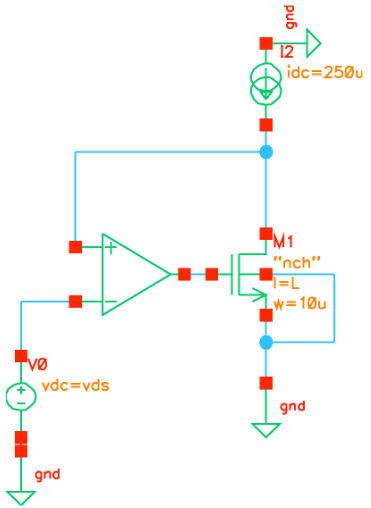
Can't just model by a simple equation, $r_o = 1/I_{D,sat}$

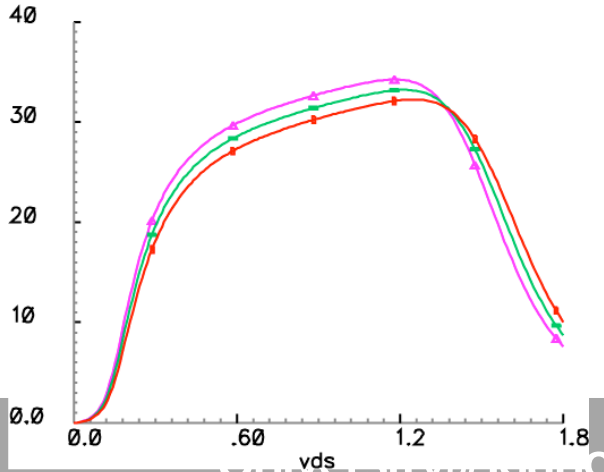




OPEN-LOOP GAIN ($g_m r_o$)

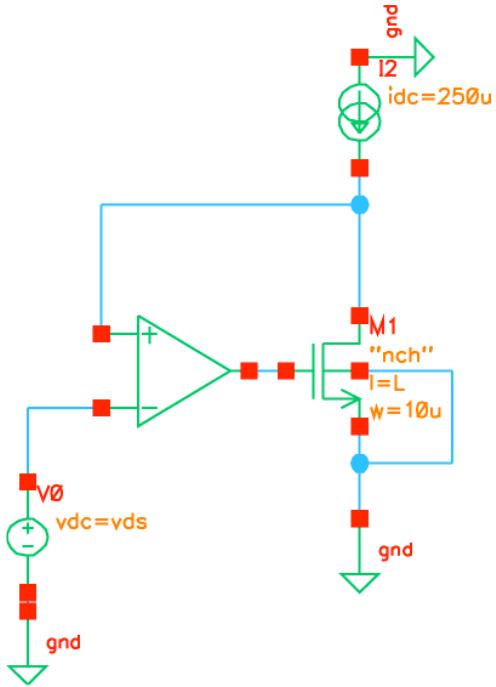
- $g_m r_o$ is more useful than just r_o
  - Represents maximum attainable gain from a transistor
- Simulation Notes:
  - Bias current *idc* sets V_{ov}
  - Use feedback to find the correct V_{GS} while sweeping V_{DS}
  - Use relatively small error-amplifier gain (A=100) for fast DC convergence





OPEN-LOOP GAIN ($g_m r_o$)

- The open loop gain is roughly $g_m r_o = 150\mu AV \cdot 170k$ ~25
- Considerably lower than the open-loop gain in a long-channel process.



LONG-CHANNEL CMOS, L_{MIN}=1UM

Table 9.1 Typical parameters for analog design using the *long-channel* CMOS process discussed in this book. Note that the parameters may change with temperature or drain-to-source voltage (e.g., Fig. 9.24).

Long-channel MOSFET parameters for general analog design *VDD* = 5 V and a scale factor of **1 μm** (*scale* = 1e–6)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	20 μA	20 μA	Approximate
W/L	10/2	30/2	Selected based on I_D and $V_{DS,sat}$
$V_{DS,sat}$ and $V_{SD,sat}$	250 mV	250 mV	For sizes listed
V_{GS} and V_{SG}	1.05 V	1.15 V	No body effect
V_{THN} and V_{THP}	800 mV	900 mV	Typical
$\partial V_{THN,P}/\partial T$	−1 mV/C°	−1.4 mV/C°	Change with temperature
KP_n and KP_p	120 μA/V^2	40 μA/V^2	t_{ox} = 200 Å
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	1.75 fF/μm^2	1.75 fF/μm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	35 fF	105 fF	PMOS is three times wider
C_{gsn} and C_{sgp}	23.3 fF	70 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	2 fF	6 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 μA/V	150 μA/V	At I_D = 20 μA
r_{on} and r_{op}	5 MΩ	4 MΩ	Approximate at I_D = 20 μA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	750 V/V	600 V/V	Open circuit gain
λ_n and λ_p	0.01 V^{-1}	0.0125 V^{-1}	At L = 2
f_{Tn} and f_{Tp}	900 MHz	300 MHz	For L =2, f_T goes up if L = 1

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SHORT-CHANNEL CMOS, L_{MIN}=50NM

Table 9.2 Typical parameters for analog design using the *short-channel* CMOS process discussed in this book. These parameters are valid only for the device sizes and currents listed.

Short-channel MOSFET parameters for general analog design *VDD* = 1 V and a scale factor of **50 nm** (*scale* = 50e–9)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	10 μA	10 μA	Approximate, see Fig. 9.31
W/L	50/2	100/2	Selected based on I_D and V_{ov}
Actual W/L	2.5μm/100nm	5μm/100nm	L_{min} is 50 nm
$V_{DS,sat}$ and $V_{SD,sat}$ V_{ovn} and V_{ovp}	50 mV 70 mV	50 mV 70 mV	However, see Fig. 9.32 and the associated discussion
V_{GS} and V_{SG}	350 mV	350 mV	No body effect
V_{THN} and V_{THP}	280 mV	280 mV	Typical
$\partial V_{THN,P}/\partial T$	– 0.6 mV/C°	– 0.6 mV/C°	Change with temperature
v_{satn} and v_{satp}	110 x 10^3 m/s	90 x 10^3 m/s	From the BSIM4 model
t_{ox}	14 Å	14 Å	Tunnel gate current, 5 A/cm^2
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	25 fF/μm^2	25 fF/μm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	6.25 fF	12.5 fF	PMOS is two times wider
C_{gsn} and C_{sgp}	4.17 fF	8.34 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	1.56 fF	3.7 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 μA/V	150 μA/V	At I_D = 10 μA
r_{on} and r_{op}	167 kΩ	333 kΩ	Approximate at I_D = 10 μA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	25 V/V	50 V/V	!!Open circuit gain!!
λ_n and λ_p	0.6 V^{-1}	0.3 V^{-1}	L = 2
f_{Tn} and f_{Tp}	6000 MHz	3000 MHz	Approximate at L = 2

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BMR CIRCUIT IN 1UM CMOS

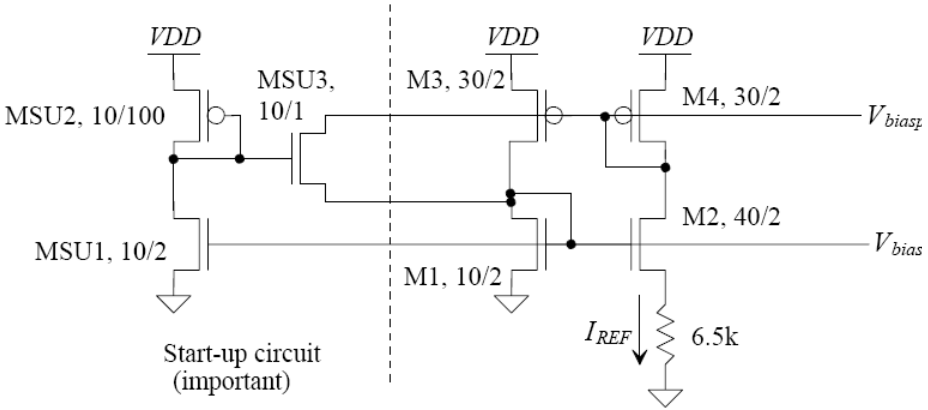

Figure 20.15 Beta-multiplier reference for biasing in the long-channel process described in Table 9.1.

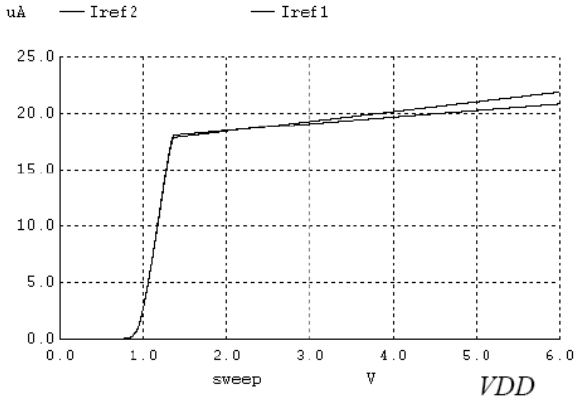

Figure 20.16 The reference currents through M1 and M2 in the Beta-multiplier.

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