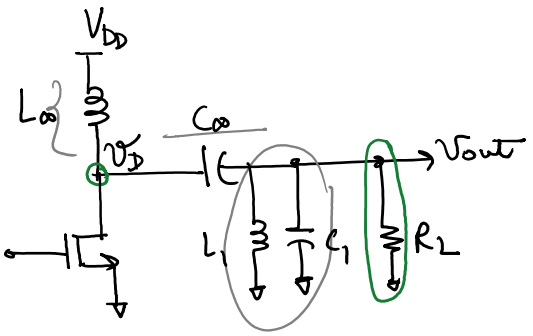
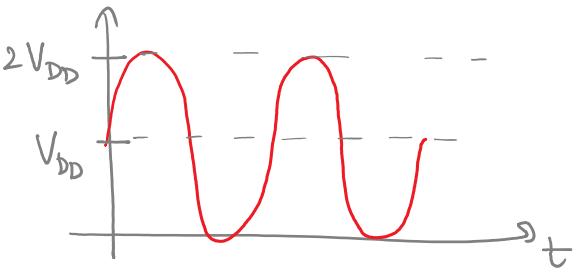
ECE 513- lecture 28

Tuesday, December 4, 2018 9:30 AM



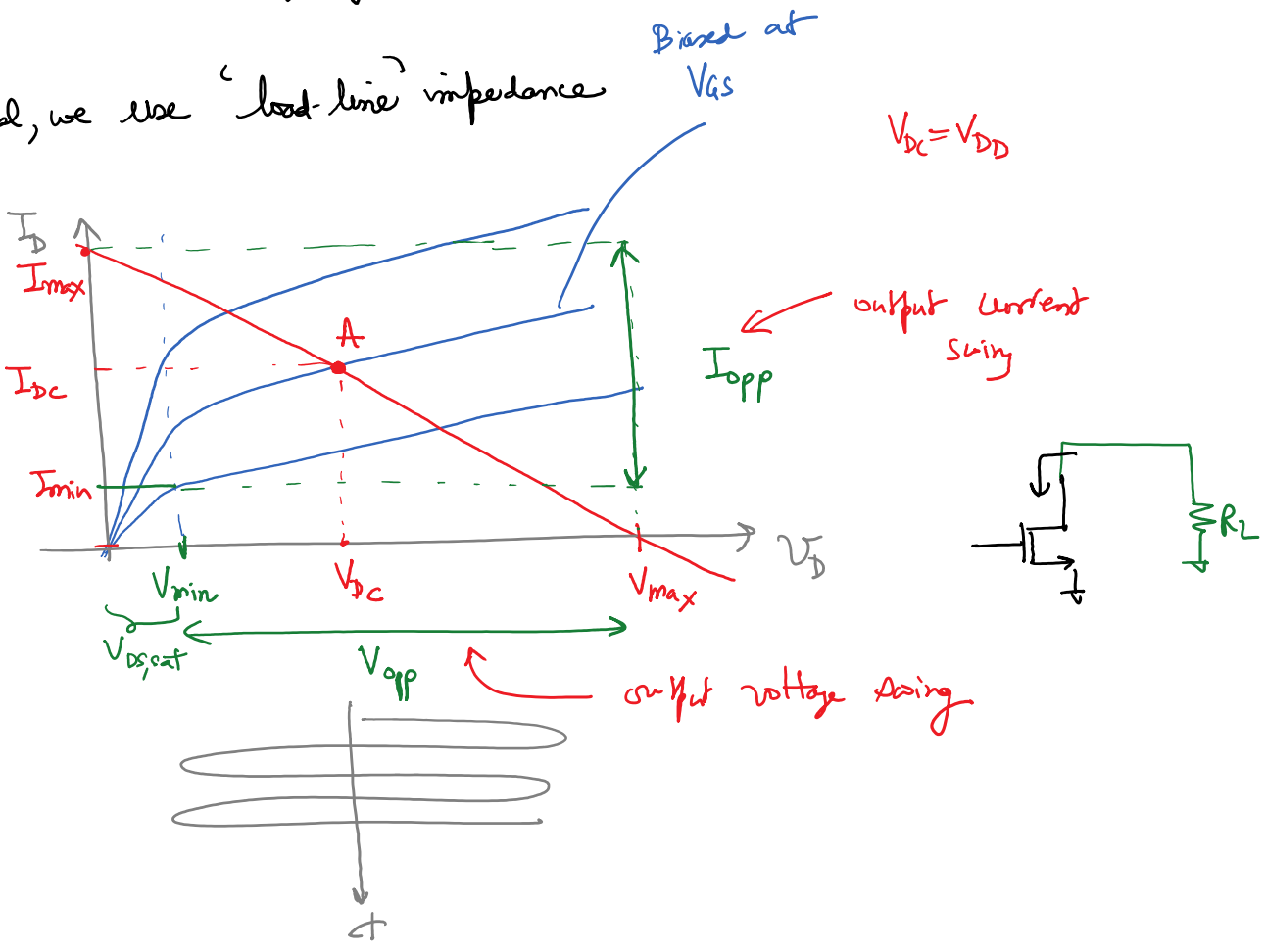


$R_{L_{OPT}}$:

↳ The PAs operate with the largest voltage & current swing
↳ large signal behavior

↳ small-signal parameters obtained from measurements are not useful in the design of output matching network

* Instead, we use 'load-line' impedance



$$R_{Lopt} = \frac{V_{opp}}{I_{opp}} \approx \frac{V_{MAX}}{I_{max}} = \frac{V_{MAX}}{2 \cdot I_{DC}}$$

↳ This optimal load impedance maximizes the output power delivered to the load when the amplifier is operated at P_{1dB} and beyond.

↳ called power matching as opposed to small-signal impedance matching.

* Simulation Techniques have been developed to allow for the prediction of R_{LOPT}, return loss, etc as a function of load impedance

* The output matching network must be designed to transform $Z_0 = 50\Omega$ load impedance to R_{LOPT} of the transistor output.

↳ for input side → for small voltage swings, we can use small-signal impedance matching.

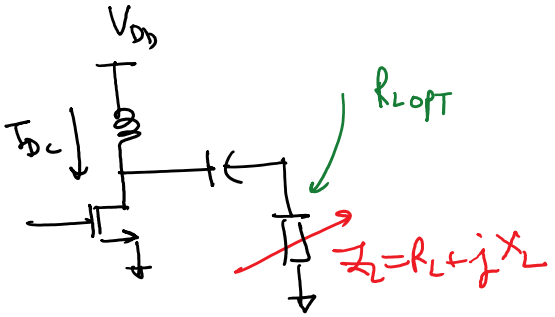
Load-pull Contours:

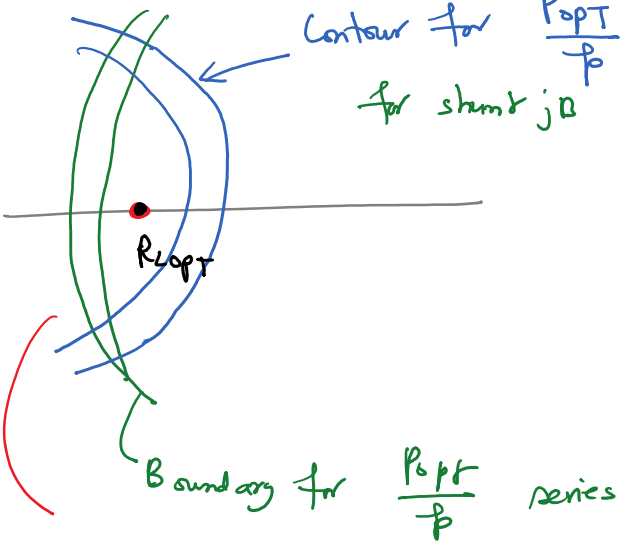
If $V_{min}=0$, the maximum output power

$$P_{LOPT} = \frac{V_{opp} \cdot I_{opp}}{8} \simeq \frac{V_{max} I_{max}}{8} \simeq \frac{V_{DC} \cdot I_{DC}}{2}$$

is obtained when $R_L = R_{LOPT}$

* The exact value of R_{LOPT} is obtained by measuring or simulating the output power for different load impedance values. and selecting the load impedance corresponding to the highest output power.



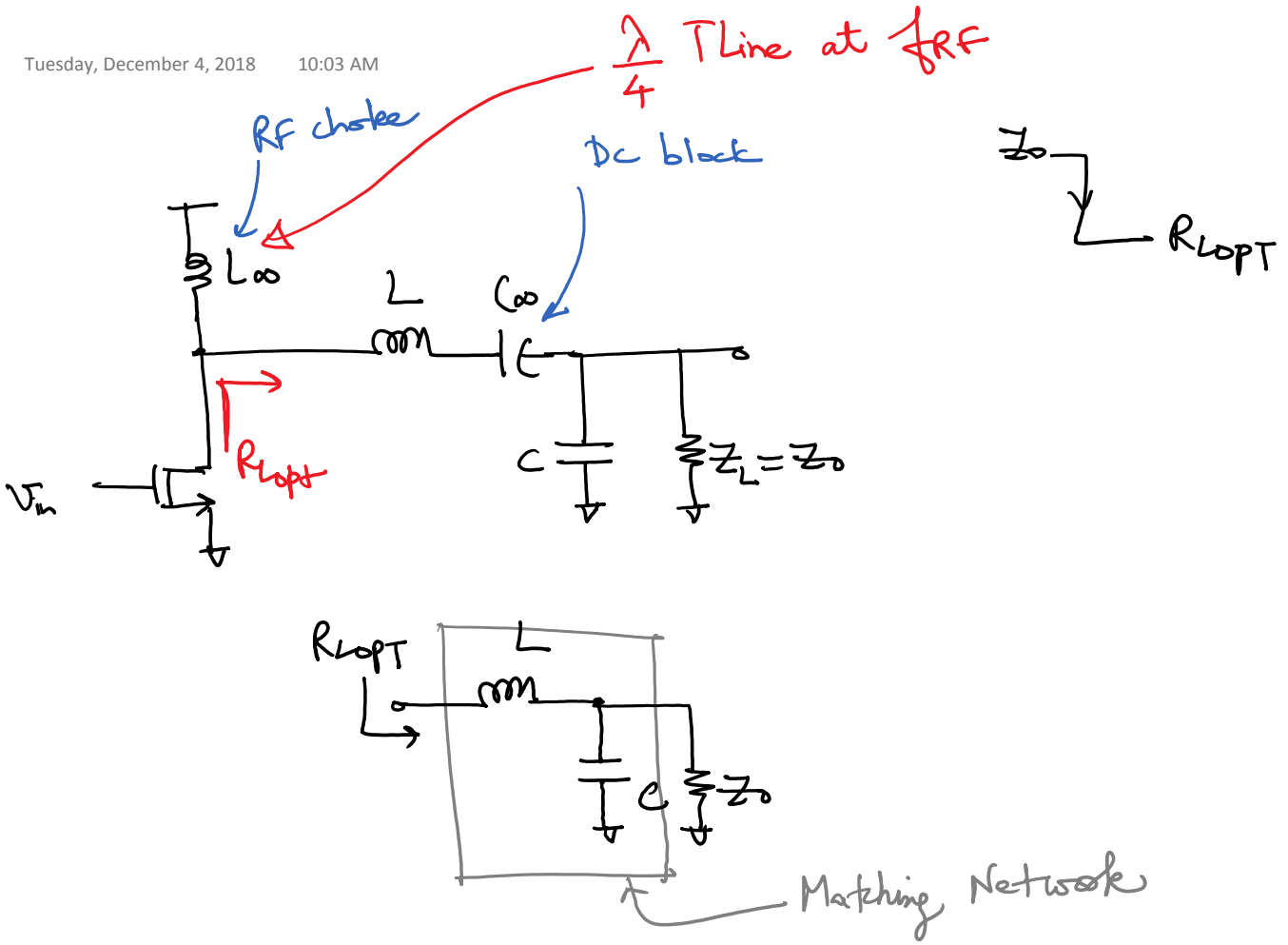


Constant output power contours on the Smith chart.

* Constant resistance $\left(R_L = \frac{R_{LOPT}}{p}\right)$ and constant conductance circles $\left(G_L = \frac{1}{pR_{LOPT}}\right)$ along which the power is $10\log_{10}(p)$ dB

P_{LOPT}

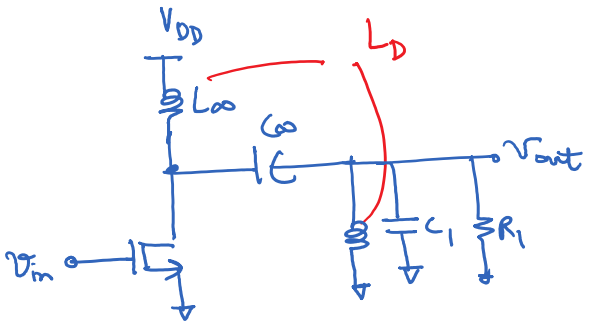
Smaller than P_{LOPT}.



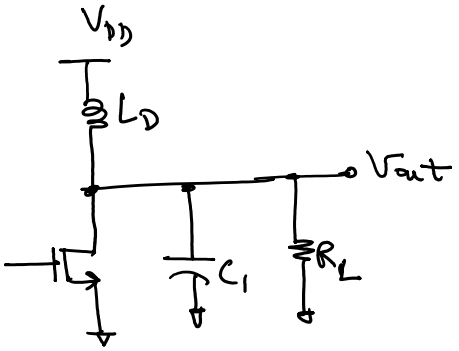
In general $\frac{Z_o}{Z_{OPT}}$ leads to high-Q matching network
↳ narrowband
↳ use two-step match for higher BW.

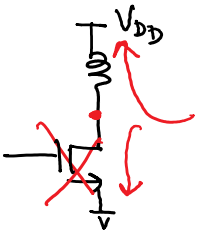
Class-A:

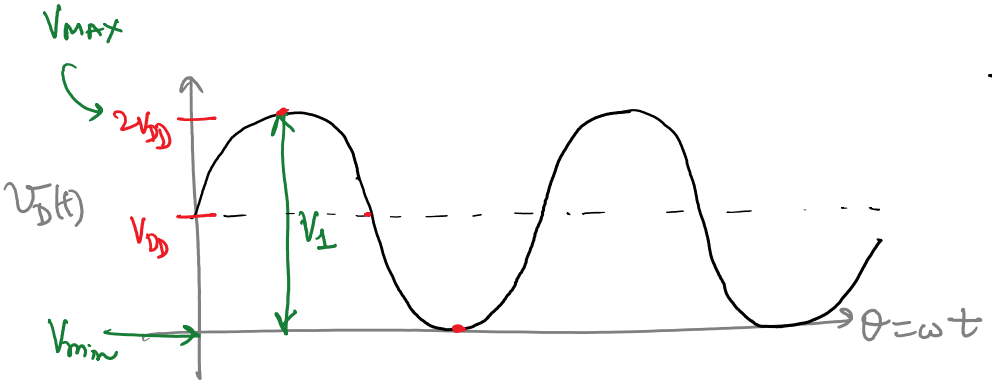
* The class A, B, (AB), C similar looking waveforms but different conduction angles.



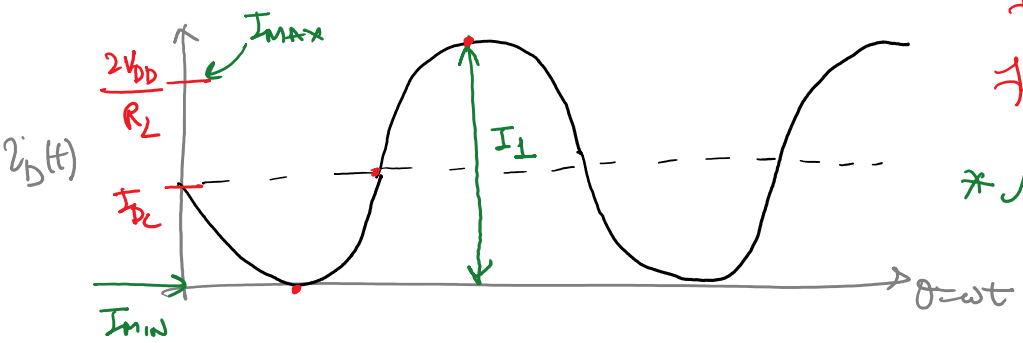
Simplified ⇒







$\omega \Rightarrow Rf$ frequency



transistor conducts for full $0 < \theta < 2\pi$

* Conduction angle is 2π

* The transistor is biased at the peak f_T current density J_{pf_T}

* The output matching network is designed so that the transistor is terminated (or matched) to R_L at the fundamental frequency f_0

↳ and short circuit for all of its harmonics.

$Z_L(f_0) = R_L$ & $Z_L(nf_0) = \infty$ for $n > 1$

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

Class-A Efficiency :

$$\eta = \frac{P_L}{P_{DC}} = \frac{(V_1 \cdot I_1)/2}{V_{DD} \cdot I_{DC}} = \frac{V_1 I_1}{2 V_{DD} \cdot I_{DC}} = \frac{(V_{DD} - V_{MIN})(I_{DC} - I_{min})}{2 V_{DD} \cdot I_{DC}} \quad (1)$$

$I_{min} \Rightarrow$ min value of current

$I_1 = I_{DC} - I_{min} \Rightarrow$ amplitude of the fundamental voltage in the load

$V_{DC} = V_{DD}$

$I_{DC} = \frac{V_{DD}}{R_L}$

from (1), maximum drain efficiency for $V_{min}=0$ & $I_{min}=0$

$\eta \leq 50\%$

$PAE \propto \left(1 - \frac{V_{MIN}}{V_{MAX}}\right)$ ← really depends upon the value of V_{max}

Ex. 65nm CMOS : $V_{max} = 1.5V$ $V_{min} = 0.1V$

$V_1 = \frac{(V_{max} - V_{min})}{2} = 0.7V$

$\eta = \frac{V_1}{V_{1\,ideal}} \times 50\% = \frac{0.7}{0.75} \times 50\% = 46.6\%$

* for GaN PA: $V_{max} = 80V$, $V_{min} = 0.5V$

$\Rightarrow \eta_{max} = 49.7\%$

for CMOS FoM improves as f^2

with scaling we can leverage a higher f_{max}

* It usually helps to use scaled CMOS to get more power out of the transistors esp. at mmWave frequencies.

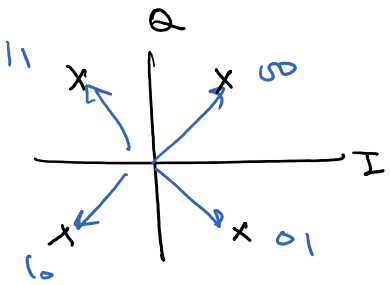
Issues with Class-A PA:

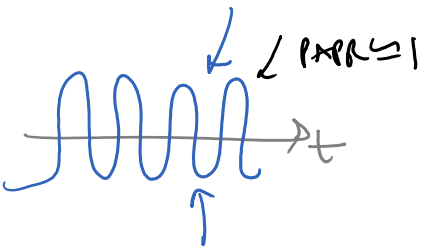
* Current is conducted for the full $\theta = 2\pi$ period

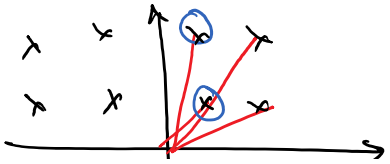
$\Rightarrow$ keeps the $\eta < 50\%$

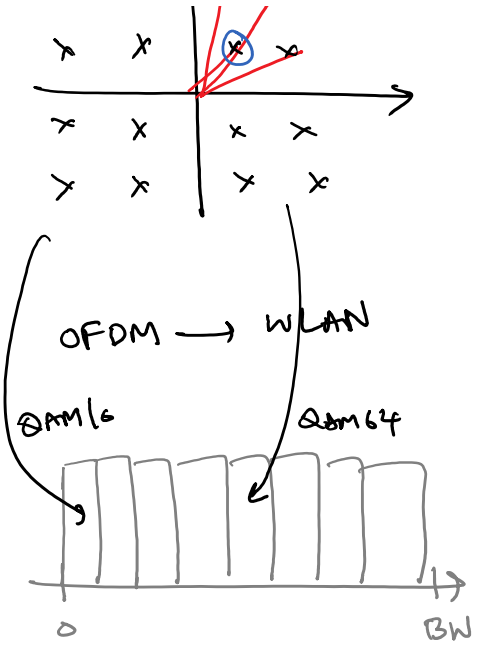
└ backoff efficiency is lower as the transistor conducts the same I_{DC} from V_{DD}.

PAPR $\Rightarrow$ Peak to average power ratio









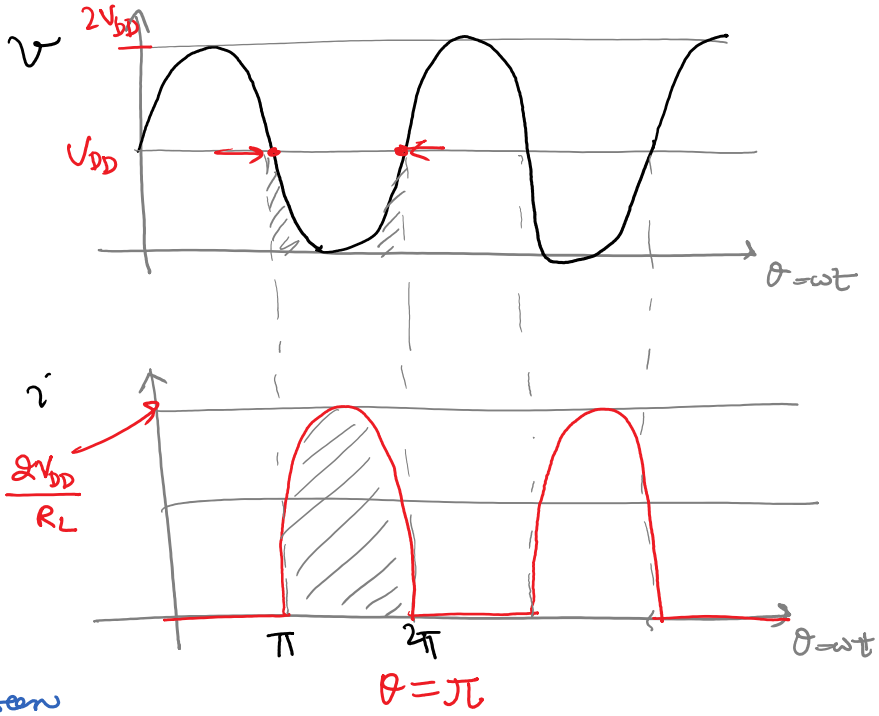
PAPR is very high

Class-B :

⇒ The transistor enters cutoff for half of the signal period

⇒ Bias the transistor at the edge of cutoff such that the conduction angle $\theta = \pi$.

↳ reduces the overlap between the voltage and current waveforms.



Average (or DC current)

$$I_{DC} = \frac{I_{max}}{2\pi}\int_{\pi}^{2\pi} \sin\theta \, d\theta = \frac{I_{MAX}}{\pi} = \frac{2V_{DD}}{\pi \cdot R_L}$$

$$\eta = \frac{P_L}{P_{DC}} = \frac{V_1 \cdot I_1}{2I_{DC} \cdot V_{DD}} = \frac{V_{DD} \cdot \frac{I_{max}}{2}}{\frac{2V_{DD}}{\pi} \cdot I_{max}} = \frac{\pi}{4} \Rightarrow 78.5\%$$

maximum drain effeciency.