ECE 513- Lecture 21

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* 6 GHz LNA Design Example:

Data from Table 7.1 in Textbook

Also, $k_1 = 0.5$

$$X_{sopT} = 1.15 \frac{\omega_T}{\omega g_{meff}}$$

* 180nm CMOS

* load inductor has a fixed $Q = 10$

* output of the LNA is terminated on a matched load

* Determine transistor sizes, bias current, L_s & L_G and estimate the power gain for the CMOS Cascode LNA

* Assume that the best finger width for minimum noise is $W_f = 2\,\mu m$.

6 GHz LNA Design:

$W_f = 2\,\mu m$, $J_{opT} = 0.15 \frac{mA}{\mu m}$ ← from process characterization

from Table

* $$g'_{meff} = \frac{g'_m}{1 + g'_m R'_s} \Rightarrow g'_m = \frac{g'_{meff}}{1 - R'_s g'_{meff}} = \frac{0.4 \frac{mS}{\mu m}}{1 - 200\,\Omega\,\mu m \times 0.4 \frac{mS}{\mu m}}$$

$$g'_m = 0.434 \frac{mS}{\mu m}$$

$\frac{mA}{V \cdot \mu m}$

① Size the transistors in the cascode st. $R_{sopT} = Z_0 = 50\,\Omega$

$$\Rightarrow N_f = \frac{f_{Teff}}{f Z_0 W_f g'_{meff}} \cdot \sqrt{\frac{g'_m R'_s + W_f g'_m R'_g(W_f)}{k_1}}$$

$R'_g = f(W_f)$

$$= \frac{35\,GHz}{6\,GHz \cdot 50.2\,\mu m \times \frac{0.4\,mS}{\mu m}} \cdot \sqrt{\frac{0.43 \times 0.2 + 2 \times 0.43 \times 10^{-3} \times 75}{0.5}}$$

$$\simeq 71$$

$\Rightarrow W = N_f W_f = \underline{142\,\mu m}$, $\quad L = 180\,nm$

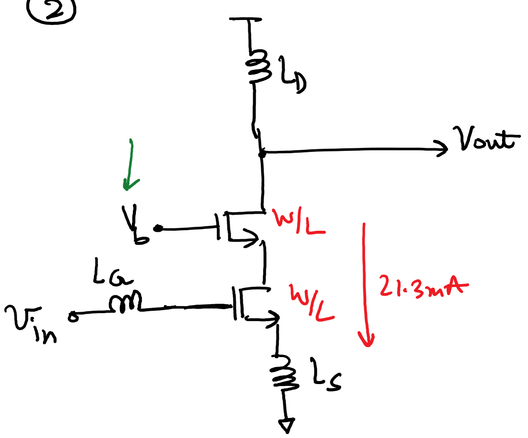
* If we biasing at $J_{OPT} \Rightarrow$

drain current, $I_D = J_{OPT} \times W = 0.15 \frac{mA}{\mu m} \times 142\,\mu m$

$= \underline{21.3\,mA}$.

* $g_{meff} = 0.4 \frac{mS}{\mu m} \times 142\,\mu m = \underline{56.8\,mS}$

②



* $L_S = \frac{Z_0 - R_g - R_s}{\omega_T} = \frac{50 - \frac{75\,\Omega}{71} - \frac{100\,\Omega}{71}}{2\pi \times 35 \times 10^9} \simeq 217\,pH$

* $L_G + L_S = \frac{\omega_T}{\omega_0^2\, g_{meff}} = \frac{\omega_T}{(2\pi f_0)^2\, W g'_{meff}}$

$= 2.72\,nH$

$L_G = 2.72\,nH - 217\,pH = \underline{2.5\,nH}$

PVT ⇒ Process, Voltage & Temperature variations

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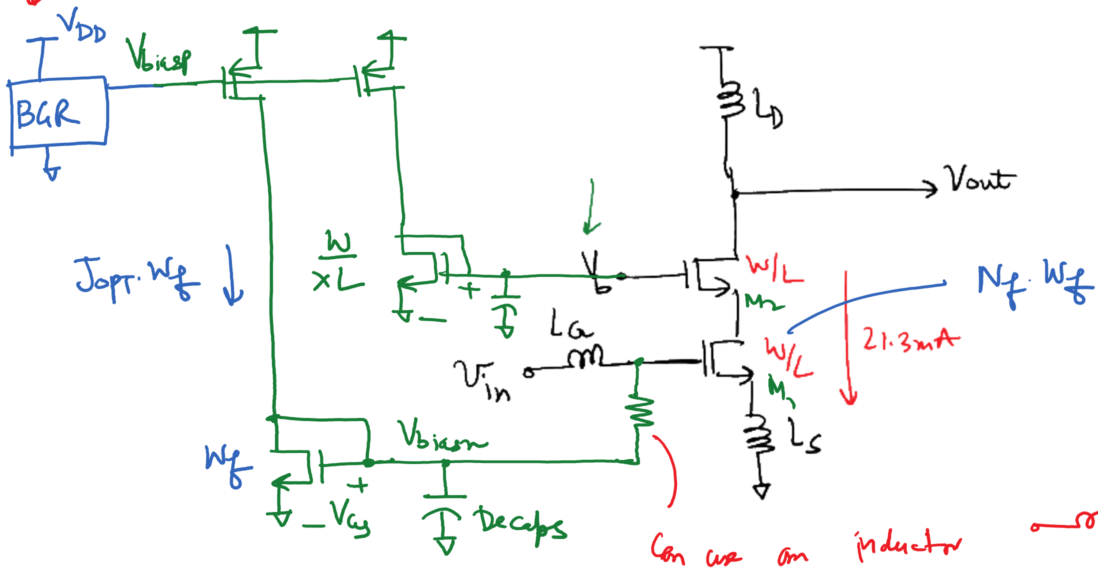
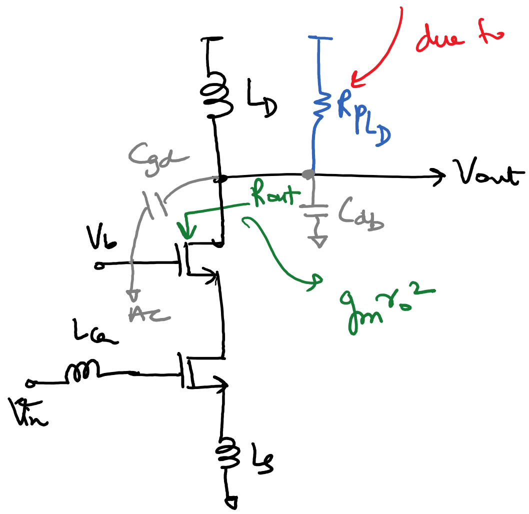


Can use an inductor

↳ becomes part of the matching circuit

$Q = 10$

output is matched



$C_{OUT} = C_{gd} + C_{db}$

$= (C_{db}' + C_{gd}') \cdot W$

$= (1.1 + 0.4) \frac{fF}{\mu m} \times 142\,\mu m = 213\,fF$

$* \quad L_D = \frac{1}{\omega_o^2 C_{OUT}} = \frac{1}{(2\pi\, 6\,GHz)^2\, 213\,fF}$

$= \underline{3.3\,nH}$

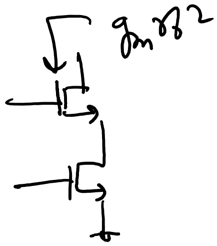
$\omega_o = \frac{1}{\sqrt{LC}}$

$\Rightarrow$ for a parallel RLC

$Q = \frac{R_p}{\omega_o L_p} \Rightarrow R_p = Q \cdot 2\pi f_o \cdot L_D = \underline{1.244\,k\Omega}$

$\Rightarrow$ Resistance looking into the drain of the cascode

$\quad \rightarrow R_{out} = g_m r_o^2 = \frac{g_m}{g_o^2} = \underline{1.76\,k\Omega}$



$\Rightarrow$ Total output resistance

$R_p = R_{pL_D} \| R_{out} = 1.244\,k\Omega \| 1.76\,k\Omega$

$= \underline{728\,\Omega}$

$\because$ the output is matched

$\Rightarrow R_L = R_p$

$\Rightarrow$ Power gain $\Rightarrow G = \frac{f_T^2}{f_o^2} \cdot \frac{R_p}{4Z_o} \longrightarrow$ Eqn 7.25 in the Textbook

$= 126$

$= \underline{\underline{21 \text{ dB}}}$

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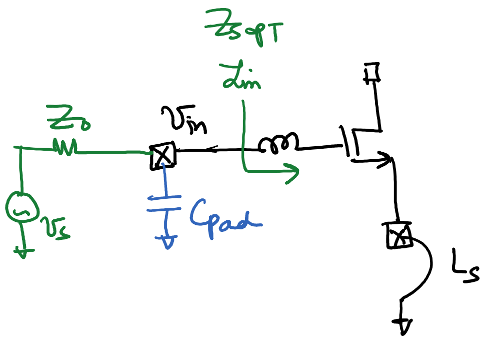
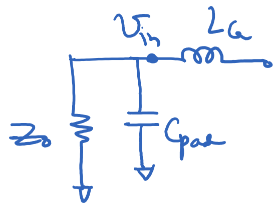
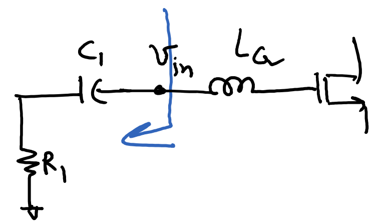
Parasitic Capacitance of the Bond Pad:



$\Rightarrow$



$\Rightarrow$



$\parallel^{l}$ to series transformation

$$R_1 = \frac{Z_0}{1+Q^2} \quad \text{and} \quad C_1 = \left(\frac{Q^2+1}{Q^2}\right) C_{pad}$$

$$Q = \omega_0 R_p C_p = \frac{R_p}{\omega_0 L_p} \rightarrow = \omega_0 Z_0 C_{pad}$$

$$\Rightarrow \quad R_1 = \frac{Z_0}{k}$$

$$C_1 = \frac{k}{k-1} C_{pad}, \quad k = 1+Q^2 = 1+\omega^2 C_{pad}^2 Z_0^2$$

* The new source impedance is complex instead of Z_0

↳ real part (R_1) is frequency dependent

$\Rightarrow$ Adjust our matching.

for noise match, we set $R_{sopT} = \frac{Z_0}{k}$ ← correction factor

$$L_s = \frac{\frac{Z_0}{k} - R_g - R_s}{\omega_T}$$

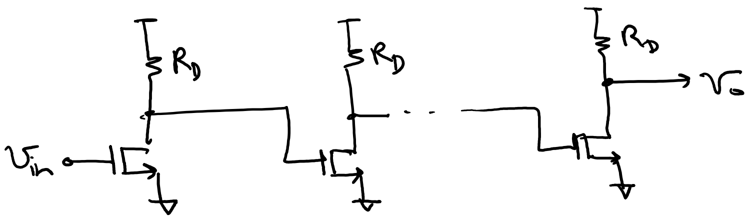
Ex. $f_0 = 65\,GHz$ in 65nm CMOS

$$k = 1.166$$

Techniques to Maximize Bandwidth (BW Extension Techniques):

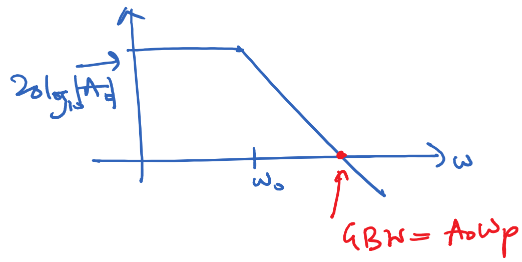
(Chapter 5)

* Bandwidth of an Amplifier Cascade:



* If the voltage gain of each stage is a single pole response

$$A(s) = \frac{A_o}{(1 + s/\omega_p)}$$



* For a cascade of n-identical single-pole stages

$$A_{tot}(s) = A(s)^n = \frac{A_o^n}{(1 + s/\omega_p)^n}$$

⇒ 3dB bandwidth of the chain

$$A_{tot}(s = j\omega_{3dB}) = \frac{|A_o|^n}{\sqrt{2}}$$

$$\Rightarrow \left|1 + \frac{j\omega_{3dB}}{\omega_p}\right| = 2^{1/2n}$$

$$\Rightarrow 1 + \frac{\omega_{3dB}^2}{\omega_p^2} = 2^{1/n}$$

$$\Rightarrow \omega_{3dB} = \omega_p\sqrt{2^{1/n} - 1} \leq \omega_p$$

$$\Rightarrow \quad \omega_{3dB} = \underbrace{\omega_p \sqrt{2^{1/n} - 1}} \;\leq\; \omega_p$$

Overall BW shrinks!

$\Rightarrow$ gain bandwidth

$$GBW_{tot} = A_0^n \, \omega_p \sqrt{2^{1/n} - 1} = A_{tot} \, \omega_p \sqrt{2^{1/n} - 1}$$

* Ratio of GBW of the entire cascade to that of the individual stage

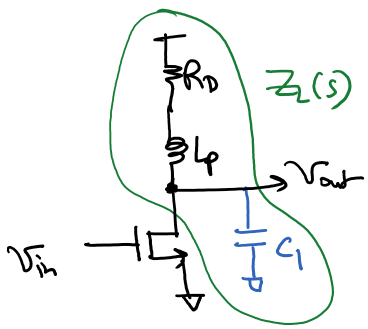
$$\frac{GBW_{tot}}{GBW_s} = A_{tot}^{1 - 1/n} \times \sqrt{2^{1/n} - 1}$$

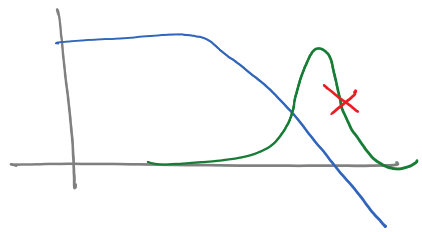
$$\frac{\partial}{\partial n}\left(\frac{GBW_{tot}}{GBW_s}\right) = 0 \quad \Rightarrow \quad n_{opt} \simeq 2 \ln(A_{tot})$$

* See Ex. 5.5 in the Textbook

* How to increase the BW of the individual stages?

Shunt peaking: (Broadband stages, not tuned stages)





* A zero is introduced by adding an inductor to the load
  - ↳ the zero partly compensates for the pole's response
  - ↳ inductor also introduces a second pole

Voltage gain $\quad A_v(s) = -g_m \cdot Z_L(s)$

$$Z_L = \frac{R_D + sL_p}{1 + sR_DC_1 + s^2C_1L_p}$$

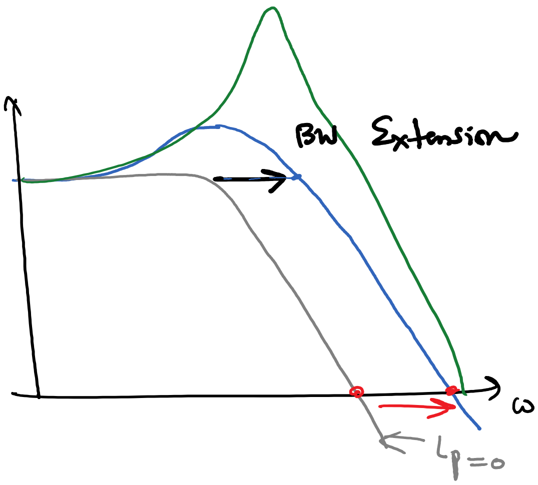
$$= -g_m \cdot R_D \cdot \frac{1 + \frac{sL_p}{R_D}}{1 + sR_DC_1 + s^2C_1L_p}$$

zero

$$\rightarrow A_v(s) = A_o \frac{(1 + s/\omega_z)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \leftarrow \text{2nd order Denominator}$$

$A_o = -g_mR_D, \quad \omega_o = \frac{1}{\sqrt{L_pC_1}}, \quad \omega_z = \frac{R_D}{L_p} = \frac{\omega_o}{Q}$

(parallel



$$Q = \frac{1}{R_D}\sqrt{\frac{L_p}{C_1}}$$

(parallel RLC tank circuit)