ECE 513 - Lecture 19

Tuesday, October 23, 2018 9:36 AM

Tuned LNA Design:

↳ Power Gain & min NF

↳ linearity

↳ Minimum power

figure of merit

$$FoM = \frac{g \cdot IIP_3 \cdot f_0}{(F-1)P} = \frac{OIP_3 \cdot f_0}{(F-1)P}$$

(OIP_3 = $g \cdot IIP_3$)

* In a well-designed LNA, OIP_3 depends only on V_{DD} and $(F-1)$ increases linearly with frequency

$\frac{OIP_3}{(F-1)}$ ↓ with f ↑

$\frac{OIP_3}{(F-1)} f$

* In most cases the input & output return loss ($|S_{11}|$ & $|S_{22}|$) should be better than −15dB over the desired bandwidth

* Reverse isolation & stability factor → amplifier should not turn into an oscillator

* Traditional LNA design (Microwave & mmWave) employed lossless reactive matching networks to transform Z_s to the Z_{sopt} of the discrete transistor.
  - ↳ The transistor itself is biased at the NF_{min} sweet spot.
  - ↳ transfer Z_s to Z_{sopt} using LC network (L-match, π-match, $\frac{\lambda}{4}$ – Transmission line)
    - ↳ noise match
      - ↳ $NF = NF_{min}$

But this is quite different from the impedance match ∵ $R_{sopt} = Re\{Z_{sopt}\}$ and $R_{in} = Re\{Z_{in}\}$ are different.

↳ compromises 'G' = $|S_{21}|$ & input reflection $|S_{11}|$ of the design

* Solution was always unique and optimal.

x With the advent of RFIC & MMICs, the geometry and the optimal bias current were 'fixed up' as design variables.

Read Section 7.3 of Book

LNA Design Methodology

Tuesday, October 23, 2018 9:50 AM

Part I: Active Device Matching

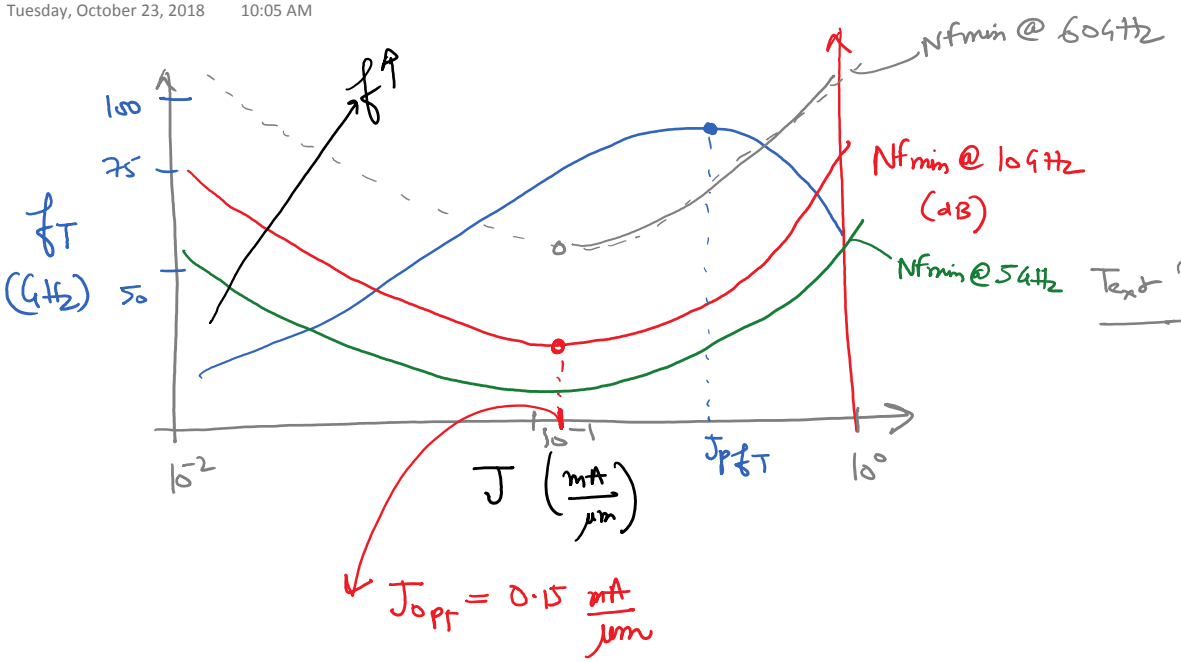
$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|$$

$Y_{sopt} = G_{sopt} + jB_{sopt}$ → $\frac{1}{R_{sopt}}$

$Y_s = G_s + jB_s$

① F_{min} must be made as low as possible to reduce first term
↳ ideally close to the F_{min} of the transistor itself

② Optimal source impedance, $Z_{sopt} = \frac{1}{Y_{sopt}}$, should be made equal to the signal source impedance $Z_s = Z_0 = 50\Omega$.
(i.e. Noise Match with active device itself)
↳ without any passive matching network.



J = Drain current density = $\frac{I_D}{W}$

Text Book fig 7.3

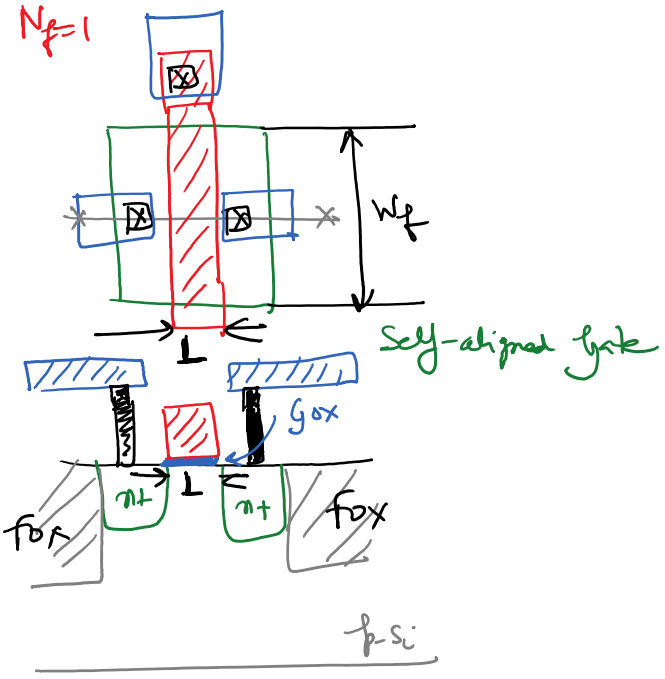
* from this plot for MOSFETs:
  * J_{opt} doesn't change with frequency
    - ↳ Interestingly, J_{opt} in CMOS NMOSFET remained fairly constant at $\leq 0.15 \frac{mA}{\mu m}$ till 65-nm node
      - ↳ In more recent nodes due to device engineering it has increased to $0.2 - 0.3 \frac{mA}{\mu m}$.

* Once J_{OPT} has been selected, the next step is to size the transistor such that Z_{sopT} of the LNA $= Z_0 = 50\Omega$.

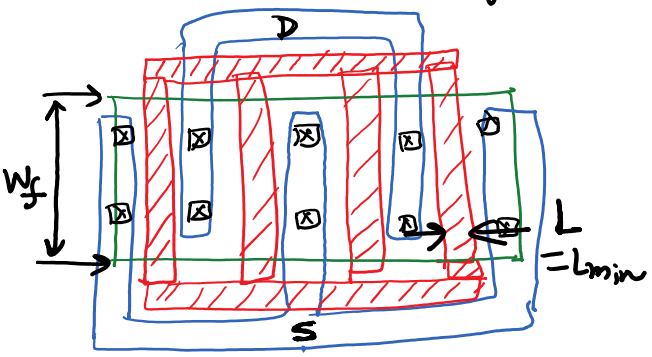
* At a given $J = \frac{I_D}{W}$, the FET noise parameters R_n, G_u, G_{cor} and B_{cor} all scale with the width W.

$$\{R_n, G_u, G_{cor}, B_{cor}\} = f(W_f, N_f)$$

$$W = W_f \cdot N_f$$



$W_f =$
$N_f = 4$



Single gate contact vs double gate contact

* R_g is reduced with double contact

Read from Chapter 4 MOSFET section

for MOSFETs:

$$R_n = \frac{R_{N,FET}}{N_f}$$

$$g_n = g_{N,FET} \cdot W^2 \cdot N_f$$

$$g_{cor} = g_{c,FET} W N_f$$

$$B_{cor} = B_{FET} W N_f$$

* We can describe the optimal source admittance (Y_{SOPT}) as a f^n of f, W_f and N_f as:

$$Y_{SOPT} = N_f W_f \cdot W \cdot \left[\sqrt{g_{c,FET}^2 + \frac{g_{FET}}{R_{FET}}} - j B_{FET} \right]$$

* Alternatively, we can express $Z_{SOPT} = \frac{1}{Y_{SOPT}}$ as a function of small signal parameters and layout geometry of FETs:

$$Z_{SOPT} \simeq \frac{f_{T_{eff}}}{N_f W_f f g'_{m_{eff}}} \left[\sqrt{\frac{g_m' \cdot R_c' + W_f g_m' R_g'}{R_1}} + j \right] \Rightarrow R_{SOPT} + j X_{opt}$$

$R_{SOPT} \rightarrow Z_0$, $X_{opt} \rightarrow 0$ → (1)

* $J = J_{OPT}$
* Sweep and find $W_{OPT} = W_f$ s.t. N_{fmin} is further minimized

$$\Rightarrow N_f = \frac{f_{T_{eff}}}{\simeq W_f} \sqrt{\frac{g_m' \cdot R_g' + W_f g_m' \cdot R_g'}{R_1}}$$ → (2)

$\Rightarrow \quad N_f = \frac{R_{eq}}{Z_0 W_f f} \sqrt{\frac{K_1}{K_1}}$ → ②

↑ # of fingers to set $R_{S-PT} = Z_0 = 50\Omega$

: Noise parameters

$K_1 = 0.5$ to 1 depending upon W_f.

$R_g = R_g(W_f)$ & single or double contact.

+ Eq ① & ② permit the optimization of the transistor geometry as a part of the matching network.

↳ optimizing W_f & N_f have little impact over NF_{min} or T_{OPT}.

* Only minimum gate lengths are used in LNA as NF ↑ with L ↑

Tuesday, October 23, 2018 10:43 AM