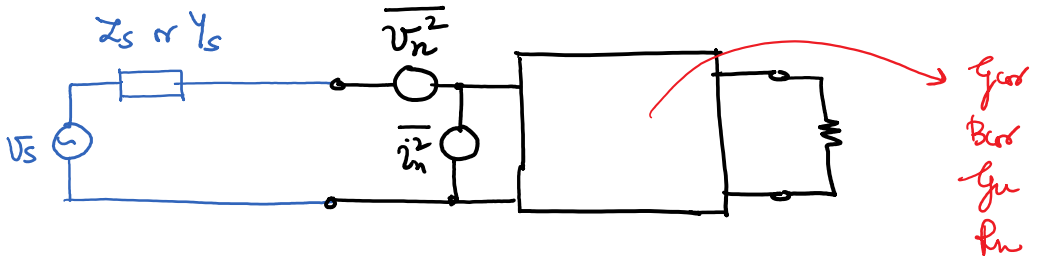
ECE 513 - Lecture 13

Tuesday, October 2, 2018 9:34 AM

$$Y_s = \frac{1}{Z_s}$$



Noise Admittance formalism:

$$Y_{s,opt} = G_{s,opt} + jB_{s,opt}$$

$$B_{s,opt} = -B_{cor}$$

$$G_{s,opt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}}$$

$$R_n \triangleq \frac{\overline{v_n^2}}{4kT\Delta f}$$

$$G_u \triangleq \frac{\overline{i_n^2}}{4kT\Delta f}$$

$$F_{min} = 1 + 2R_n(G_{cor} + G_{s,opt})$$

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2$$

$Y_s = Y_{s,opt}$ for $F = F_{min}$

$R_n \Rightarrow$ Sensitivity parameter of NF to noise impedance mismatch

Noise Impedance formalism:

$Z_{cor}' \neq Y_{cor}$

$i_n = i_n$

$v_n = v_u + v_c = v_u + Z_{cor}' i_n$

$Z_{cor}' = R_{cor}' + j X_{cor}'$

$Z_s = Z_{s,opt}$ for $F = F_{min}$

$R_{s,opt} + j X_{s,opt}$ → $X_{s,opt} = -X_{cor}'$

$\sqrt{R_{cor}'^2 + \frac{R_u}{G_n'}}$

$G_n' \triangleq \frac{\overline{i_n^2}}{4kT\Delta f}$

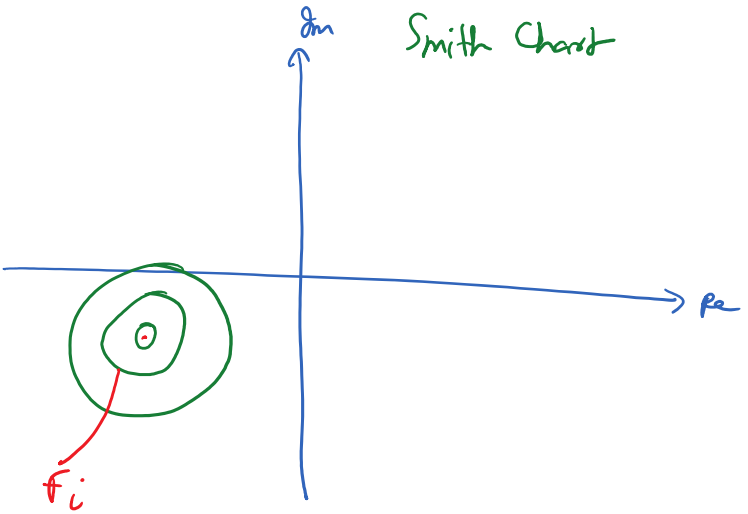
$R_u' \triangleq \frac{\overline{v_u^2}}{4kT\Delta f}$

$F_{min} = 1 + 2G_n'(R_{cor}' + R_{s,opt})$

4 $F = F_{min} + \frac{G_n'}{R_s} |Z_s - Z_{s,opt}|^2$

Constant Noise Circles

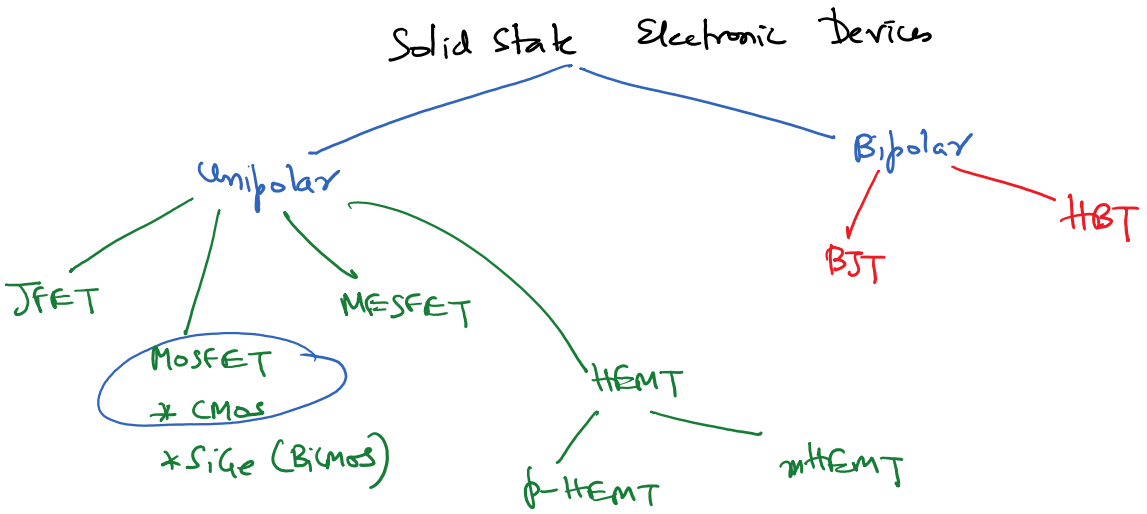
$$F = F_{min} + \frac{R_n}{G_s} \left| Y_s - Y_{s,opt} \right|^2$$



$F < F_i$

Chapter- 4

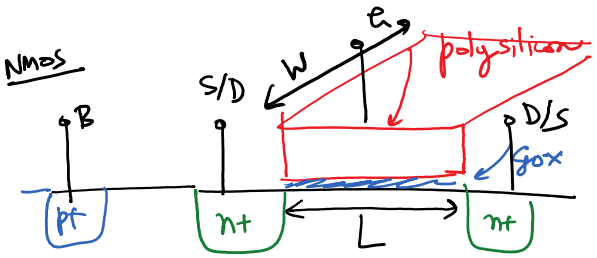
Tuesday, October 2, 2018 9:50 AM



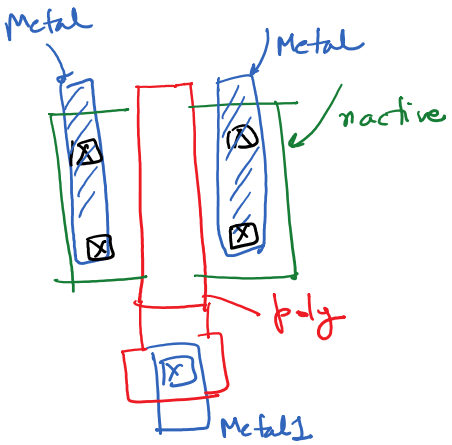
Si
SiGe
GaAs
GaN

Tuesday, October 2, 2018 9:54 AM

MOSFETs (CMOS) → NMOS / PMOS



p-Si



Long-channel

$L > 1\mu m$

Cutoff

$V_{GS} < V_{TH,n}$

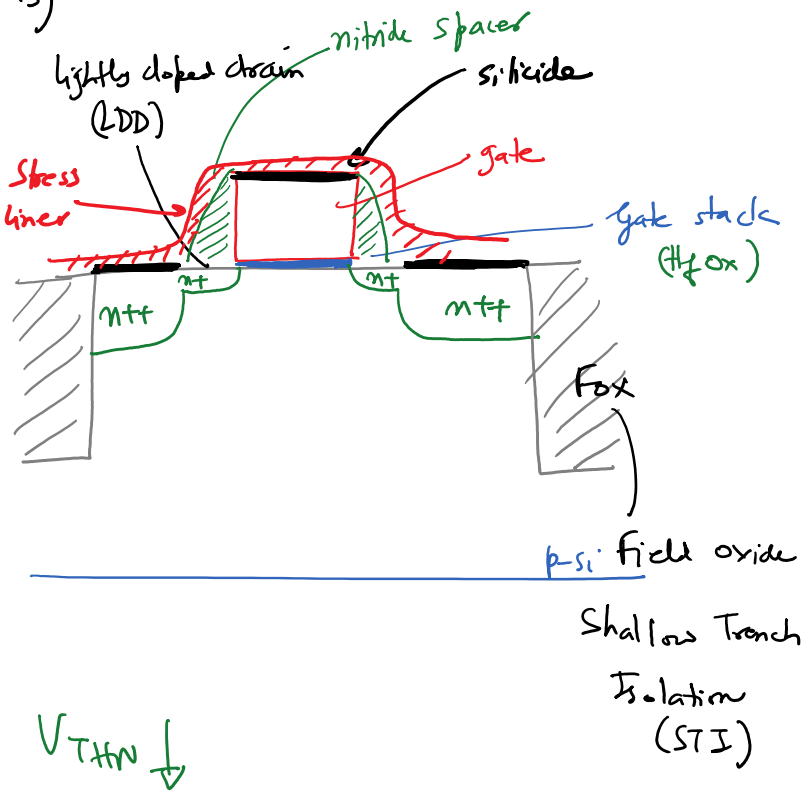
$V_{GS} > V_{TH,n}$

$$I_D = \begin{cases} k_n \frac{W}{L}\left[(V_{GS}-V_{TH,n})V_{DS} - \frac{V_{DS}^2}{2}\right] & V_{DS} < V_{GS}-V_{TH,n} \quad \text{(Triode)} \\ \frac{1}{2}k_n \frac{W}{L}(V_{GS}-V_{TH,n})^2 \times (1+\lambda V_{DS}) & V_{DS} > \underbrace{V_{GS}-V_{TH,n}}_{V_{DS,sat}} \quad \text{(SAT)} \end{cases}$$

Tuesday, October 2, 2018 10:00 AM

Nanoscale MOSFET (before FINFETs)

≤ 14nm



Silicide ⇒ Co or Ti reacting with Si

↳ Silicide

V_{DD} has been shrinking

0.5 μm CMOS → 5V

65 nm CMOS → 1V

14nm CMOS ≈ 0.8 – 1V

V_{THN} ↓

Metal gates for controlling the work function → V_{THN}.

Tuesday, October 2, 2018 10:10 AM

DC I-V characteristics

* Short-channel I-V characteristics depart from the square-law equations

In simplest form:

In saturation

$$I_D = W v_{x0} C_{ox}^{inv} (V_{GS} - V_{THN})(1 + \lambda V_{DS})$$

v_{x0} ⇒ effective carrier velocity at the source

C_{ox}^{inv} ⇒ effective capacitance of the channel in inversion

λ ⇒ channel length parameter

* mobility μ_n ⇒ has been replaced by v_{x0} (velocity saturation regime)

* not a square law equation anymore

DIBL ⇒ Drain induced barrier lowering

$V_{DS} \uparrow \Rightarrow V_{THN} \downarrow$

V_{THN} has dependence upon Length

$L \uparrow \Rightarrow V_{THN} \uparrow$

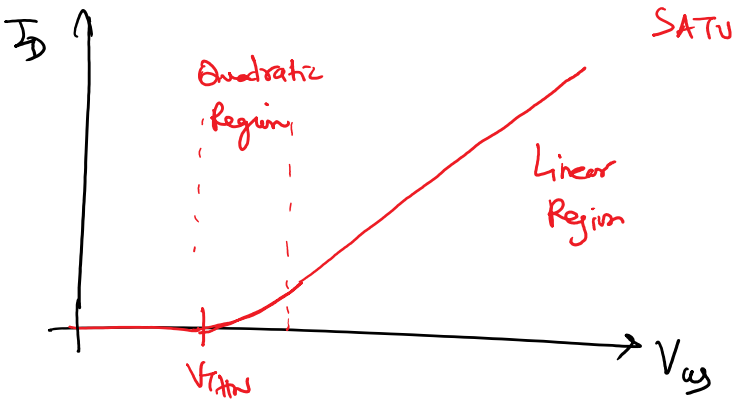
* Can't fix a V_{GS} and "size" all transistors accordingly

↳ Constant Current Density Design Techniques

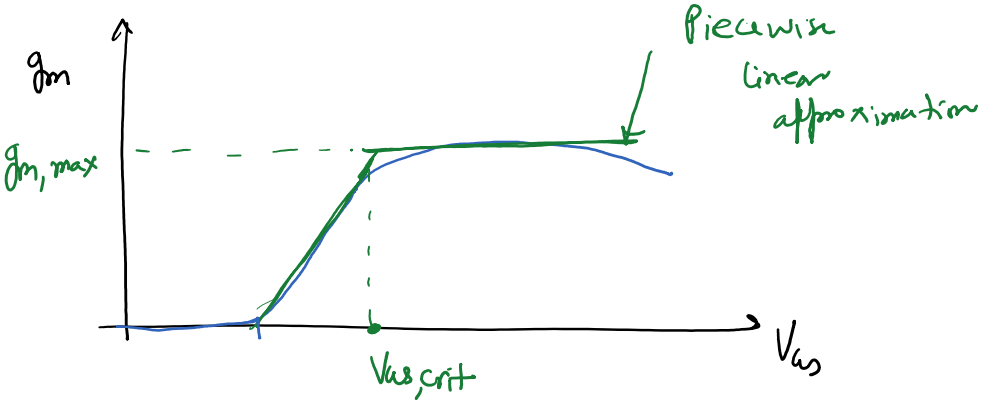
↳ $\frac{I_D}{W}$

Tuesday, October 2, 2018 10:17 AM

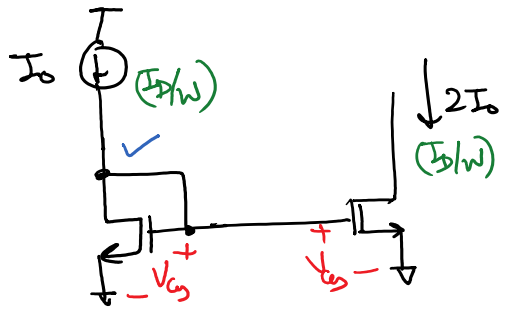
Fig 4.35



$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$



Constant Current Density (I_D/W) Design Methodology



① fix the gate length ($L \geq$ 2–5 L_{min} typically)

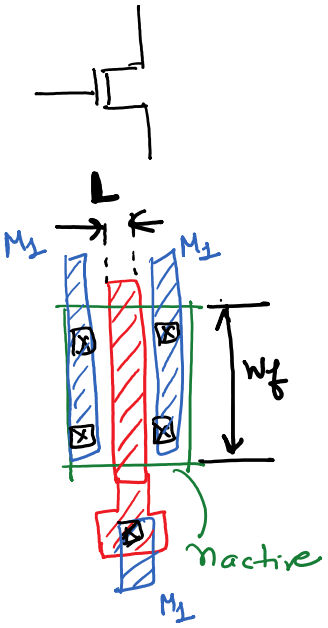
② Transistors are first biased at the desired constant current density (I_D/W)

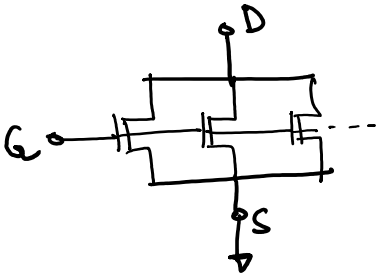
③ Then the desired current (I_D) or g_m are achieved by fixing the gate fingers width (W_f) and varying the number of fingers in parallel

Essentially we are keeping $\frac{I_D}{W}$ constant across the circuit

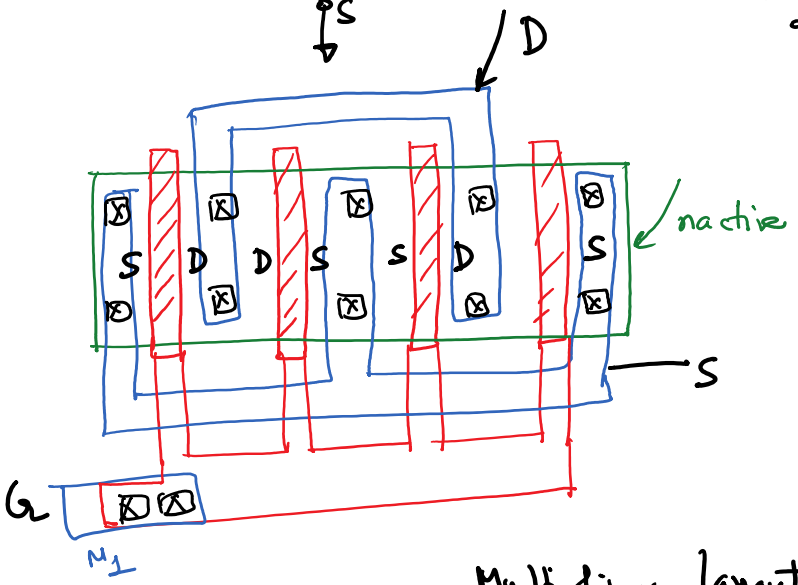
$$\frac{I_D}{W} = \text{constant} \Rightarrow \frac{g_m}{I_D} \text{ constant}$$

* Actual value of V_{GS} is of secondary importance.





Source has more capacitance
↳ connected to ground

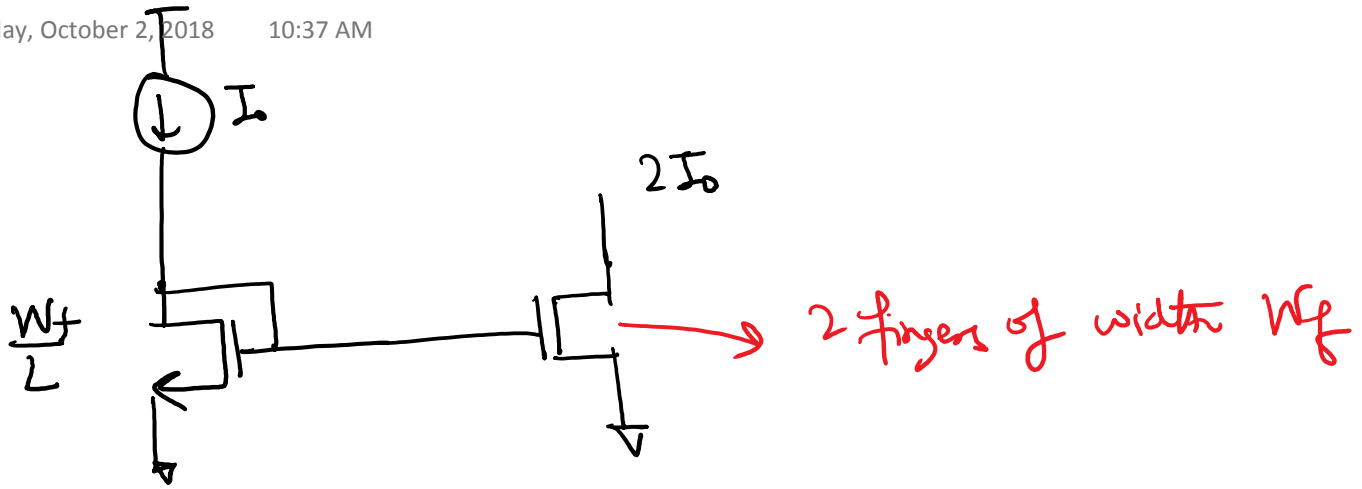


Multi finger layout

N_f = Number of fingers = 4 here

Effective $W = N_f \cdot W_f$

* FINFETs designs are more restrictive

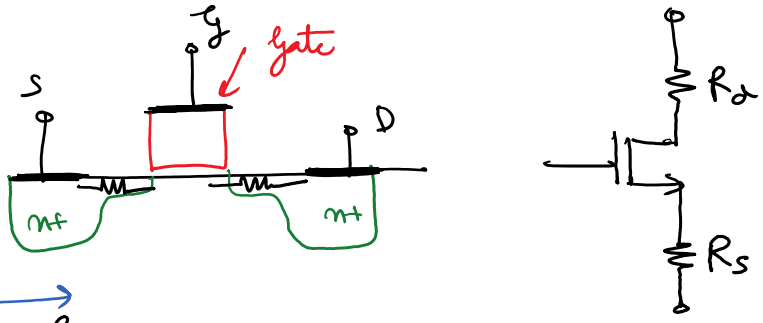


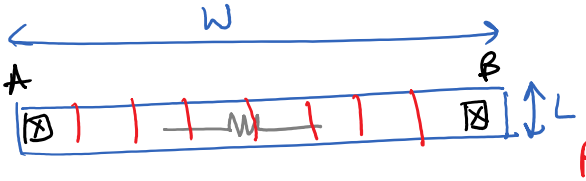
Layout Matching Techniques-

Tuesday, October 2, 2018 10:38 AM

Parasitic Resistances and Capacitances :

* Source and drain resistances due to the LDD



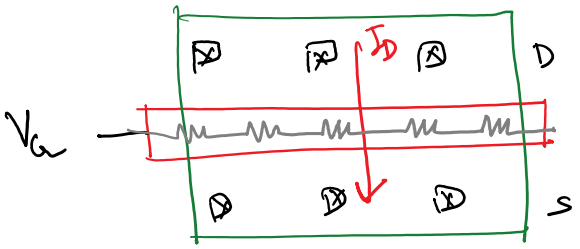


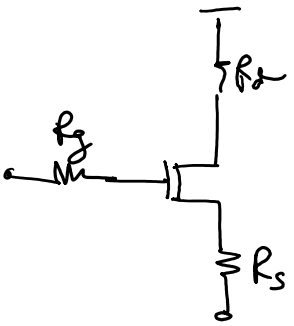
Resistance per square $\Rightarrow R_\square$

$R_{AB} = R_\square \times$ num of squares

Different material on chip have different $R_\square$

$$R = R_\square \cdot \frac{W}{L}$$





Effectively Gate Resistance

$$R_g \approx \frac{1}{3} R_{\square} \frac{W}{L}$$

due to distributed nature

* See Section 4.2.5 in the Book