

ECE 413/513 – RADIO FREQUENCY IC DESIGN

LNA DESIGN TESTBENCH

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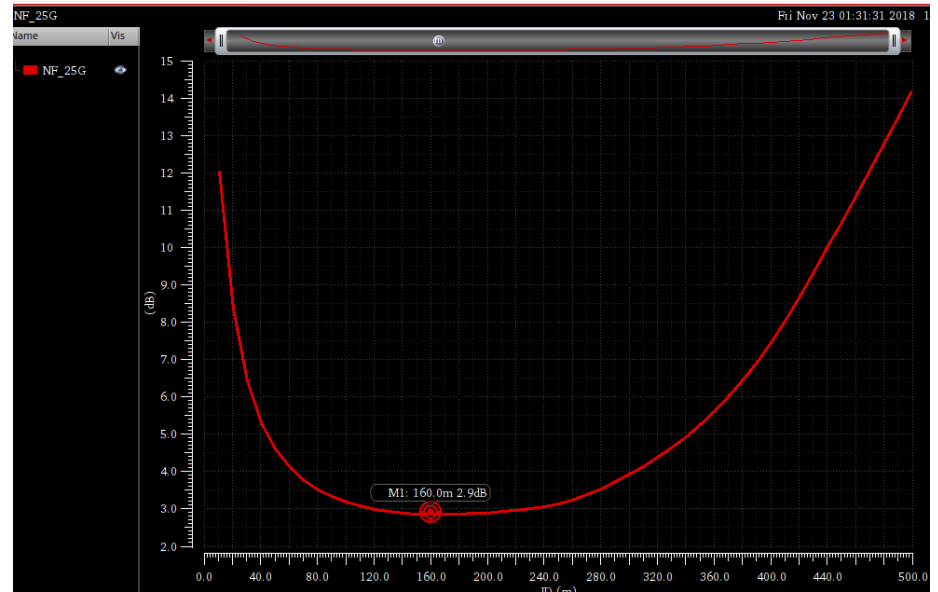
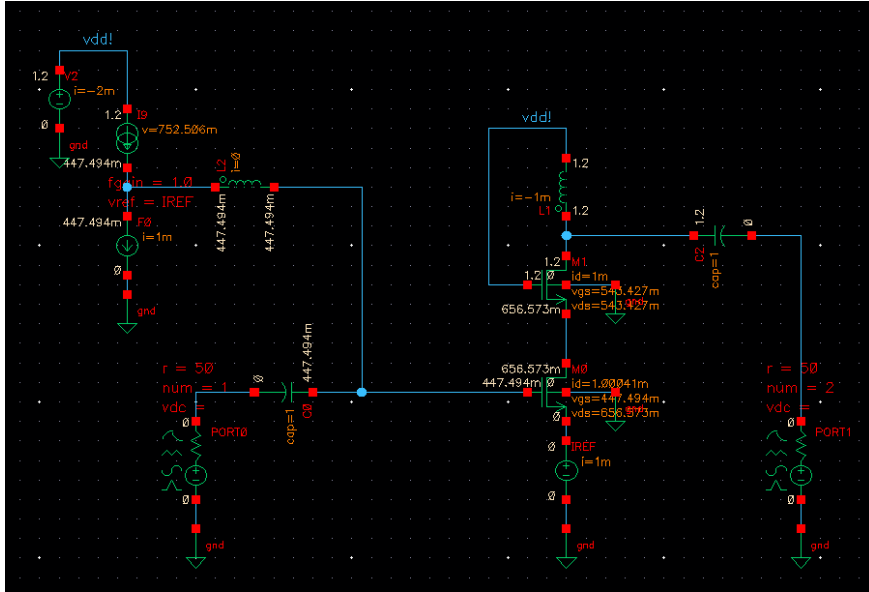
LNA DESIGN EXAMPLE

- Design an LNA using the 90nm CMOS models
 - with $V_{DD}=1.2V$
 - $f_0=25GHz$ center frequency

Parameter	Value
R_{in}	50 Ω
Load	100fF
Frequency range	23.5-26.5 GHz
Power gain ($G_T= S_{21} ^2$)	>8dB
S_{11}	<-15dB
S_{12}	<-35dB
NF	<4dB
IIP ₃	>-5dBm



CASCODE DEVICE

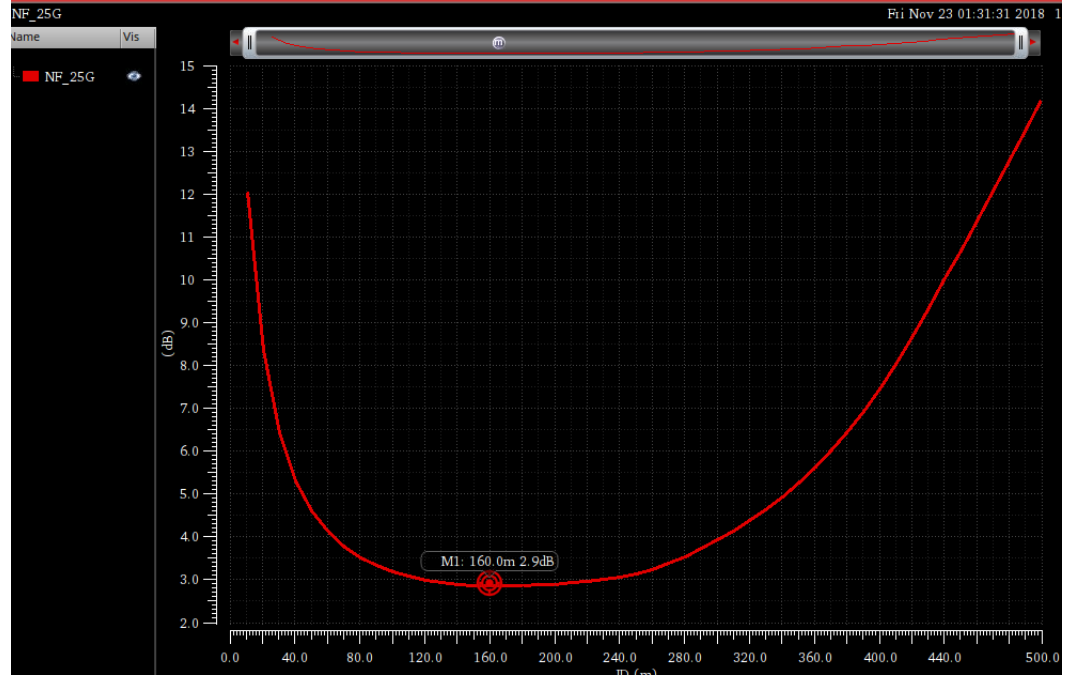


Schematic: NF_Cascode_Testbench

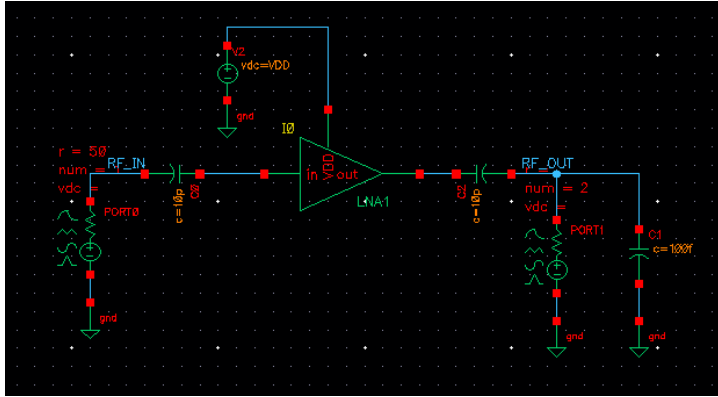


J_{OPT} AND NF_{MIN}

- $J_{OPT@28GHz} = 0.16 \text{ mA}/\mu\text{m}$
- $W_f = 1 \mu\text{m}$
- N_f (multiplier) = 80
- $NF_{min} = 2.9 \text{ dB}$
- $R_{OPT} = 79.3 \Omega$



LNA TESTBENCH



Name	Value
1 LS	95p
2 frf1	28G
3 prf	-40
4 LD	210p
5 LG	500p
6 JD	160m
7 VDD	1.2
8 Wf	1u
9 Nr	80
10 ID	$JD * 1e3 * Wf$
11 Rg	$(60 + 444 * (0.1 + Wf / 6)) / (2 * Nr)$

Name/Signal/Expr	Value	Plot	Save	Save Options
1 Gumx dB10		<input type="checkbox"/>	<input type="checkbox"/>	
2 Gmax dB10		<input type="checkbox"/>	<input checked="" type="checkbox"/>	
3 fMAX		<input type="checkbox"/>	<input type="checkbox"/>	
4 NFmin		<input type="checkbox"/>	<input checked="" type="checkbox"/>	
5 Gopt	13.2708m	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
6 Bopt	20.3501m	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

S-Parameter Analysis

Ports: /PORT0 /PORT1

Sweep Variable: Frequency

Sweep Range: Start 15G Stop 35G

Output port: /PORT1

Input port: /PORT0

Mode: Single-Ended

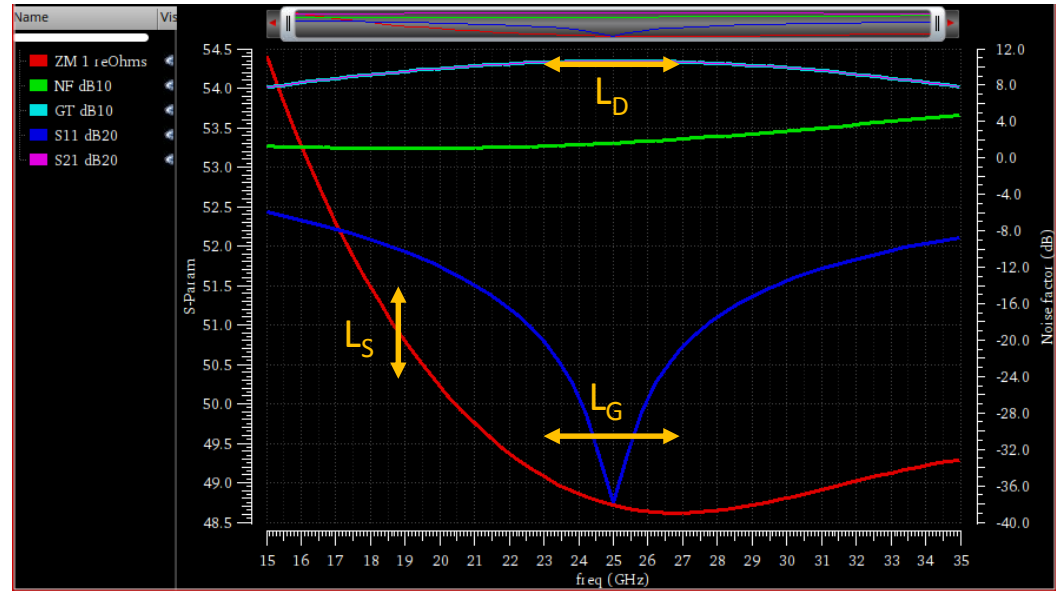
Schematic: LNA_Testbench

- Swap between LNA1 and LNA2 cellviews for ideal or modeled inductors



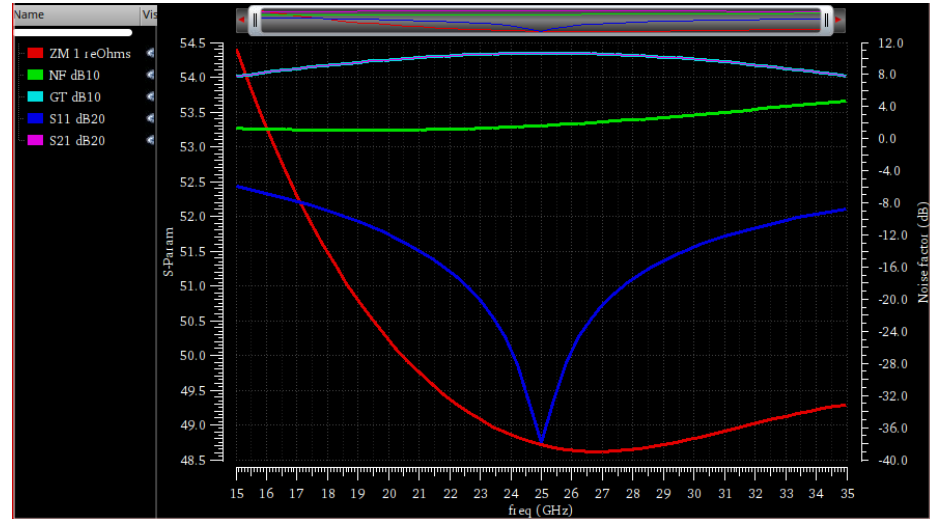
LNA DESIGN USING SP ANALYSIS

- Starting with $W_f=1\mu\text{m}$, $N_f=80$
- Start with ballpark values for the inductors from hand-calculations
- First tune L_S to obtain R_{in} (real part of ZM_1) close to $\sim 50\Omega$
- Next, tune L_G to center S_{11} null at f_0
- Tune L_D to center the peak of S_{21} at f_0



S-PARAM SIMULATION

- $W_f=1\mu\text{m}$, $N_f=80$
- $L_S=95\text{pH}$, $L_G=500\text{pH}$, $L_D=210\text{pH}$
- **NF=1.75dB**
- $R_{IN} \sim 49\Omega$
- $X_{IN} \sim 0$
- $R_{OPT}=75\Omega$ and $X_{OPT}=49\Omega$
 - A perfect noise match is not needed for meeting the NF specification
 - More suited for mmWave designs



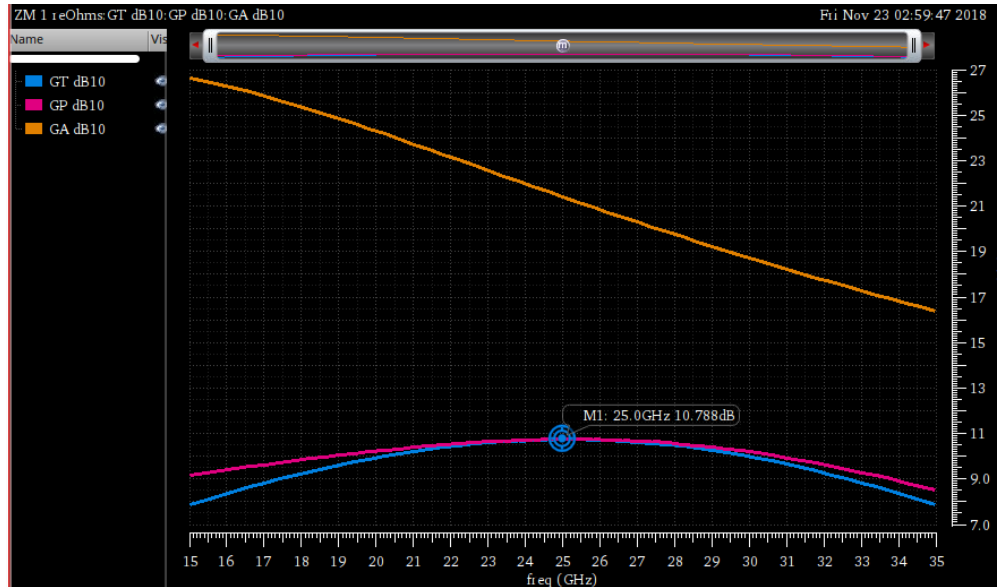
POWER GAIN DEFINITIONS

- G_T , transducer power gain
 - Ratio between the power delivered to the load and the power available from the source
 - $G_T = |S_{21}|^2$
- G_P , operating power gain
 - Ratio between the power delivered to the load and the power input to the LNA, $G_P = |S_{21}|^2 / (1 - |S_{11}|^2) < G_T$
 - The closer G_P to G_T , the better is the input matching
- G_A , available power gain
 - Ratio between the power available from the LNA and the power available from the source, $G_A = |S_{21}|^2 / (1 - |S_{22}|^2) > G_T$
 - The closer G_T to G_A , the better is the output matching
- Read more in the *SpectreRF Workshop: LNA Design Using SpectreRF PDF* and Section 3.1 in the Textbook



POWER GAINS

- Here, $G_T = |S_{21}|^2 = 10.78\text{dB}$
 - Meets the 8dB specification



1DB COMPRESSION POINT SIMULATION

- Harmonic Balance analysis is used
- See the tutorial from Linkoping for details
- Testbench is provided
 - LNA_P1dB_Testbench

The screenshot displays the Cadence ADE L (32) interface for an LNA_P1dB_Testbench schematic. The main window shows the Design Variables table, the Analyses panel with 'hb' selected, and the Direct Plot Form dialog. The Direct Plot Form dialog is configured for Harmonic Balance Analysis with the following settings:

- Plotting Mode: Append
- Analysis: hb
- Function: Compression Point
- Select: Port (fixed Rpport)
- Format: Output Power
- Gain Compression (dB): 1
- Input Power Extrapolation Point (dBm): (Defaults to -20)
- Input Referred 1dB Compression: (Dropdown)
- 1st Order Harmonic Table:

Order	Power (dBm)
0	0
1	25G
2	50G
3	75G
4	100G
5	125G
- Loadpull Contours: (Unchecked)
- Add to Outputs: (Checked)
- OK, Cancel, Help buttons.

The bottom status bar indicates: INFO (ADE-3071): Simulation completed successfully. reading simulation data... successful.



IP3 SIMULATION

- Harmonic Balance analysis is used
- See the tutorial from Linköping University or the Spectre LNA Design workshop PDF for details
- Testbench is provided
 - [LNA_IIP3_Testbench](#)

Choosing Analyses -- ADE L (26)

stb pz lf sp
 envlp pss pac pstb
 pnoise pxf psp qpss
 qpac qpnoise qpxf qpss
 hb hbac hbstb hbnoise
 hbsp hbxf

Harmonic Balance Analysis

Transient-Aided Options

Run transient?

Detect Steady State Stop Time(tstab)

Save Initial Transient Results (saveinit) no yes

Dynamic Parameter

Tones Frequencies Names

Multi-divider Mode

Number of Tones 1 2 3 4

Fundamental Frequency

Number of Harmonics

Oversample Factor

Tone 1 be LO or signal which causes the most nonlinearity.

Freqdivide Ratio for Tone 1

Harmonics

Accuracy Defaults (errpreset)

conservative moderate liberal

Oscillator

Sweep

Loadpull

LSSP

Compression

Enabled

Options...

OK Cancel Defaults Apply Help

Direct Plot Form

Plotting Mode

Analysis

hb_mt

Function

Voltage Current
 Power Voltage Gain
 Current Gain Power Gain
 Transconductance Transimpedance
 Compression Point IPN Curves
 Power Contours Reflection Contours
 Power Added Eff. Power Gain Vs Pout
 Comp. Vs Pout Node Complex Imp.

Select

Single Point Input Power Value (dBm)

Input Referred IP3 Order

	Freq. (Hz)	_hb_ton	_hb_ton
3rd	1.2G	-3	3
	24.2G	3	-2
	24.6G	2	-1
Order	25G	1	0
	25.4G	0	1
	25.8G	-1	2

	Freq. (Hz)	_hb_ton	_hb_ton
1st	400M	-1	1
	800M	-2	2
	1.2G	-3	3
Order	24.2G	3	-2
	24.6G	2	-1
	25G	1	0

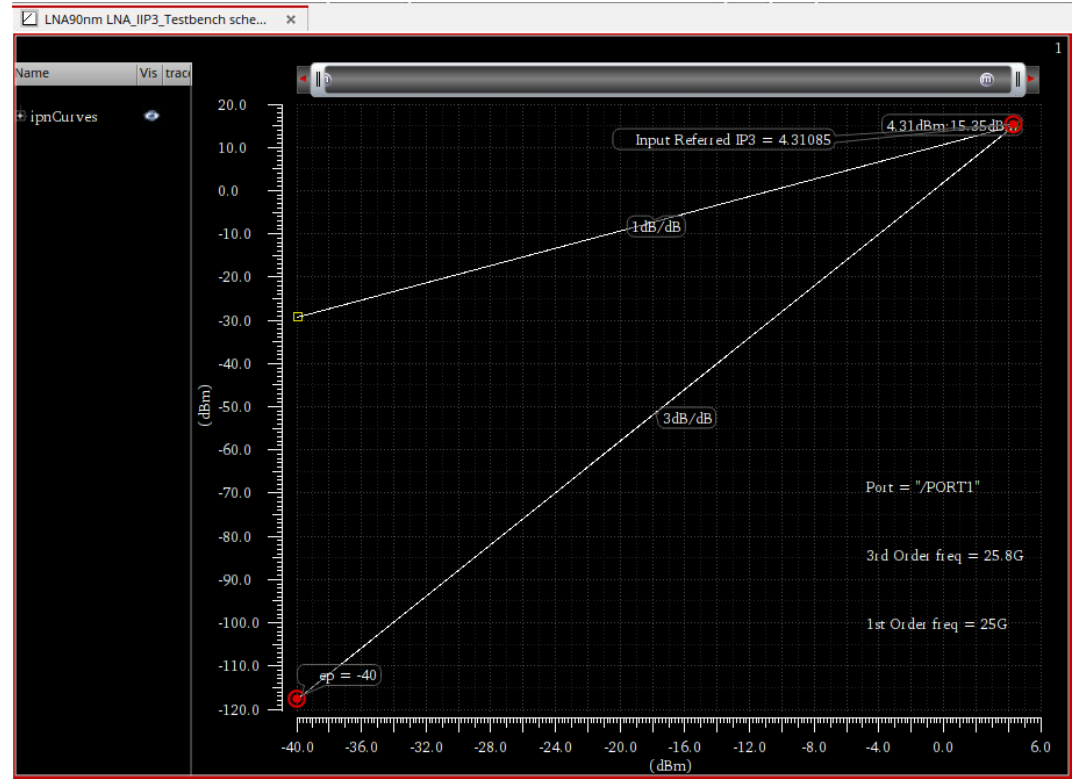
Add To Outputs

> Select Port on schematic...

OK Cancel Help

IP3 SIMULATION

- Here $IIP_3 = 4.31\text{dBm}$ which easily meets the -5dBm specification
- Linearity trades-off with gain based on the amount of inductive degeneration and g_m
- See textbook section on LNA design for linearity



TRANSIENT SIMULATION

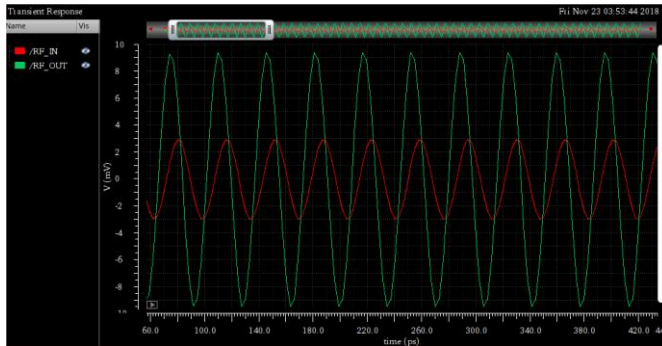
- You can perform more simulations provided in the tutorials from Linkoping and Cadence for stability, gains, large-signal NF etc.
- One can visualize the operation of the LNA from transient simulations
- Schematic: [LNA_tran_Testbench](#)



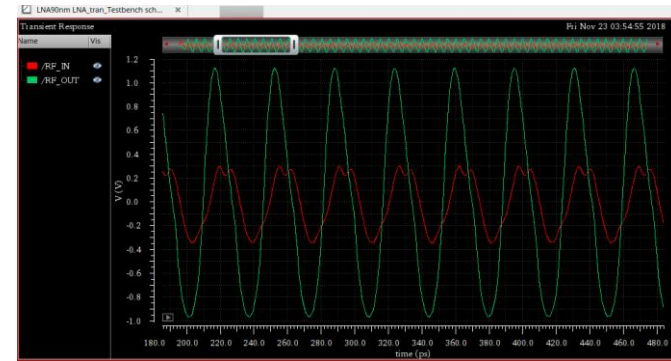
TRANSIENT SIMULATION

- You can verify the voltage/power gain from the transient waveforms
- Linearity degrades as the input power increases. Note output signals are about to clip (and the transistor is entering triode) as the input level is increased beyond the IIP_3 input-level.

$P_{in} = -40\text{dBm}$



$P_{in} = +5\text{dBm}$



REFERENCES

- T. Johansson, “LNA Simulation using Cadence SpectreRF,” RF IC Design 2018, Linköping University.
 - http://www.isy.liu.se/en/edu/kurs/TSEK03/laboration/TSEK03_2018_LAB1_LNA-simulation.pdf
- Cadence SpectreRF Workshop: LNA Design Using SpectreRF.
 - https://www.ece.ucsb.edu/Faculty/rodwell/Classes/ece218c/tutorials_etc/CadenceLNA.pdf
- S. Voinigescu, “High-Frequency Integrated Circuits,” The Cambridge RF and Microwave Engineering Series, 1st ed., 2013

