ECE 413/513 –RADIO FREQUENCY IC DESIGN

LNA DESIGN TESTBENCH

VISHAL SAXENA
VSAXENA@UIDAHO.EDU

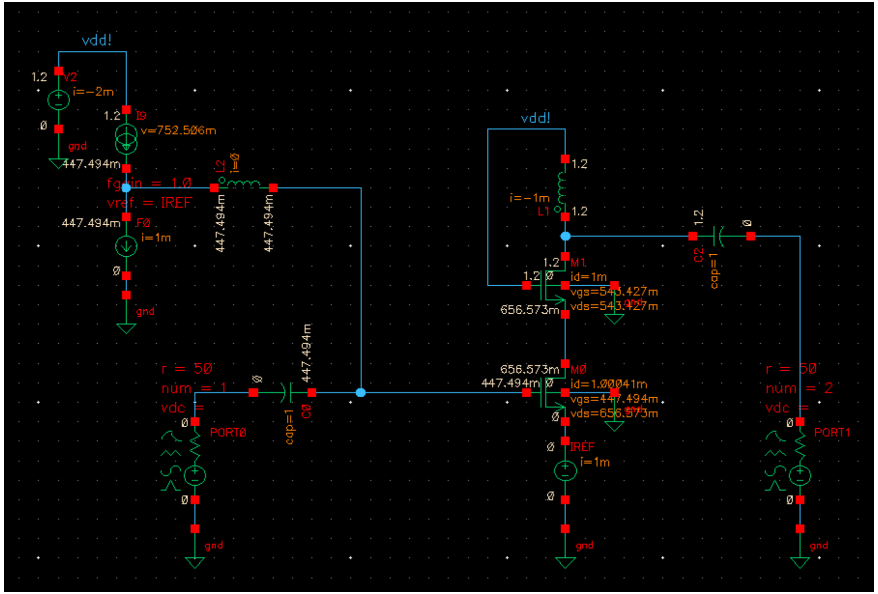
University of Idaho
College of Engineering

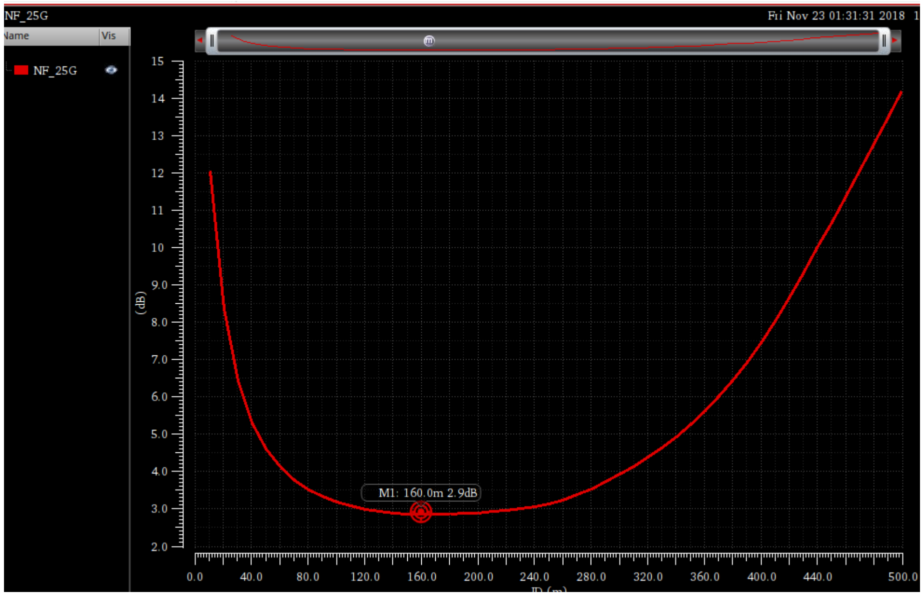
LNA DESIGN EXAMPLE

- Design an LNA using the 90nm CMOS models
  - with V_{DD}=1.2V
  - f_0=25GHz center frequency

Parameter	Value
R_{in}	50Ω
Load	100fF
Frequency range	23.5-26.5 GHz
Power gain ($G_T=\|S_{21}\|^2$)	>8dB
S_{11}	<-15dB
S_{12}	<-35dB
NF	<4dB
IIP_3	>-5dBm

CASCODE DEVICE

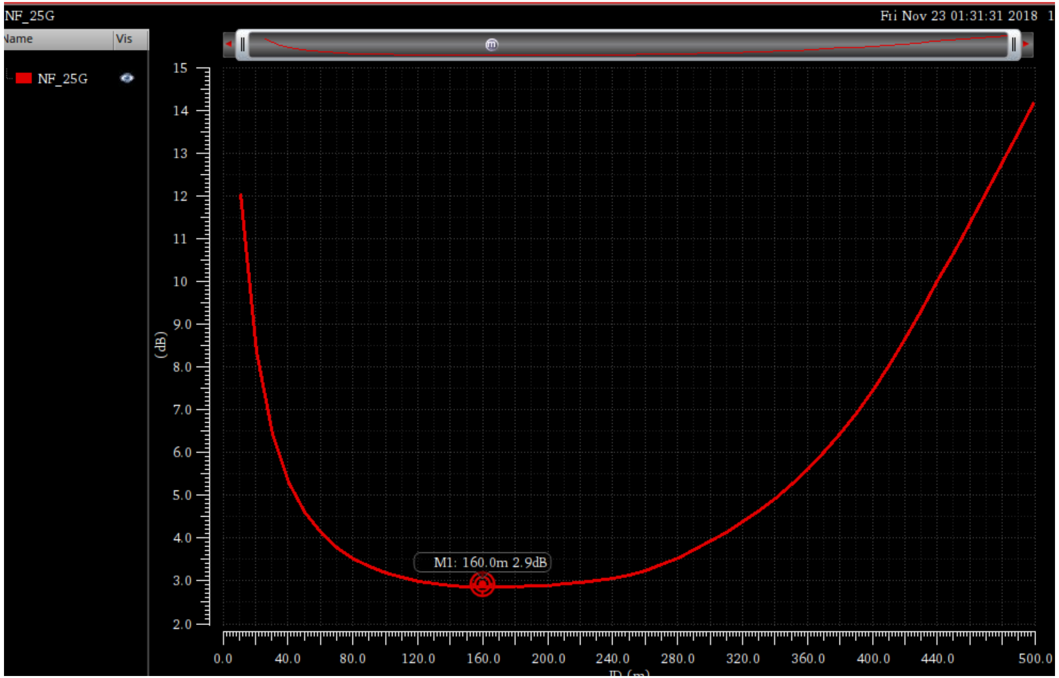




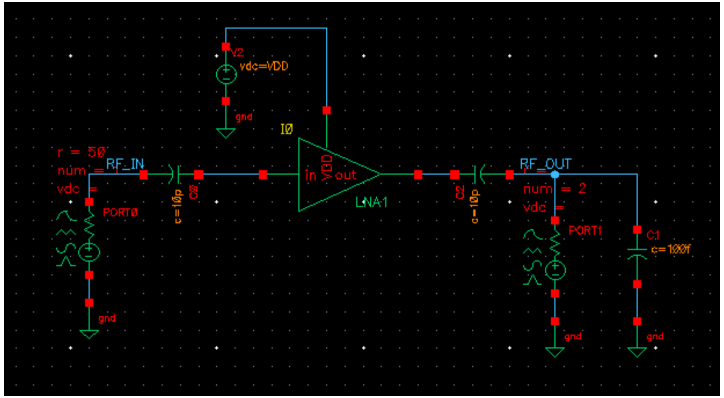
Schematic: NF_Cascode_Testbench

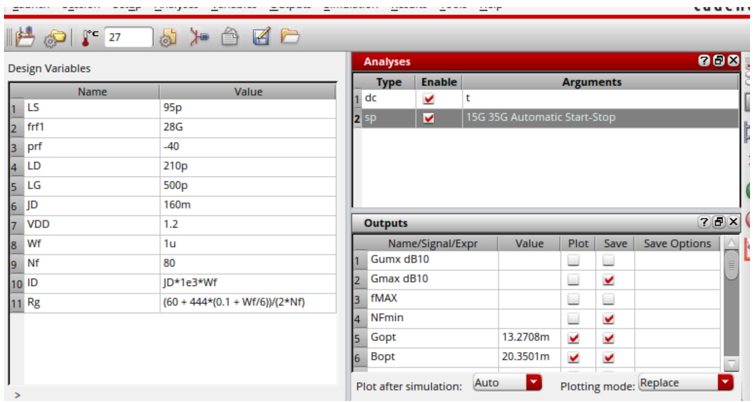
J_{OPT} AND NF_{MIN}

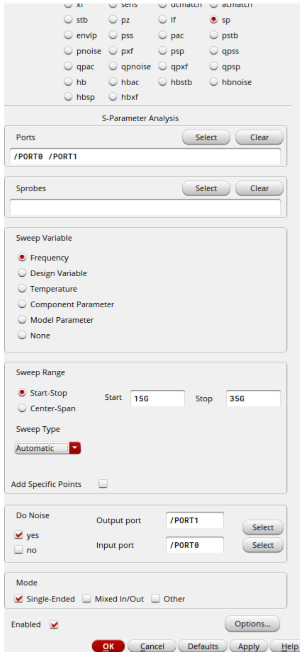
- $J_{OPT@28GHz}$=0.16mA/μm
- W_f=1μm
- Nf (multiplier) = 80
- NF_{min}=2.9dB
- R_{OPT}=79.3Ω



LNA TESTBENCH





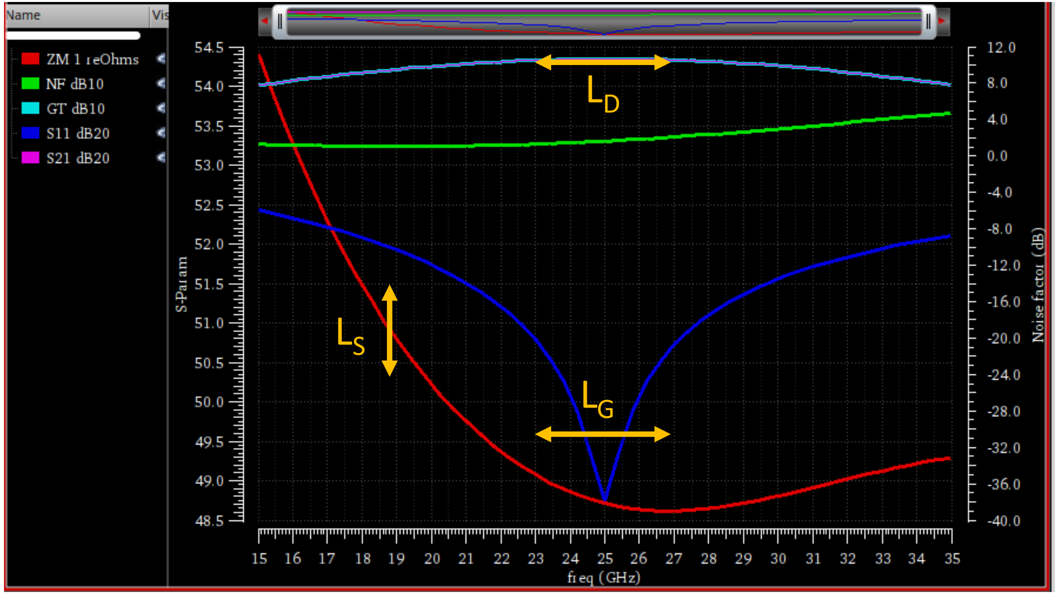


Schematic: LNA_Testbench

- Swap between LNA1 and LNA2 cellviews for ideal or modeled inductors

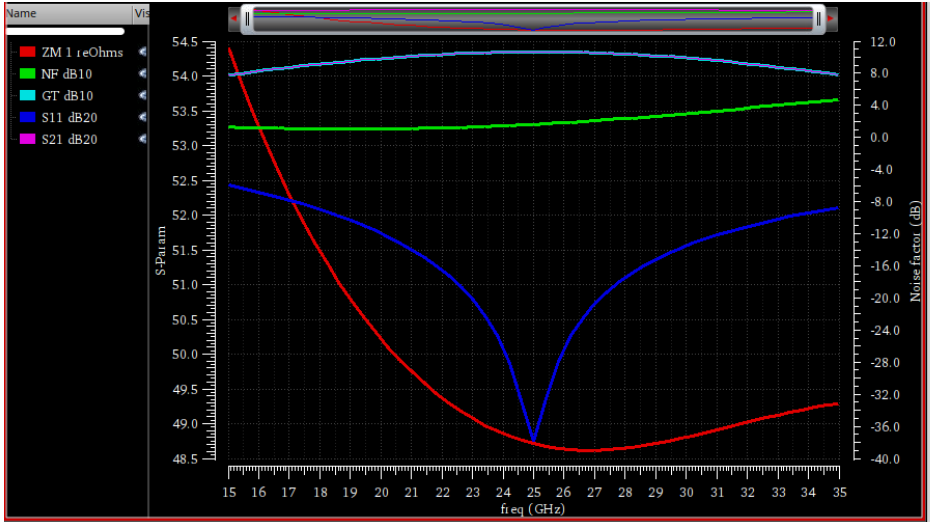
LNA DESIGN USING SP ANALYSIS

- Starting with W_f=1μm, N_f=80
- Start with ballpark values for the inductors from hand-calculations
- First tune L_S to obtain R_{in} (real part of ZM_1) close to ~50Ω
- Next, tune L_G to center S_{11} null at f_0
- Tune L_D to center the peak of S_{21} at f_0



S-PARAM SIMULATION

- W_f=1µm, N_f=80
- L_S=95pH, L_G=500pH, L_D=210pH
- NF=1.75dB
- R_{IN} ~49Ω
- X_{IN} ~0
- R_{OPT}=75Ω and X_{OPT}=49Ω
  - A perfect noise match is not needed for meeting the NF specification
  - More suited for mmWave designs

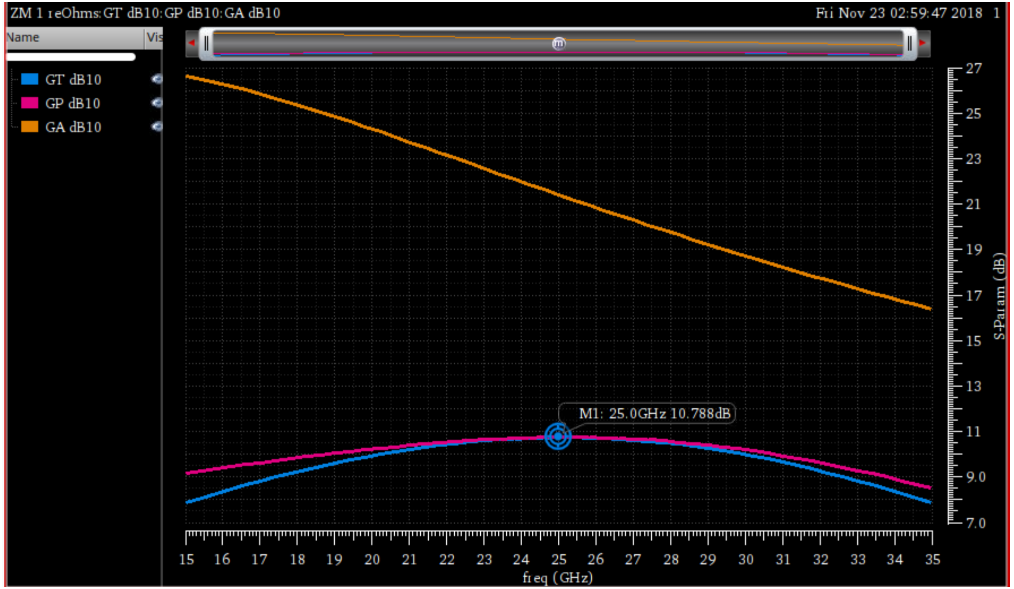


POWER GAIN DEFINITIONS

- G_T, transducer power gain
  - Ratio between the power delivered to the load and the power available from the source
  - $G_T = |S_{21}|^2$
- G_P, operating power gain
  - Ratio between the power delivered to the load and the power input to the LNA, $G_P = |S_{21}|^2/(1-|S_{11}|^2) < G_T$
  - The closer G_P to G_T, the better is the input matching
- G_A, available power gain
  - Ratio between the power available from the LNA and the power available from the source, $G_A = |S_{21}|^2/(1-|S_{22}|^2) > G_T$
  - The closer G_T to G_A, the better is the output matching
- Read more in the *SpectreRF Workshop: LNA Design Using SpectreRF* PDF and Section 3.1 in the Textbook

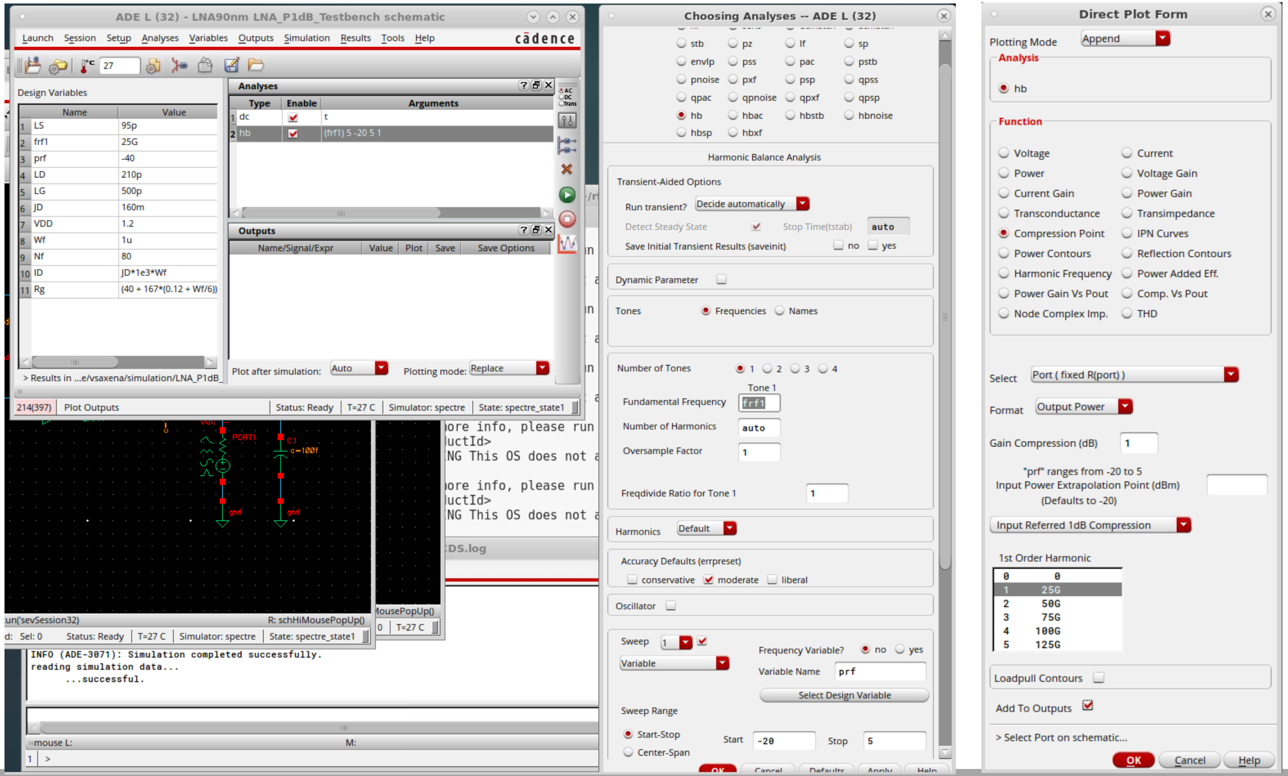
POWER GAINS

- Here, $G_T=|S_{21}|^2 = 10.78dB$
  - Meets the 8dB specification



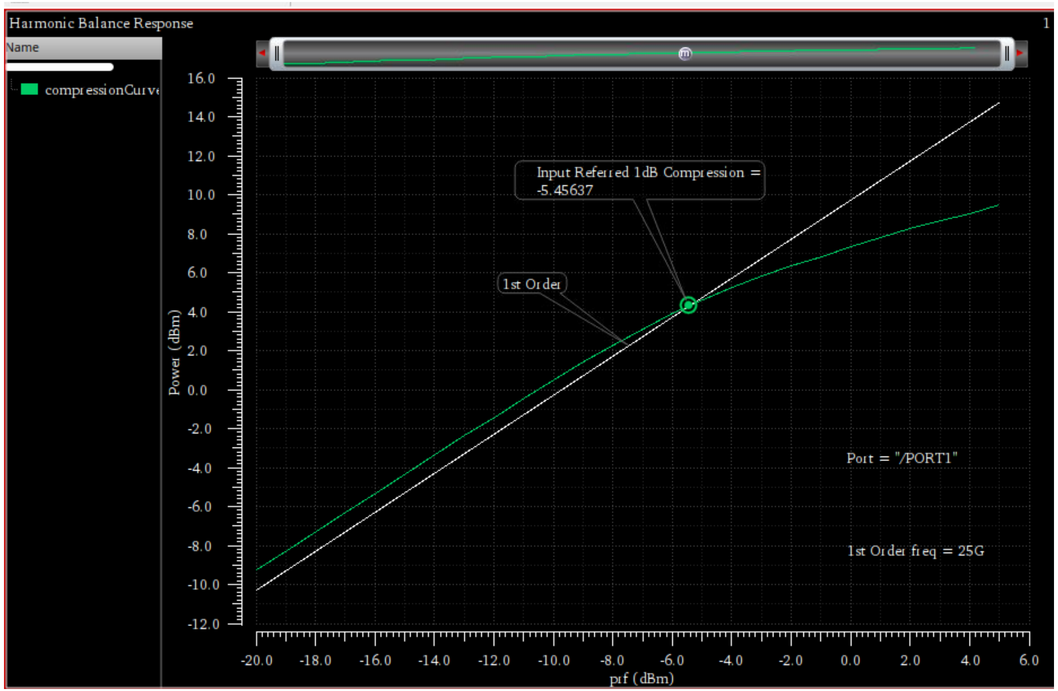
1DB COMPRESSION POINT SIMULATION

- Harmonic Balance analysis is used
- See the tutorial from Linkoping for details
- Testbench is provided
  - LNA_P1dB_Testbench



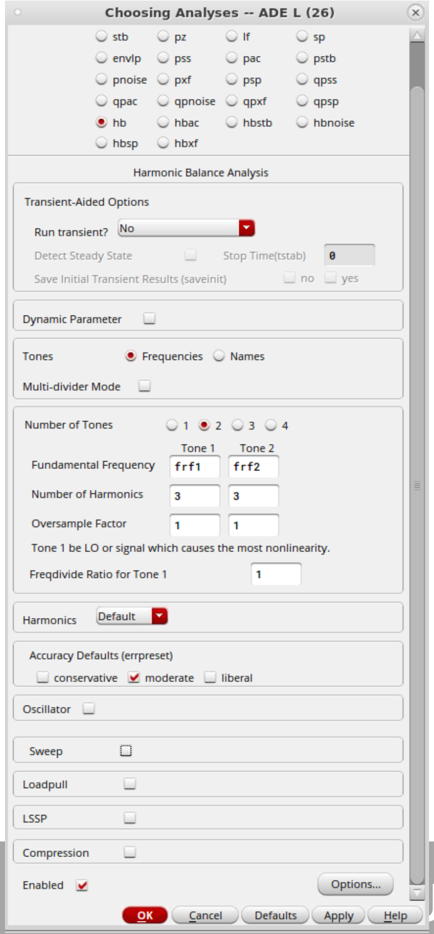
1DB COMPRESSION POINT SIMULATION

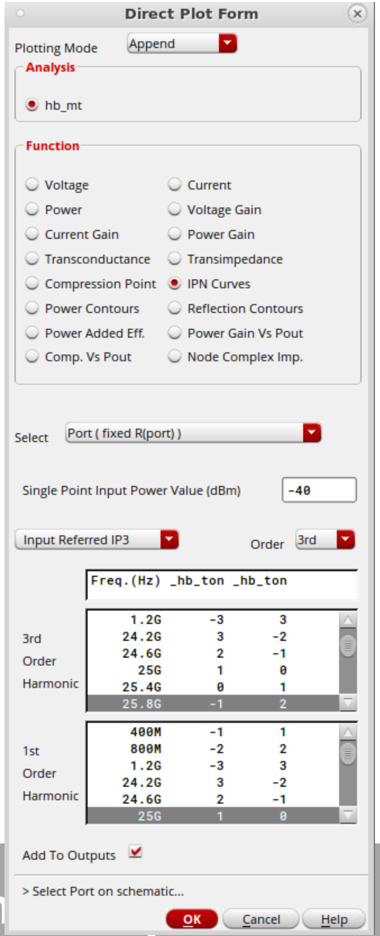
- Here, P_{1dB} = -5.45 dBm



IP3 SIMULATION

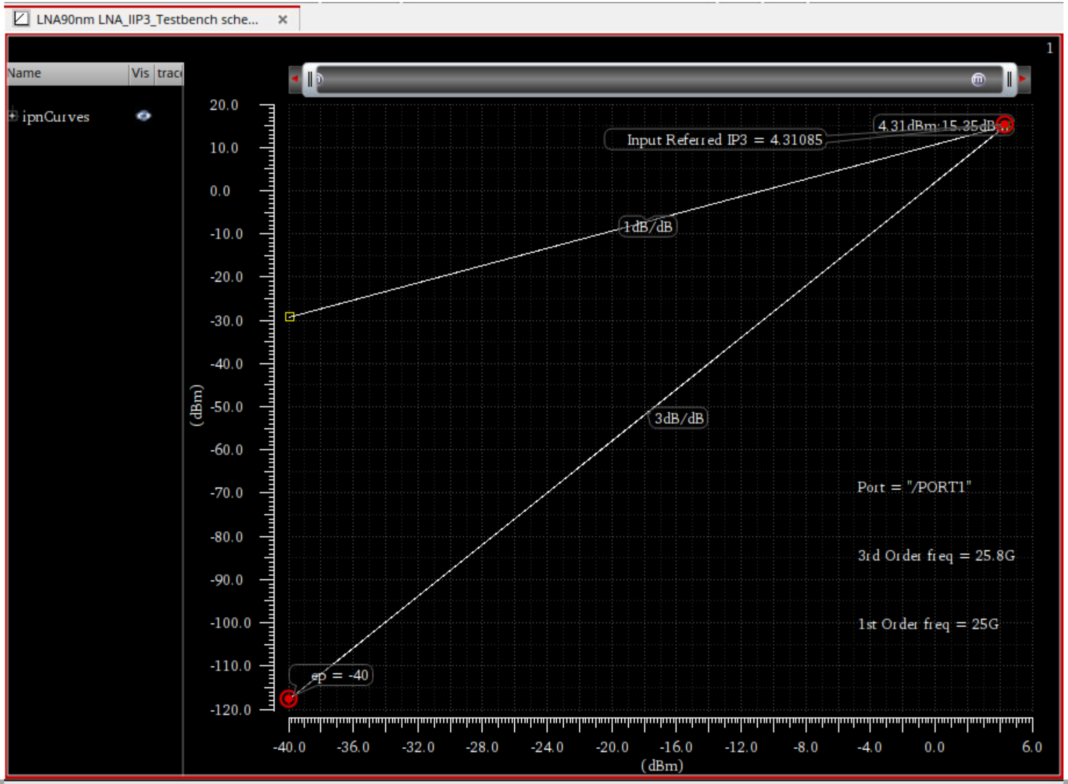
- Harmonic Balance analysis is used
- See the tutorial from Linkoping University or the Spectre LNA Deisgn workshop PDF for details
- Testbench is provided
  - LNA_IIP3_Testbench





IP3 SIMULATION

- Here IIP_3=4.31dBm which easily meets the -5dBm specification
- Linearity trades-off with gain based on the amount of inductive degeneration and g_m
- See textbook section on LNA design for linearity



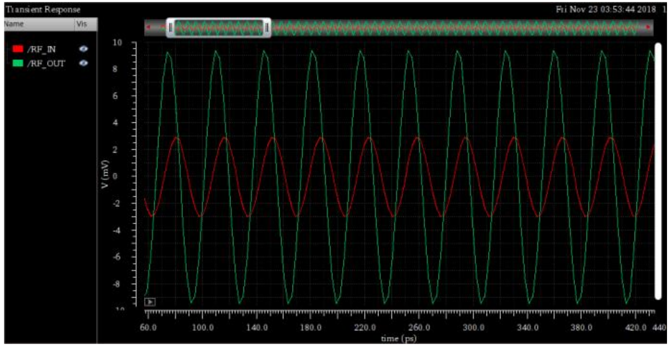
TRANSIENT SIMULATION

- You can perform more simulations provided in the tutorials from Linkoping and Cadence for stability, gains, large-signal NF etc.
- One can visualize the operation of the LNA from transient simulations
- Schematic: LNA_tran_Testbench

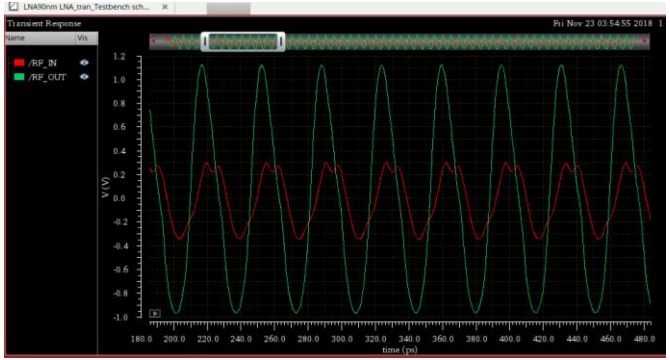
TRANSIENT SIMULATION

- You can verify the voltage/power gain from the transient waveforms
- Linearity degrades as the input power increases. Note output signals are about to clip (and the transistor is entering triode) as the input level is increased beyond the IIP_3 input-level.

P_{in}=-40dBm



P_{in}=+5dBm



REFERENCES

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  - http://www.isy.liu.se/en/edu/kurs/TSEK03/laboration/TSEK03_2018_LAB1_LNA-simulation.pdf
- Cadence SpectreRF Workshop: LNA Design Using SpectreRF.
  - https://www.ece.ucsb.edu/Faculty/rodwell/Classes/ece218c/tutorials_etc/CadenceLNA.pdf
- S. Voinigescu, “High-Frequency Integrated Circuits,” The Cambridge RF and Microwave Engineering Series, 1st ed., 2013