Homework 4

ECE 5/413 – Radio Frequency IC Design

Note:
1. Use the 45nm GPDK CMOS with $V_{DD} = 1.1V$ on the ECE servers for design problems.

Problem 1: Impedance Match

1. Design an L-match network to match a $R_L = 10\Omega$ load to a $R_s = 50\Omega$ source. Assume that the center frequency is $f_0 = 2.4GHz$.

2. As you know that L-match has only two-degrees of freedom where the impedance transformation ratio and center frequency is specified. Redo part (1) using a π-match network with an additional constraint that the total bandwidth of the match is $BW = 20MHz$.

3. Simulate the above two networks in Cadence Spectre and plot $|S_{11}|$ and $|S_{21}|$ (in dB scale) with labeled center frequency and bandwidth. Compare the BW and resulting Q from these plots with your hand-calculations.
   You can copy example testbenches by adding the line[1] to your cds.lib file in the ece513 directory.

Problem 2: RLC Circuits
Consider the network shown in Fig. 1. Using the method of series-parallel transformations, simplify the network to find the impedance at $100MHz$ when $C = 1pF$, $L = 10nH$, $R_s = 15\Omega$ and $R_p = 1k\Omega$.

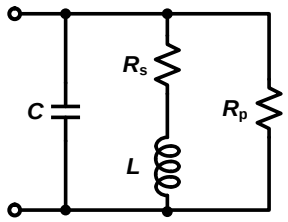

Figure 1

[1]DEFINE **Passive_RLC** /home/vsaxena/rficdesign/**Passive_RLC**

Problem 3: Transistor FoM Calculations:
A 32-nm CMOS technology has the following transistor data (**Note: '** denotes per unit width):
$L = 22nm$, $J_{OPT} = 0.3\frac{mA}{\mu m}$
$J_{pfT} = 0.5\frac{mA}{\mu m}$ for $0.3V < V_{DS} < 0.9V$.
$g'_{mn} = g'_{mp} = 2.6\frac{mS}{\mu m}$
$g'_{on} = g'_{op} = 0.4\frac{mS}{\mu m}$
For both NMOS and PMOS devices:
$C'_{gs} = 0.55\frac{fF}{\mu m}$; $C'_{gd} = 0.3\frac{fF}{\mu m}$
$C'_{sb} = C'_{db} = 0.55\frac{fF}{\mu m}$
R'_s=R'_d =$200\,\Omega \times \mu m$
Total R_g with finger contacted on one side is $96\Omega \times \mu m$.
Noise parameter: $k_1 = 0.5$.

1. Calculate the f_T and f_{MAX} of the NMOS and PMOS transistors using the small signal equivalent circuit parameters. ***Hint:*** Textbook Eqs. 4.124 & 4.125, and set $R_i = 0$. You don't need to know the NMOS width as 'μm' cancels out in the expressions.

2. Calculate the corresponding f_T of the NMOS cascode stage. ***Hint:*** Substitute $2C_{gd}$ instead of C_{gd} in the first term in Eq. 4.124 to account for Miller effect in the bottom NMOS.

3. Assuming the NMOS transistor is biased at J_{OPT} and the finger width is $W_f = 1\mu m$, what is the total gate width ($N_f \cdot W_f$) and bias current (I_D) of an NMOS whose R_{sOPT} is 50Ω at 140 GHz? What is the corresponding R_n? ***Hint:*** From Eq. 4.53:
   $R_{sOPT} \approx \frac{f_T}{fWg'_{meff}}\sqrt{\frac{g'_m(R'_s+W_fR'_g(W_f))}{k_1}}$
   where $g'_{meff} = \frac{g'_m}{1+g_mR_s}$, and
   $R_n \approx \frac{R'_g}{N_fW_f} + \frac{R'_s}{N_fW_f} + \frac{k_1}{g'_m \cdot N_fW_f}$,

4. Calculate NF_{min} (in dB) for the transistor in part (3) for f =2.4GHz, 28GHz, 60GHz and 140GHz. ***Hint:*** Textbook Eq. 4.55.

5. Calculate the intrinsic slew-rate of the NMOS and PMOS transistors given by $SL_i = \frac{J_{pf_T}}{C'_{gd}+C'_{db}}$ in terms of $\frac{V}{ps}$.

Problem 4: RF Transistor Characterization: Setup your Cadence environment using directions provided in the wiki. Copy the library with simulation testbenches by adding the line[2] to your cds.lib. Using the standard 1V transistors in the 45nm CMOS GPDK with sizes of $\frac{W}{L} = \frac{120nm \times 5}{45nm}$:

1. Generate I_D-V_{GS} and I_D-V_{DS} plots for NMOS and PMOS.

2. Plot $\frac{g_m}{W}$ vs V_{GS} as in Textbook Fig. 4.36. Comment on the plot. Hint: g_m is obtained by deriv(I_D) vs V_{GS} plot using Tools→Calculator in ADE-L.

3. Plot C_{gs} and C_{gd} vs V_{GS} as in Textbook Fig. 4.43. Also, plot C_{gs} and C_{gd} vs V_{DS} for $V_{GS} = 0.7V$(Fig. 4.44).

4. The testbenches are designed to sweep current density $J_D = \frac{I_D}{W}$ and plot f_T, f_{MAX} and NF_{min}@$50GHz$ for the NMOS. You will also find the example Tools→Parametric Analysis files used for sweeping variables in the *rficdesign* directory. R_g is modeled using Eqn. 4.109 from the book. Plot f_T and f_{MAX} as functions of current density J_D, and find J_{pf_T} and $J_{pf_{MAX}}$ for the technology. See Textbook Figs. 4.62-4.65.

5. Plot NF (in dB) *vs* J_D and find J_{OPT} and NF_{min} for the NMOS at 5GHz, 28GHz and 60GHz. See Textbook Fig. 4.66. Comment on the trends.

6. Why is constant current density (J_D) method for MOSFET sizing preferred over other schemes such as using a fixed V_{GS}? ***Hint:*** Read Textbook Sections 4.2.8 and 9.

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